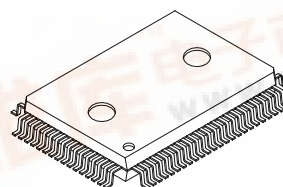


SONY**CXP84412/84416****CMOS 8-bit Single Chip Microcomputer****Description**

The CXP84412/84416 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, 32kHz timer/counter, remote control reception circuit and other servo systems besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84412/84416 also provides and a sleep/stop function that enables lower power consumption.

80 pin QFP (Plastic)

**Features**

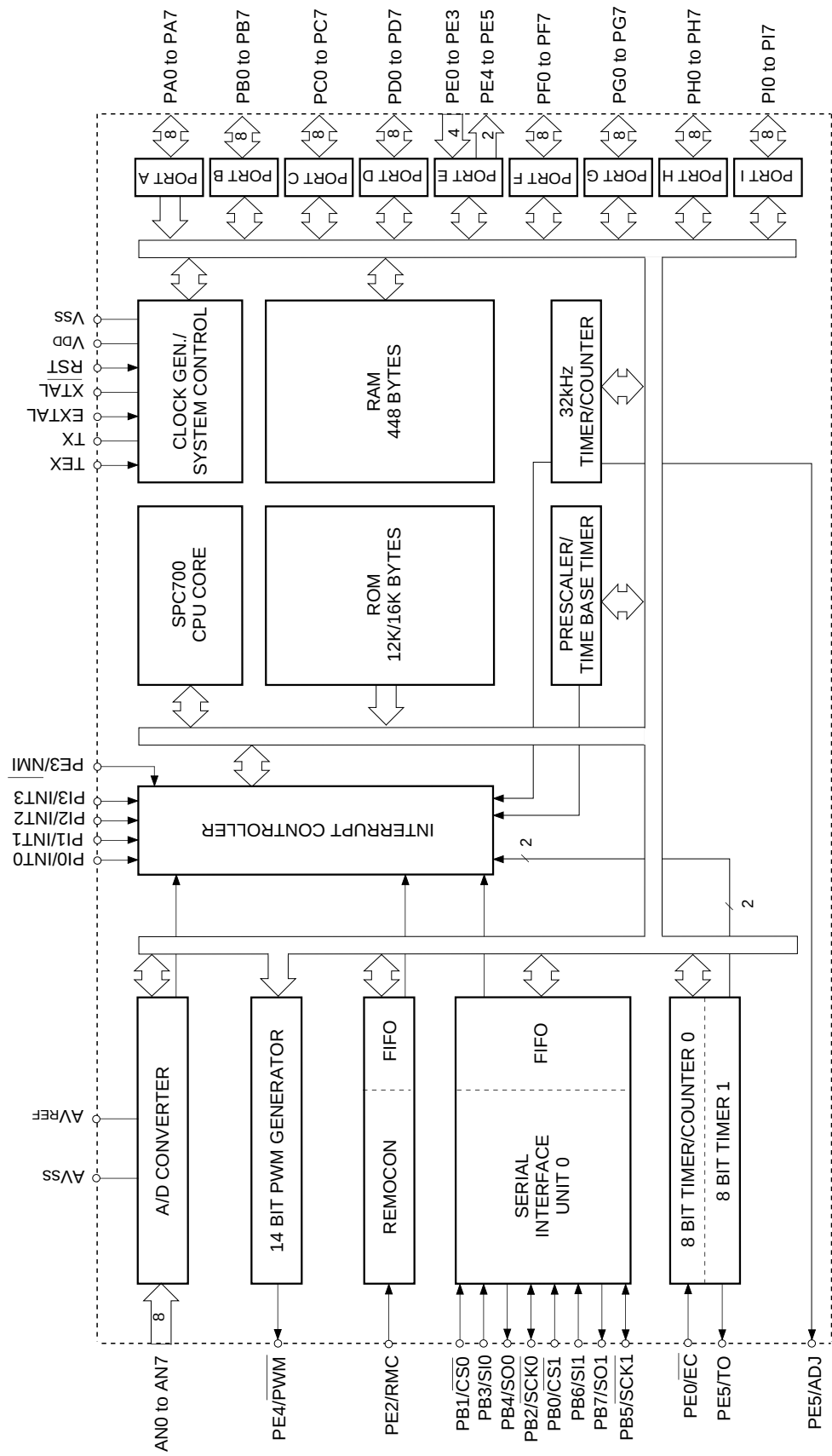
- Wide-range instruction system (213 instructions) to cover various types of data.
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 400ns at 10MHz operation
 - 122μs at 32kHz operation
- Incorporated ROM capacity
 - 12Kbytes (CXP84412)
 - 16Kbytes (CXP84416)
- Incorporated RAM capacity
 - 448bytes
- Peripheral functions
 - A/D converter
 - 8-bit, 8-channel, successive approximation method
 - (Conversion time of 32μs/10MHz)
 - Serial interface
 - Incorporated 8-bit, 8-stage FIFO
 - (Auto transfer for 1 to 8 bytes), 2 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer,
 - 32kHz timer/counter
 - Remote control reception circuit
 - Incorporated 6-stage FIFO 8-bit measurement counter
 - PWM output for tuner
 - 14 bits
- Interruption
 - 12 factors, 12 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 80-pin plastic QFP
- Piggyback/evaluation chip
 - CXP84400 80-pin ceramic QFP

Structure

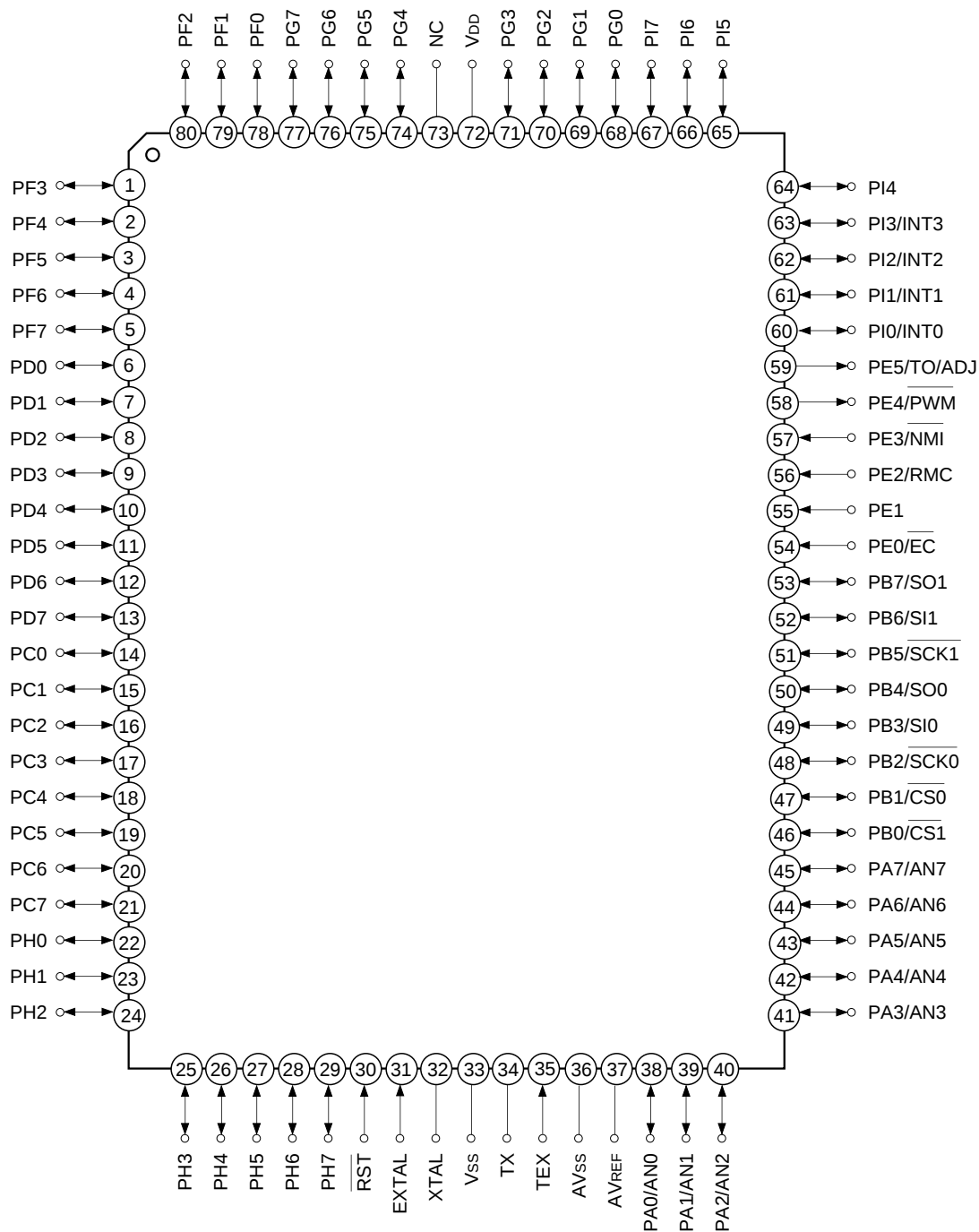
Silicon gate CMOS IC



Block Diagram



Pin Assignment (Top View)



Note) NC (Pin 73) must be connected to V_{DD}.

Pin Description

Pin code	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/analog input	(Port A) 8-bit I/O port. I/O can be set in single bit units. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/ $\overline{\text{CS1}}$	I/O/input	(Port B) 8-bit I/O port. I/O can be set in single bit units. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	Chip select input for serial interface (CH1).
PB1/ $\overline{\text{CS0}}$	I/O/input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/input		Serial data input (CH0).
PB4/SO0	I/O/output		Serial data output (CH0).
PB5/ $\overline{\text{SCK1}}$	I/O/input/output		Serial clock I/O (CH1).
PB6/SI1	I/O/input		Serial data input (CH1).
PB7/SO1	I/O/output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC}}$	Input/input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. Incorporation of pull-up resistor can be set through the software. (8 pins)	External event inputs for timer/counter.
PE1	Input		
PE2/RMC	Input/input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/output		14-bit PWM output.
PE5/TO/ADJ	Output/output/output		Rectangular wave output for 16-bit timer/counter (duty output 50%). Output for 32kHz oscillation frequency demultiplication.
PF0 to PF7	I/O	(Port F) 8-bit output port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

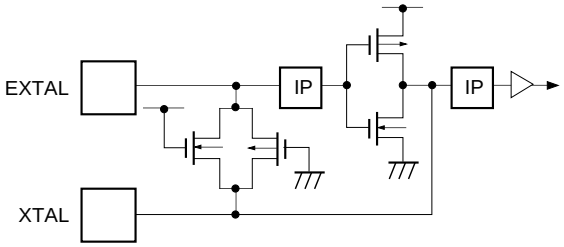
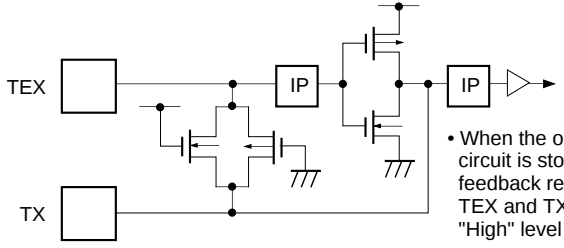
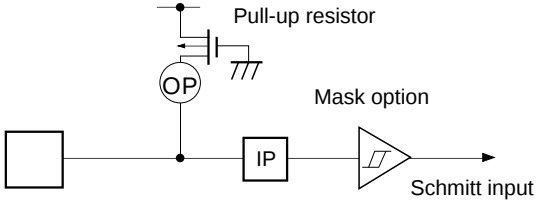
Pin code	I/O	Functions	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/input	(Port I) 8-bit output ports. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs.
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32.768kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V _{DD} .	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		V _{CC} supply.	
V _{SS}		GND	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A Pull-up resistance "0" when reset Port A data Port A direction "0" when reset Data bus RD (Port A) Port A input selection "0" when reset Input multiplexer A/D converter IP Input protection circuit * Pull-up transistors approx. 100kΩ	Hi-Z
PB0/ <u>CS1</u> PB1/ <u>CS0</u> PB3/ <u>SI0</u> PB6/ <u>SI1</u> 4 pins	Port B Pull-up resistance "0" when reset Port B data Port B direction "0" when reset Data bus RD (Port B) CS1 CS0 SI0 SI1 Schmitt input IP * Pull-up transistors approx. 100kΩ	Hi-Z
PB2/ <u>SCK0</u> PB5/ <u>SCK1</u> 2 pins	Port B Pull-up resistance "0" when reset SCK OUT Output enable Port B output selection "0" when reset Port B data Port B direction "0" when reset Data bus RD (Port B) SCK0 in SCK1 Schmitt input IP * Pull-up transistors approx. 100kΩ	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B Pull-up resistance SO Output enable Port B output selection "0" at reset Port B data Port B direction "0" when reset Data bus RD (Port B) * Pull-up transistors approx. 100kΩ	Hi-Z
PC0 to PC7 8 pins	Port C Pull-up resistance "0" when reset Port C data Port C direction "0" when reset Data bus RD (Port C) *1 High current drive of 12mA possible *2 Pull-up transistors approx. 100kΩ	Hi-Z
PE0/ $\overline{\text{EC}}$ PE1 PE2/RMC PE3/NMI 4 pins	Port E Schmitt input Note : PE1 No schmitt input. RD (Port E)	Hi-Z
PE4/ $\overline{\text{PWM}}$ 1 pin	Port E PWM Port E output selection "0" when reset Port E data "1" when reset Data bus RD (Port E)	H level

Pin	Circuit format	When reset
PE5/TO/ADJ 1 pin	Port E RD (Port B)	H level
PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7 36 pins	Port D Port F Port G Port H Port I RD	Hi-Z
PIO/INT0 to PI3/INT3 4 pins	Port I RD INT0 INT1 INT2 INT3	Hi-Z

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed during stop, and XTAL becomes "High".	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX and TX become "Low" level and "High" level respectively.	Oscillation
$\overline{\text{RST}}$ 1 pin	 Pull-up resistor Mask option Schmitt input	Hi-z or L level (When pull-up resistance is added)

Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ¹	V	
High level output current	I _{OH}	−5	mA	Output per pin
High level total output current	ΣI _{OH}	−50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding high current outputs
	I _{OLC}	20	mA	Value per pin* ² for high current outputs
Low level total output current	ΣI _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.*² The high current drive transistor is the N-ch transistor of Port C (PC)

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High speed mode guaranteed operation range* ¹
		3.5	5.5		Low speed mode guaranteed operation range* ¹
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during STOP
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ³
	V _{IHEX}	V _{DD} − 0.4	V _{DD} + 0.3	V	EXTAL* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ³
	V _{ILEX}	−0.3	0.4	V	EXTAL* ⁴
Operating temperature	T _{opr}	−20	+75	°C	

*¹ High speed mode is 1/2 frequency demultiplication clock selection; low-speed mode is 1/16 frequency demultiplication clock selection.*² Value for each pin of normal input ports (PA, PB4, PB7, PC, PD, PE1, PF to PH, PI4 to PI7).*³ Value of the following pins: $\overline{\text{RST}}$, $\overline{\text{CS0}}$, $\overline{\text{CS1}}$, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, SI0, SI1, $\overline{\text{EC}}$, RMC, $\overline{\text{NMI}}$, INT0, INT1, INT2, INT3.*⁴ Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V _{OH}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OH} = -0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = -1.2mA	3.5			V
Low level output current	V _{OL}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{IIE}		V _{DD} = 5.5V, V _{IL} = 0.4V	-0.5		-40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IL} = 5.5V	0.1		10	μA
	I _{ILT}			-0.1		-10	μA
	I _{ILR}	$\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _{IL} = 0.4V	-1.5		-400	μA
	I _{IL}	PA to PD* ² , PF to PI* ²	V _{DD} = 4.5V, V _{IL} = 4.0V	-3.3		-5.0	μA
I/O leakage current	I _{Iz}	PE0 to PE3, $\overline{\text{RST}}^{*1}$, PA to PD* ² , PF to PI* ²	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Power supply current* ³	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency demultiplier clock) V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		18	40	mA
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		35	100	μA
	I _{DDS1}		SLEEP mode V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)		1.1	8	mA
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA
	I _{DDS3}		STOP mode V _{DD} = 5.5V, 10MHz crystal oscillation; and termination of 32kHz oscillation			10	μA
Input capacity	C _{IN}	Pins other than PE4, PE5, XTAL, TX, AV _{REF} , AV _{SS} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*¹ $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*² Pins PA to PD, and PF to PI specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*³ When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f _c	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{\text{EC}}$	Fig. 3	t _{sys} + 50*			ns
Event count input clock rise time, fall time	t _{ER} , t _{EF}	$\overline{\text{EC}}$	Fig. 3			20	ms
System clock frequency	f _c	TEX TX	VDD=2.7 to 5.5V Fig. 2 (32kHz clock application condition)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

* t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

t_{sys} (ns) = 2000/f_c (upper two bits = "00"), 4000/f_c (upper two bits = "01"), 16000/f_c (upper two bits = "11")

Fig. 1. Clock timing

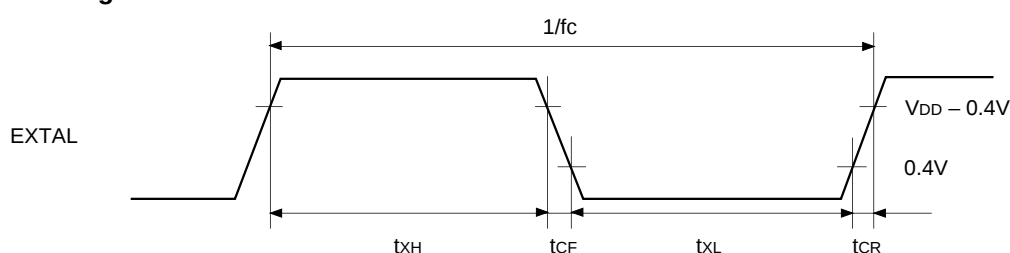


Fig. 2. Clock application conditions

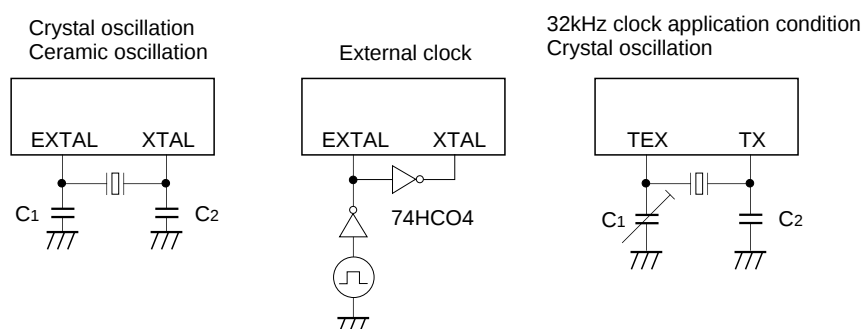
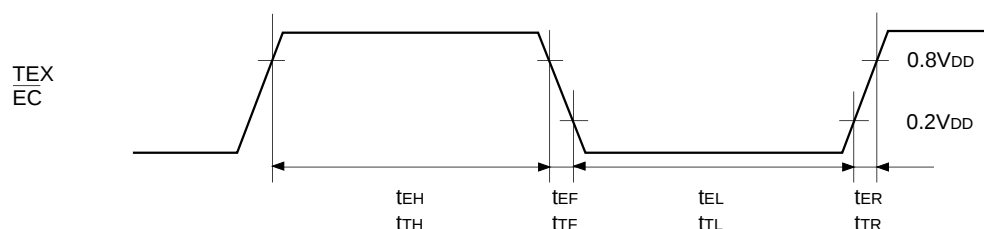


Fig. 3. Event count clock timing



(2) Serial transfer

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS reference)

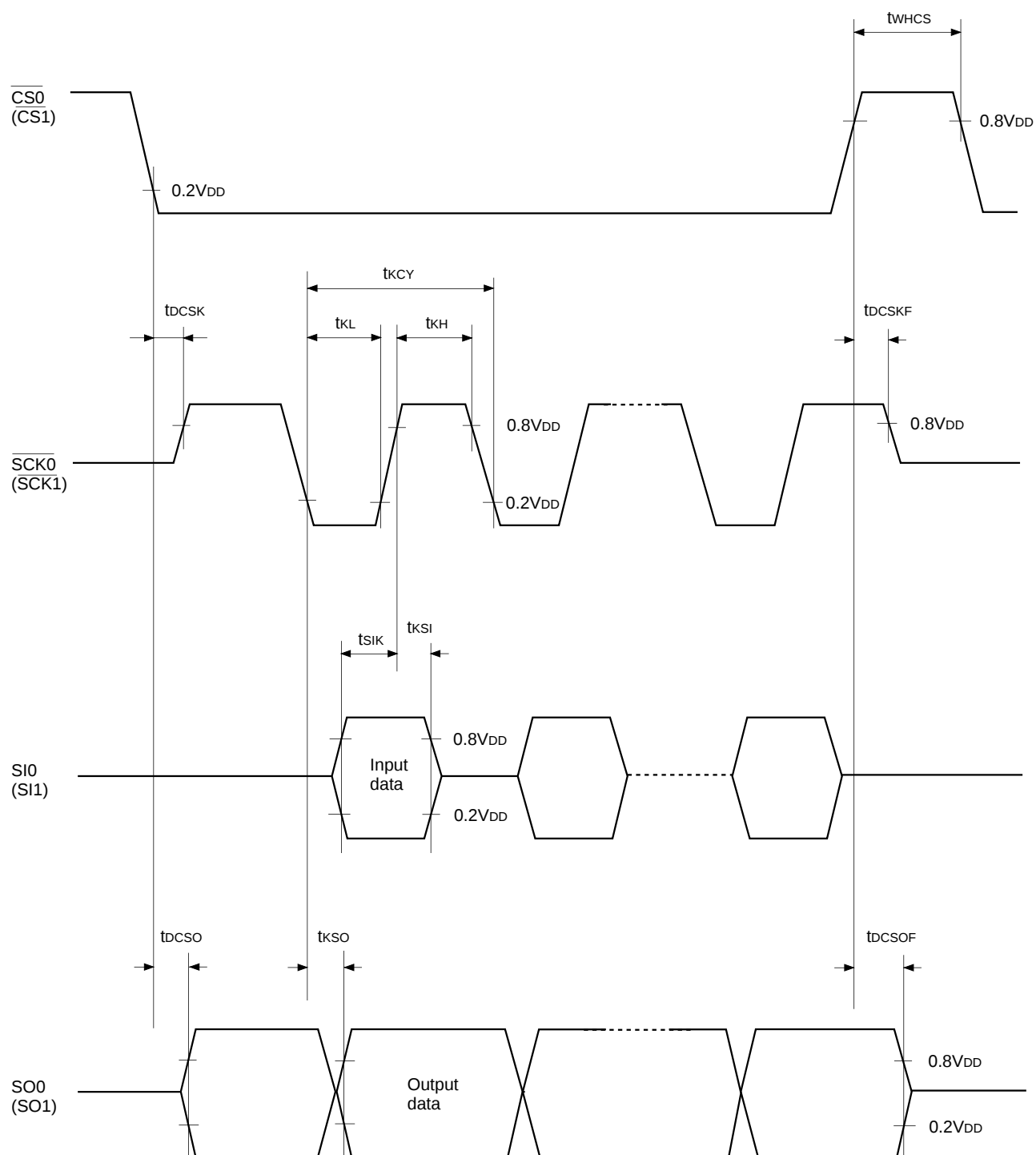
Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \downarrow \rightarrow \overline{SCK1}$) delay time	t_{DCSK}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ ($\overline{CS1} \uparrow \rightarrow \overline{SCK1}$) float delay time	t_{DCSKF}	$\overline{SCK0}$ ($\overline{SCK1}$)	Chip select transfer mode ($\overline{SCK0}$ ($\overline{SCK1}$) = output mode)		$1.5t_{sys} + 200$	ns
$\overline{CS0} \downarrow \rightarrow SO0$ ($\overline{CS1} \downarrow \rightarrow SO1$) delay time	t_{DCSO}	$SO0$ ($SO1$)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0} \uparrow \rightarrow SO0$ ($\overline{CS1} \uparrow \rightarrow SO1$) float delay time	t_{DCSOF}	$SO0$ ($SO1$)	Chip select transfer mode		$1.5t_{sys} + 200$	ns
$\overline{CS0}$ ($\overline{CS1}$) High level width	t_{WHCS}	$\overline{CS0}$ ($\overline{CS1}$)	Chip select transfer mode	$t_{sys} + 200$		ns
$\overline{SCK0}$ ($\overline{SCK1}$) cycle time	t_{KCY}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	$2t_{sys} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{SCK0}$ ($\overline{SCK1}$) High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$ ($\overline{SCK1}$)	Input mode	$t_{sys} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
$SI0$ ($SI1$) input set-up time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t_{SIK}	$SI0$ ($SI1$)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	100		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	200		ns
$SI0$ ($SI1$) input hold time (for $\overline{SCK0} \uparrow$ ($\overline{SCK1} \uparrow$))	t_{KSI}	$SI0$ ($SI1$)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode	$t_{sys} + 200$		ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ ($\overline{SCK1} \downarrow \rightarrow SO1$) delay time	t_{KSO}	$SO0$ ($SO1$)	$\overline{SCK0}$ ($\overline{SCK1}$) input mode		$t_{sys} + 200$	ns
			$\overline{SCK0}$ ($\overline{SCK1}$) output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (address: 00FEH).

t_{sys} (ns) = 2000/ f_c (upper two bits = "00"), 4000/ f_c (upper two bits = "01"), 16000/ f_c (upper two bits = "11")

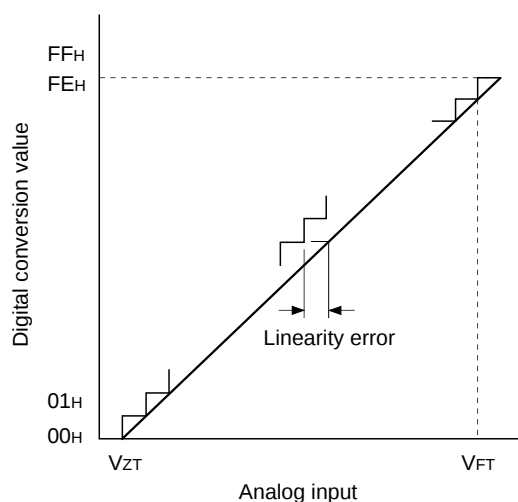
Note 2) The load condition for the $\overline{SCK0}$ ($\overline{SCK1}$) output mode, $SO0$ ($SO1$) output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing



(3) A/D converter characteristics(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V _{DD} = 5.0V V _{SS} = AV _{SS} = 0V			±3	LSB
Zero transition voltage	V _{ZT} *1			-10	30	70	mV
Full-scale transition voltage	V _{FT} *2			4930	4970	5010	mV
Conversion time	t _{CONV}			160/f _{ADC} *3			μs
Sampling time	t _{SAMP}			12/f _{ADC} *3			μs
Reference input voltage	V _{REF}	AV _{REF}		V _{DD} - 0.5		V _{DD}	V
Analog input voltage	V _{IAN}	AN0 to AN7		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode		0.6	1.0	mA
	I _{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 5. Definition of A/D converter terms

*1 V_{ZT} : Value at which the digital transfer value changes from 00H to 01H and vice versa.

*2 V_{FT} : Value at which the digital transfer value changes from FEH to FFH and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of A/D control resistor (address : 00F9H) and bits 6, 7 (PCK0, 1) of clock control resistor (address : 00FFH).

PCK 1, 0	CKS	
	0 (φ/2 selection)	1 (φ selection)
00 (φ = f _{EX} /2)	f _{ADC} = f _C /2	f _{ADC} = f _C
01 (φ = f _{EX} /4)	f _{ADC} = f _C /4	f _{ADC} = f _C /2
11 (φ = f _{EX} /16)	f _{ADC} = f _C /16	f _{ADC} = f _C /8

(4) Interruption, reset input (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{NMI}$		1		μs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		μs

Fig 6. Interruption input timing

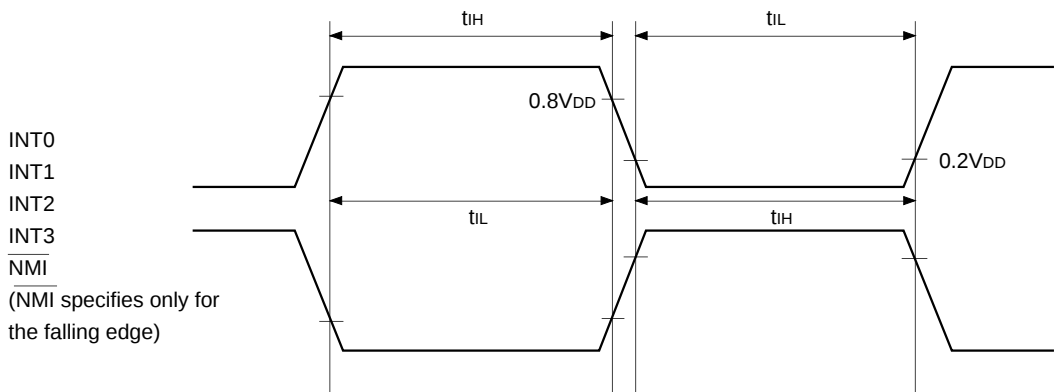
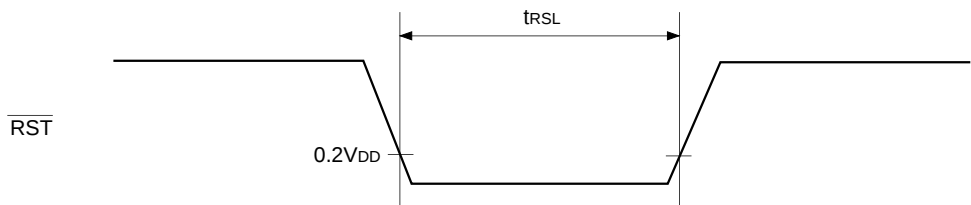


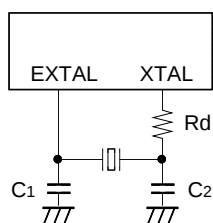
Fig. 7. $\overline{RST}$ input timing



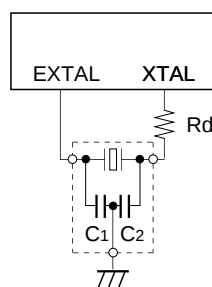
Appendix

Fig. 8. Recommended oscillation circuit

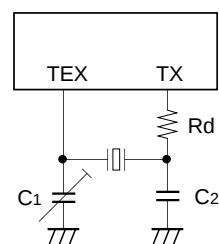
(i) Main clock



(ii) Main clock



(iii) Sub clock



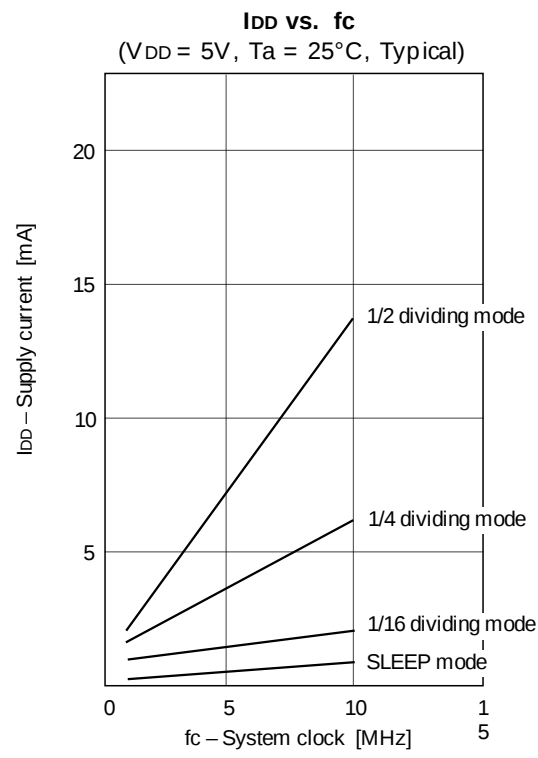
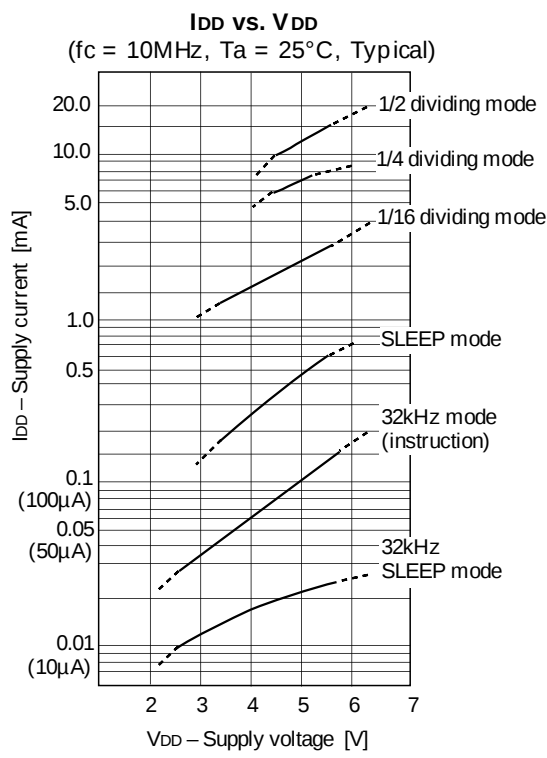
Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Rd (Ω)	Circuit example	
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)	
	CSA8.00MTZ	8.00					
	CSA10.0MTZ	10.00				(ii)	
	CST4.19MGW*	4.19					
	CST8.00MTW*	8.00					
	CST10.0MTW*	10.00					
FUJI SANGYO CO., LTD.	HC-49/U03	4.19	12	12	0	(i)	
		8.00					
		10.00					
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0		(i)
		8.00					
		10.00	20	20			
	P3	32.768kHz	50	22	1M	(iii)	

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

Mask option table

Item	Content	
Reset pin pull-up resistance	No	Yes

Characteristics Curve



Unit: mm

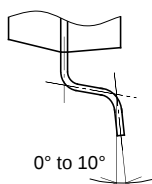
Technical drawing of a rectangular plate with dimensions and tolerances. The drawing includes a top view and a side view.

Top View Dimensions:

- Overall width: 23.9 ± 0.4
- Overall height: 17.9 ± 0.4
- Inner width: $20.0 - 0.1$ with a tolerance of $+0.4$
- Inner height: $14.0 - 0.1$ with a tolerance of $+0.4$
- Left side features: 64, 41, 65, 80
- Right side features: 40, 25
- Bottom side features: 1, 0.8, 24
- Bottom center features: 0.12 (with a circle symbol), $0.35 - 0.1$ with a tolerance of $+0.15$

Side View Dimensions:

- Overall height: 16.3
- Top width: $0.15 - 0.05$ with a tolerance of $+0.1$
- Bottom width: 0.8 ± 0.2
- Bottom center features: $0.1 - 0.05$ with a tolerance of $+0.2$
- Bottom center features: $2.75 - 0.15$ with a tolerance of $+0.35$



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	*QFP080-P-1420-A
JEDEC CODE	_____

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.6g