



CXP84600

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

The CXP84600 is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP84632/84640/84648.

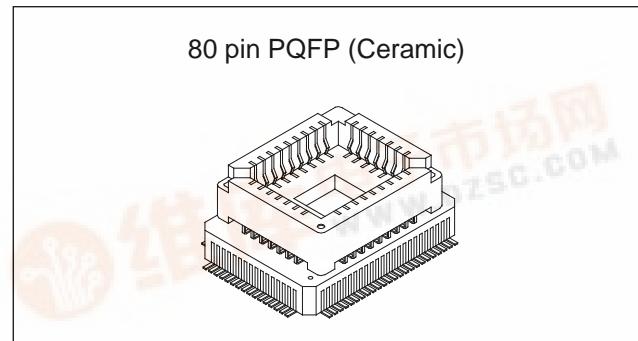
Features

- A wide instruction set (213 instructions) which covers various types of data
 - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 333ns at 12MHz operation (3.0 to 5.5V)
 - 122 μ s at 32kHz operation (2.7 to 5.5V)
- Applicable EPROM
 - LCC type 27C512 (Maximum 60K bytes are available.)
- Incorporated RAM capacity
 - 2048 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time of 20 μ s at 16MHz)
 - Serial interface
 - Start-stop synchronization (UART), 1 channel
 - Incorporated buffer RAM (Auto transfer for 1 to 32 bytes), 1 channel
 - Incorporated 8-bit, 10-stage FIFO (Auto transfer for 1 to 10 bytes), 1 channel
 - 8-bit clock synctype (MSB/LSB first selectable), 1 channel
 - Timer
 - 8-bit timer, 8-bit timer/counter, 19-bit time base timer, 16-bit capture timer/counter, 32kHz timer/counter
 - I²C bus interface
 - Remote control reception circuit
 - PWM output circuit
- Interruption
 - 21 factors, 15 vectors, multi-interruption possible
- Standby mode
 - SLEEP/STOP
- Package
 - 80-pin ceramic PQFP

Note) Mask option depends on the type of the CXP84600. Refer to the Products List for details.

Structure

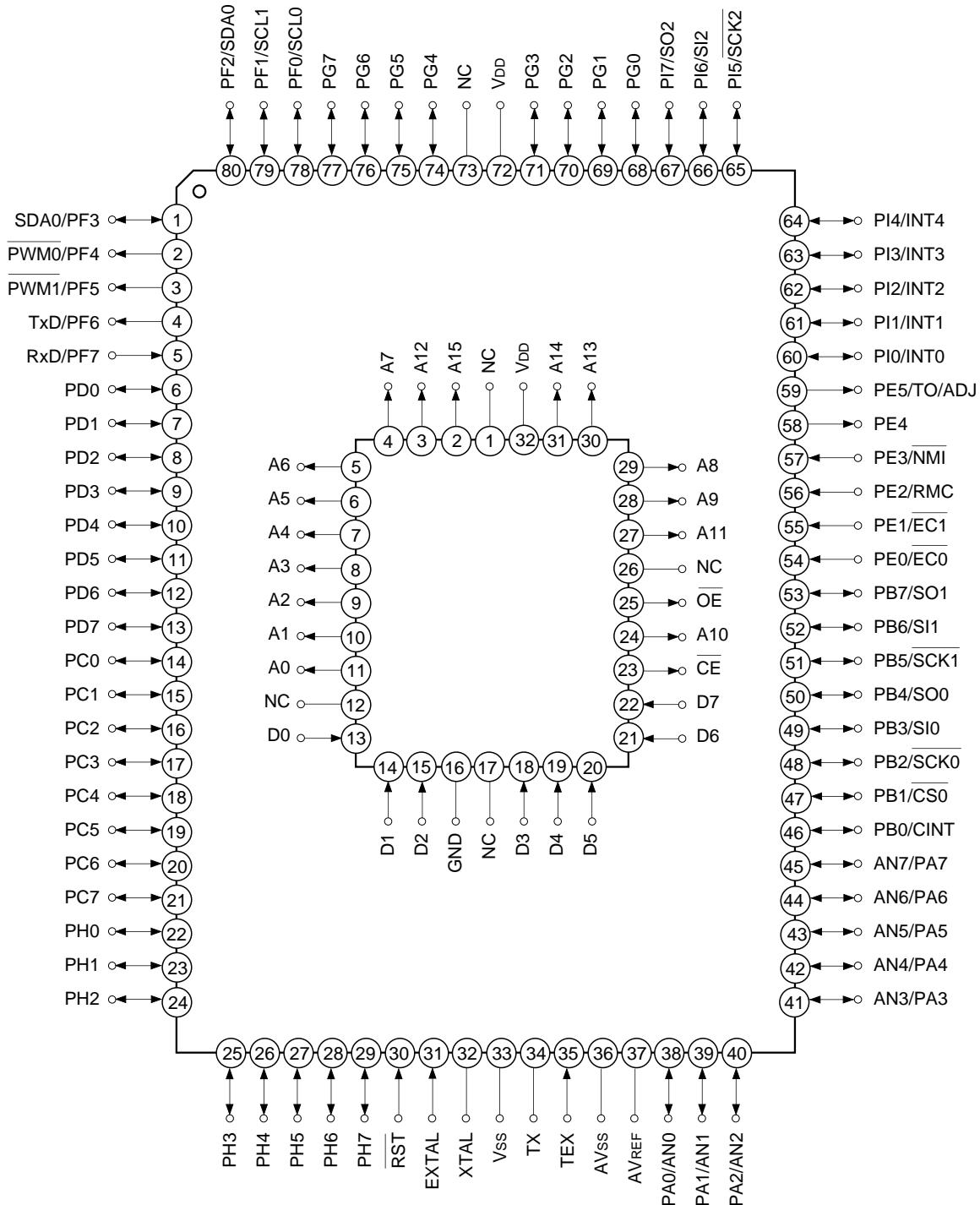
Silicon gate CMOS IC



Perchase of Sony's I²C components conveys a licence under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specifications as defined by Philips.

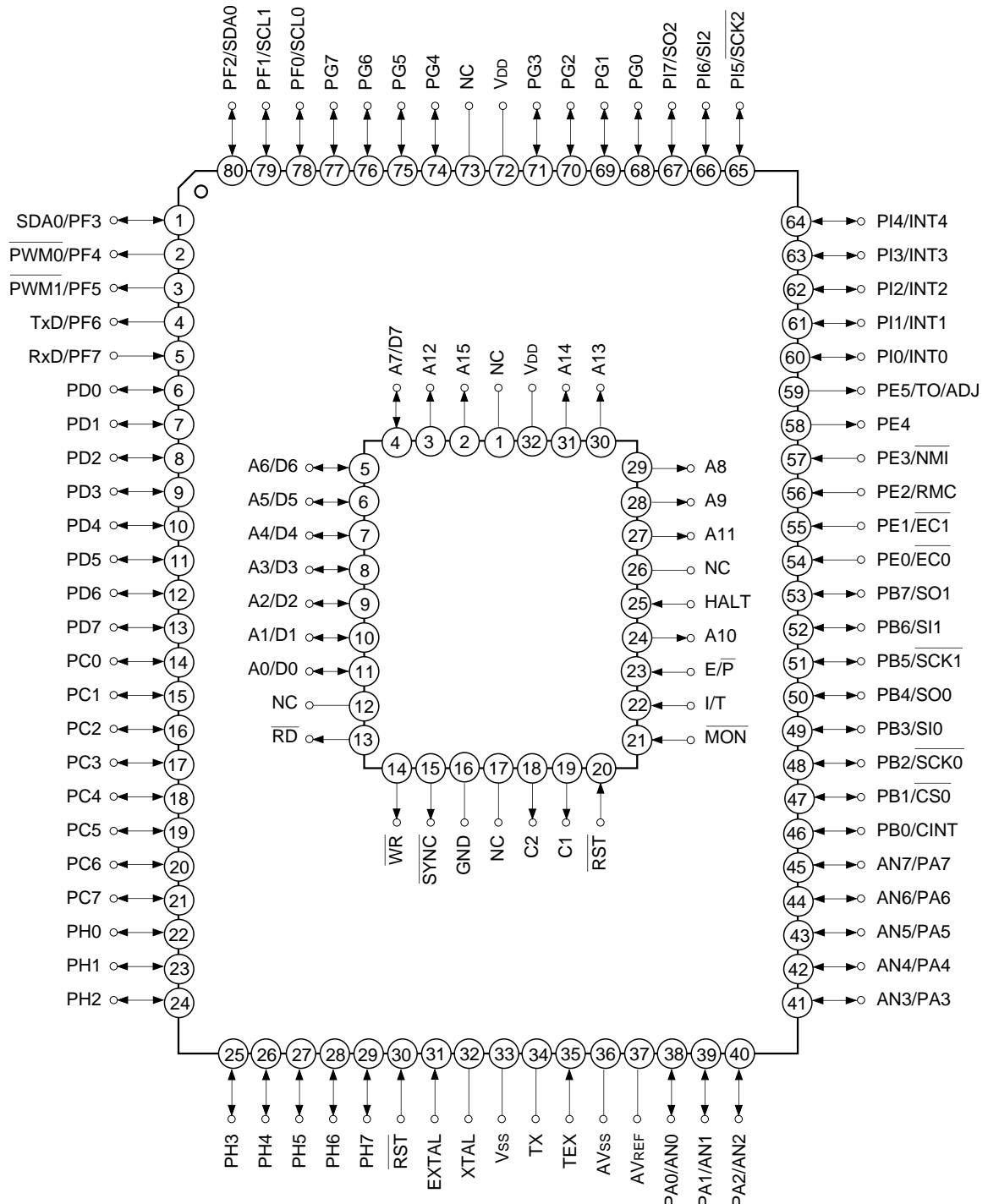
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Pin Assignment in Piggyback Mode



Note) NC (Pin 73) is always connected to V_{DD}.

Pin Assignment in Evaluator Mode



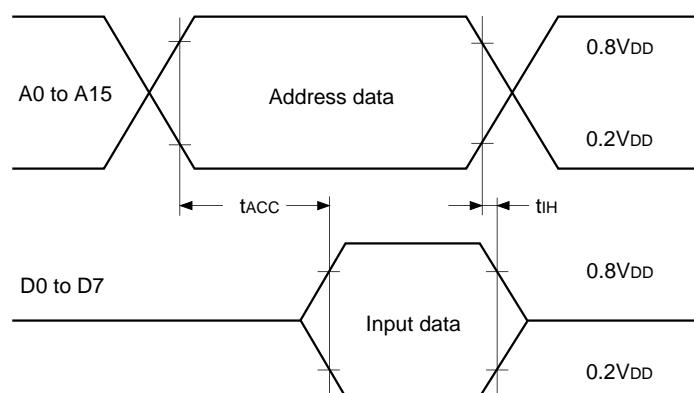
Note) NC (Pin 73) is always connected to VDD.

EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15		100 ^{*1}	ns
		D0 to D7		75 ^{*2}	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

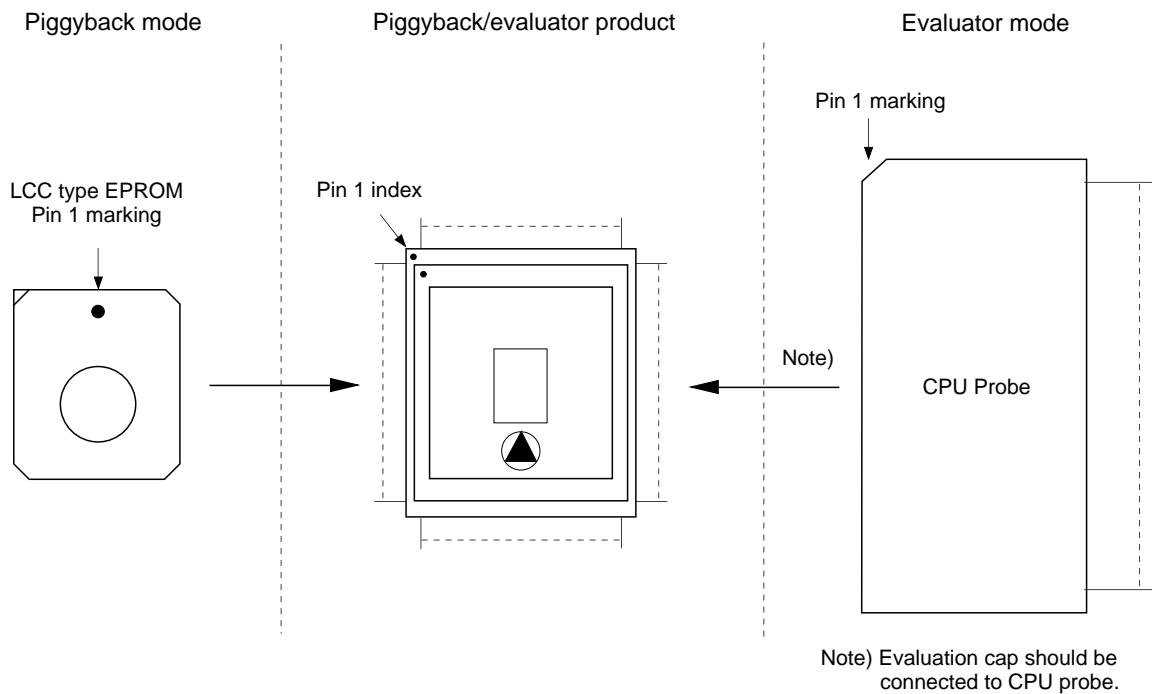
*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

*2 At 12MHz operation ($V_{DD} = 3.0$ to 5.5V), At 16MHz operation ($V_{DD} = 4.5$ to 5.5V)

**Products List**

Option item	Products		
	Mask		Piggyback/evaluator
	CXP84632	CXP84640	CXP84648
Package	80-pin plastic QFP		80-pin ceramic QFP
ROM capacity	32K bytes	40K bytes	48K bytes
Reset pin pull-up resistor	Existent/Non-existent		Existent

Piggyback mode/evaluator mode can be switched as shown below.



Note) Evaluation cap should be connected to CPU probe.

Package Outline

Unit: mm

