

**SONY**

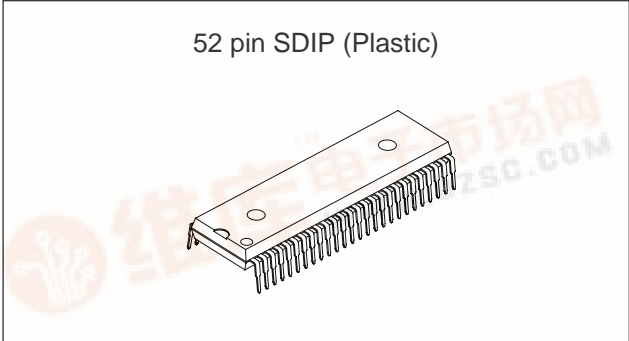
**CXP86213/86217, CXP86325/86333  
CXP86441/86449/86461**

**CMOS 8-bit Single Chip Microcomputer**

**Description**

The CXP86213/86217, CXP86325/86333, CXP86441/86449/86461 are the CMOS 8-bit single chip micro-computer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, on-screen display function, I<sup>2</sup>C bus interface, PWM output, remote control reception circuit, HSYNC counter, watchdog timer, 32kHz timer/counter besides the basic configurations of 8-bit CPU, ROM, RAM, I/O ports.

The CXP86213/86217, CXP86325/86333, CXP86441/86449/86461 also provide a sleep function that enables to lower the power consumption.



**Features**

- A wide instruction set (213 instructions) which covers various types of data
  - 16-bit operation/multiplication and division/ Boolean bit operation instructions
- Minimum instruction cycle 250ns at 16MHz operation (4.5 to 5.5V)  
122µs at 32kHz operation (2.7 to 5.5V)
- Incorporated ROM capacity 12K bytes (CXP86213) 24K bytes (CXP86325) 40K bytes(CXP86441)  
16K bytes (CXP86217) 32K bytes (CXP86333) 48K bytes (CXP86449)  
60K bytes (CXP86461)
- Incorporated RAM capacity 352 bytes (CXP86213/86217) 704 bytes (CXP86325/86333)  
1536 bytes (CXP86441/86449/86461)  
(Excludes VRAM for on-screen display and sprite RAM)
- Peripheral functions
  - A/D converter
  - Serial interface
  - Timer

**Structure**

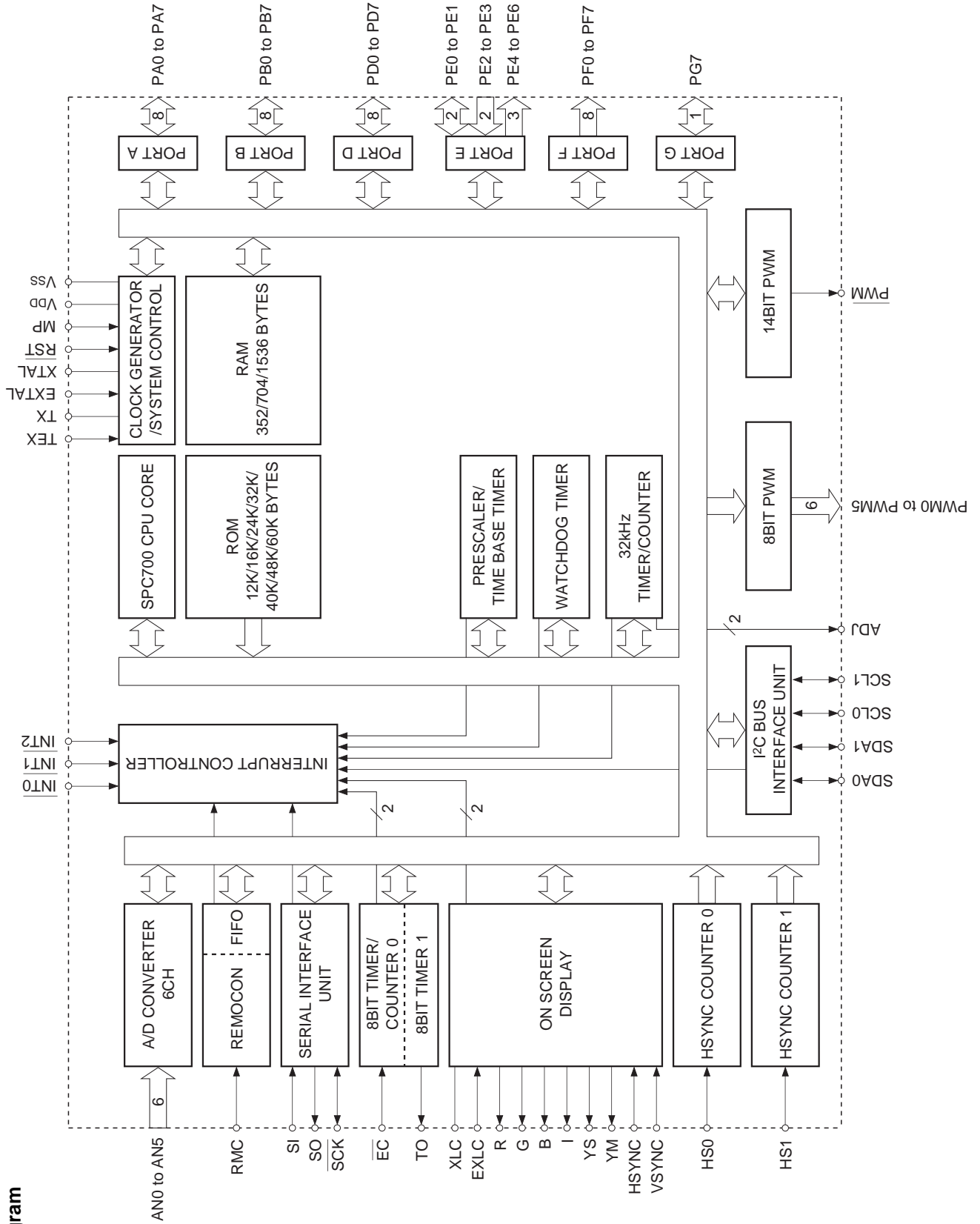
Silicon gate CMOS IC

- On-screen display (OSD) function 12 × 16 dots, 128 character types (CXP86213/86217),  
256 character types (CXP86325/86333),  
384 character types (CXP86441/86449/86461)  
15 character colors, 2 lines × 24 characters,  
frame background 8 colors/ half blanking,  
background on full screen 15 colors/ half blanking  
edging/ shadowing/ rounding for every line,  
background with shadow for every character (CXP86441/86449/86461),  
double scanning,  
sprite OSD (CXP86441/86449/86461),  
12 × 16 dots, 1 screen, 8 colors for every dot
- I<sup>2</sup>C bus interface
- PWM output
- Remote control reception circuit
- HSYNC counter
- Watchdog timer
- Interruption 13 factors, 13 vectors, multi-interruption possible
- Standby mode Sleep
- Package 52-pin plastic SDIP
- Piggyback/evaluator CXP86490 64-pin ceramic PSDIP (Supports custom font)

Purchase of Sony's I<sup>2</sup>C components conveys a licence under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

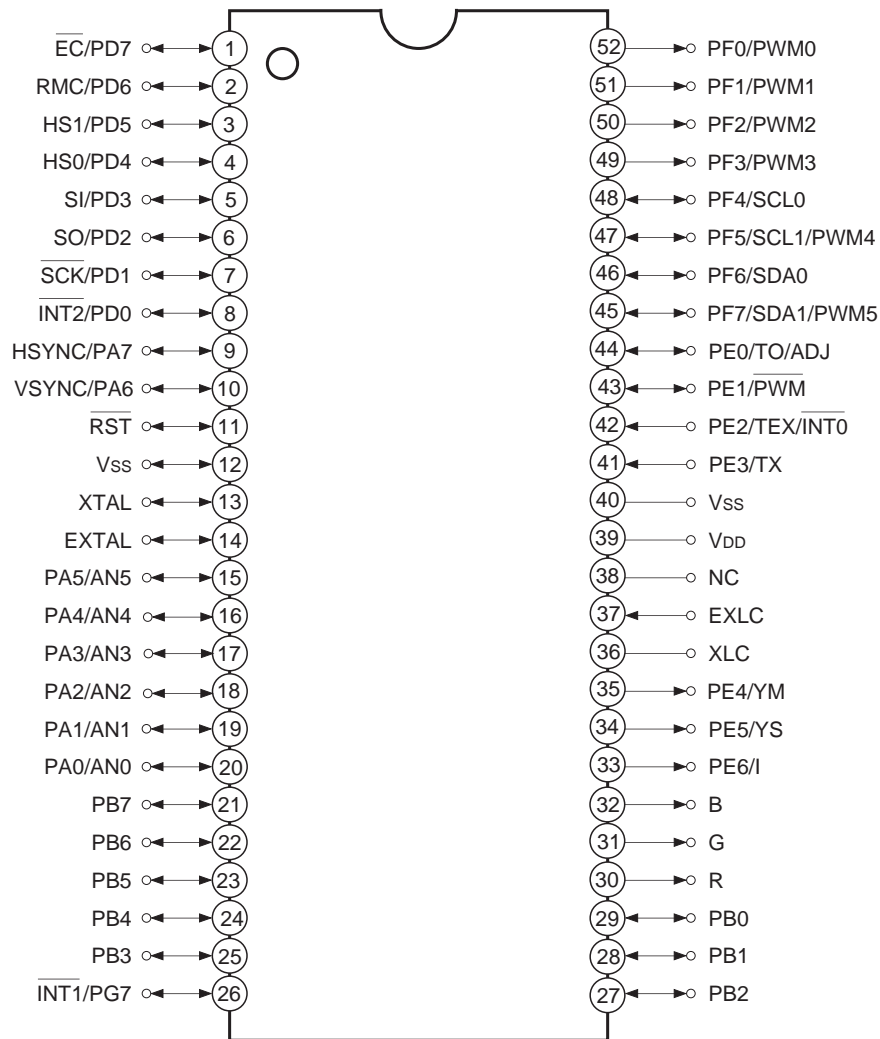


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Block Diagram

Pin Assignment (Top View)



**Note)**

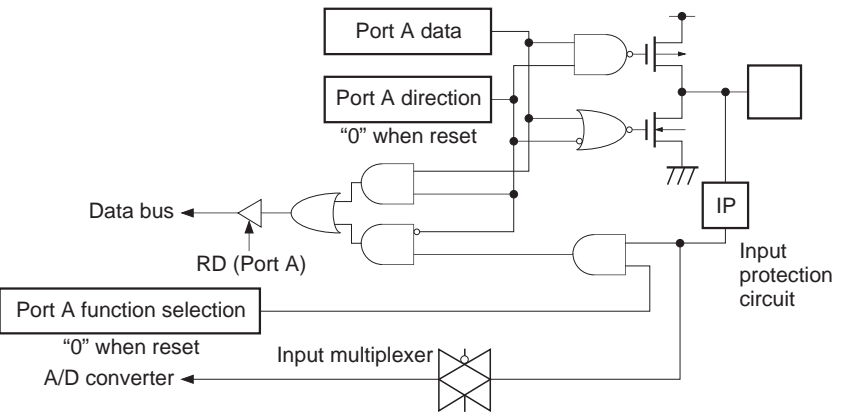
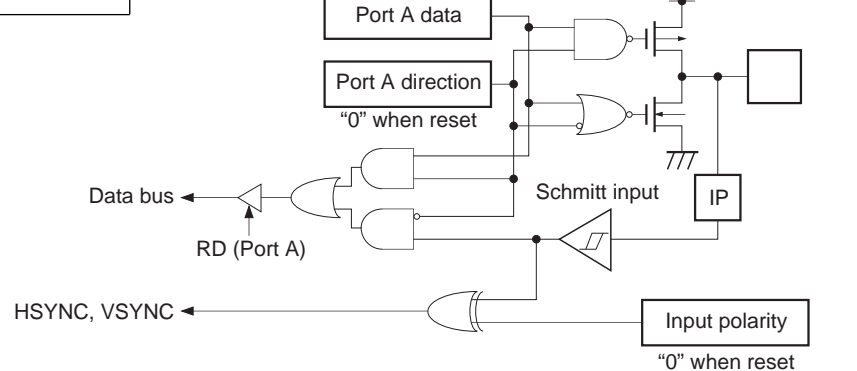
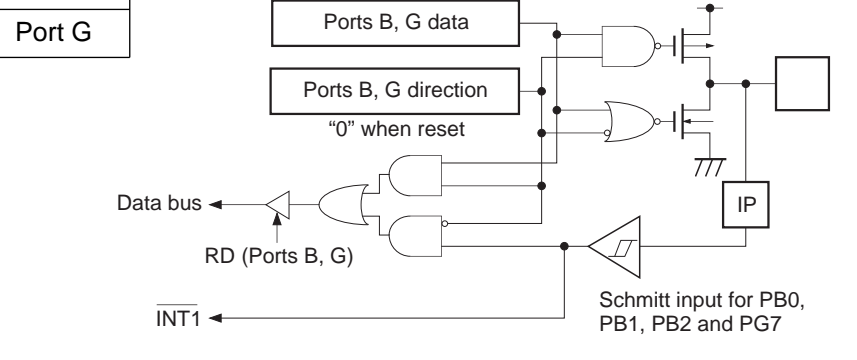
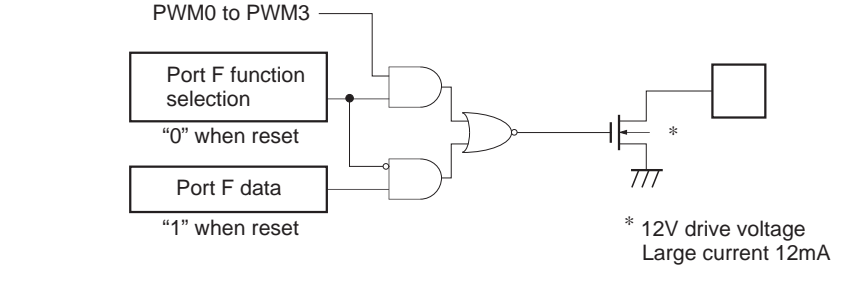
1. NC (Pin 38) is left open.
2. Vss (Pins 12 and 40) are both connected to GND.

Pin Description

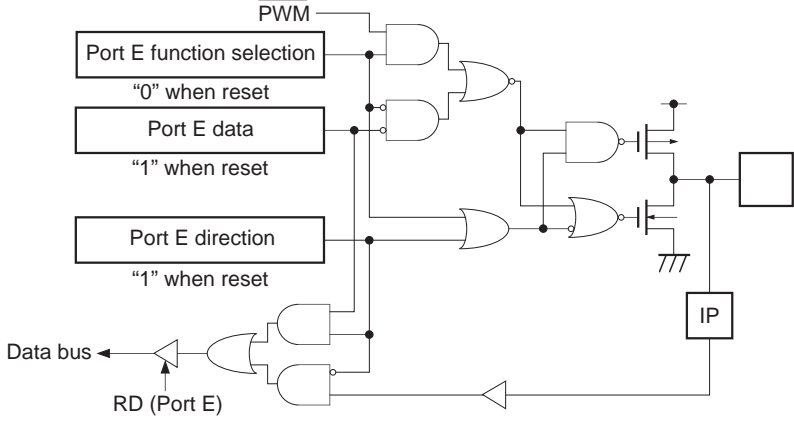
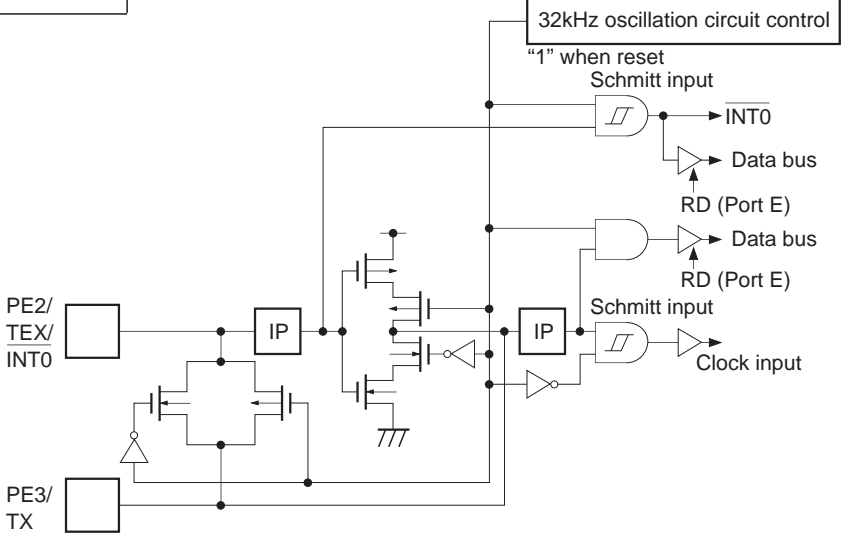
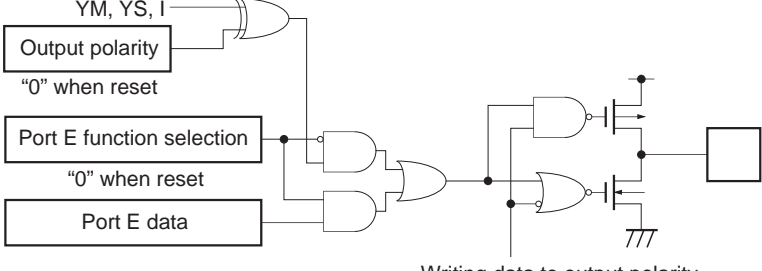
| Symbol                            | I/O                   | Description  |  |  |
|-----------------------------------|-----------------------|--|--|--|
| PA0/AN0<br>to<br>PA5/AN5          | I/O/<br>Analog input  | (Port A)<br>8-bit I/O port.<br>I/O can be set in a<br>unit of single bits.<br>(8 pins)   | Analog inputs to A/D converter.<br>(6 pins)  |  |
| PA6/VSYNC                         | I/O/Input             |  | OSD display vertical sync signal input.  |  |
| PA7/HSYNC                         | I/O/Input             |  | OSD display horizontal sync signal input.  |  |
| PB0 to PB7                        | I/O                   | (Port B)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>(8 pins)   |  |  |
| PD0/ $\overline{\text{INT2}}$     | I/O/Input             | (Port D)<br>8-bit I/O port. I/O<br>can be set in a<br>unit of single bits.<br>Can drive 12mA<br>synk current.<br>(8 pins)  | External interruption request input. Active at the<br>falling edge.  |  |
| PD1/ $\overline{\text{SCK}}$      | I/O/I/O               |  | Serial clock I/O.  |  |
| PD2/SO                            | I/O/Output            |  | Serial data output.  |  |
| PD3/SI                            | I/O/Input             |  | Serial data input.   |  |
| PD4/HS0                           | I/O/Input             |  | HSYNC counter (CH0) input.   |  |
| PD5/HS1                           | I/O/Input             |  | HSYNC counter (CH1) input.   |  |
| PD6/RMC                           | I/O/Input             |  | Remote control reception circuit input.  |  |
| PD7/ $\overline{\text{EC}}$       | I/O/Input             |  | External event input for timer/counter.  |  |
| PE0/TO/ADJ                        | I/O/Output/<br>Output | (Port E)<br>Bits 0 and 1 are I/O<br>port; I/O can be set<br>in a unit of single.<br>Bits 2 and 3 are<br>input port. Bits 4, 5<br>and 6 are output<br>port.<br>(7 pins) | Rectangular wave output<br>for 8-bit timer/counter. 32kHz oscillation<br>frequency dividing output.  |  |
| PE1/PWM                           | I/O/Output            |  | 14-bit PWM output.   |  |
| PE2/TEX/ $\overline{\text{INT0}}$ | Input/Input/<br>Input |  | Connects a crystal for<br>32kHz timer/counter<br>clock oscillation. When<br>used as an event<br>counter, input to TEX pin and leave TX pin open. | External interruption<br>request input. Active at<br>the falling edge. |
| PE3/TX                            | Input/Output          |  |  |  |
| PE4/YM                            | Output/Output         |  |  |  |
| PE5/YS                            | Output/Output         |  |  |  |
| PE6/I                             | Output/Output         |  |  | OSD display 6-bit output.<br>(6 pins)                                  |
| B                                 | Output                |  |  |  |
| G                                 | Output                |  |  |  |
| R                                 | Output                |  |  |  |

| Symbol                        | I/O               | Description  |  |   |
|-------------------------------|-------------------|--|--|---|
| PF0/PWM0 to PF3/PWM3          | Output/Output     | (Port F)<br>8-bit output port.   | 8-bit PWM output.<br>(4 pins)                                  |   |
| PF4/SCL0                      | Output/I/O        | Open drain output of large current (12mA) and N channel. Lower 4 bits are medium drive voltage (12V); upper 4 bits are 5V drive.<br>(8 pins)           | I <sup>2</sup> C bus interface transfer clock I/O.<br>(2 pins) |   |
| PF5/SCL1/PWM4                 | Output/I/O/Output |  |  | 8-bit PWM output.   |
| PF6/SDA0                      | Output/I/O        |  | I <sup>2</sup> C bus interface transfer data I/O.<br>(2 pins)  | 8-bit PWM output.   |
| PF7/SDA1/PWM5                 | Output/I/O/Output |  |  |   |
| PG7/ $\overline{\text{INT1}}$ | I/O/Input         |  | (Port G)<br>1-bit I/O port.                                    | External interruption request input.<br>Active at the falling edge. |
| EXTAL                         | Input             | Connects a crystal for system clock oscillation. When a clock is supplied externally, input to EXTAL pin and input a reversed phase clock to XTAL pin. |  |   |
| XTAL                          | Output            |  |  |   |
| $\overline{\text{RST}}$       | Input             | System reset; active at Low level.   |  |   |
| EXLC                          | Input             | OSD display clock oscillation I/O. Oscillation frequency is determined by the external L and C.  |  |   |
| XLC                           | Output            |  |  |   |
| NC                            |                   | No connected.  |  |   |
| V <sub>DD</sub>               |                   | Positive power supply.   |  |   |
| V <sub>SS</sub>               |                   | GND. Connect two V <sub>SS</sub> pins to GND.  |  |   |

Input/Output Circuit Formats for Pins

| Pin                                       | Circuit format  | When reset  |
|---|---|-------------|
| <p>PA0/AN0 to PA5/AN5</p> <p>6 pins</p>   | <p>Port A</p>  <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>Port A function selection "0" when reset</p> <p>A/D converter</p> <p>Input multiplexer</p> <p>Input protection circuit</p> <p>IP</p> | <p>Hi-Z</p> |
| <p>PA6/VSYNC PA7/HSYNC</p> <p>2 pins</p>  | <p>Port A</p>  <p>Port A data</p> <p>Port A direction "0" when reset</p> <p>Data bus</p> <p>RD (Port A)</p> <p>HSYNC, VSYNC</p> <p>Schmitt input</p> <p>Input polarity "0" when reset</p> <p>Input protection circuit</p> <p>IP</p>                | <p>Hi-Z</p> |
| <p>PB0 to PB7 PG7/INT1</p> <p>9 pins</p>  | <p>Port B</p> <p>Port G</p>  <p>Ports B, G data</p> <p>Ports B, G direction "0" when reset</p> <p>Data bus</p> <p>RD (Ports B, G)</p> <p>INT1</p> <p>Schmitt input for PB0, PB1, PB2 and PG7</p> <p>Input protection circuit</p> <p>IP</p>        | <p>Hi-Z</p> |
| <p>PF0/PWM0 to PF3/PWM3</p> <p>4 pins</p> | <p>Port F</p>  <p>PWM0 to PWM3</p> <p>Port F function selection "0" when reset</p> <p>Port F data "1" when reset</p> <p>* 12V drive voltage<br/>Large current 12mA</p> <p>Input protection circuit</p> <p>IP</p>                                  | <p>Hi-Z</p> |

| Pin  | Circuit format   | When reset  |
|--|--|---|
| <p>Port D</p> <p>PD0/<math>\overline{\text{INT2}}</math><br/>           PD3/SI<br/>           PD4/HS0<br/>           PD5/HS1<br/>           PD6/RMC<br/>           PD7/<math>\overline{\text{EC}}</math></p> <p>6 pins</p> | <p>Port D data</p> <p>Port D direction<br/>"0" when reset</p> <p>Data bus</p> <p>RD (Port D)</p> <p><math>\overline{\text{INT2}}</math>, SI, HS0, HS1, RMC, <math>\overline{\text{EC}}</math></p> <p>Schmitt input</p> <p>IP</p> <p>* Large current 12mA</p>   | <p>Hi-Z</p>   |
| <p>Port D</p> <p>PD1/<math>\overline{\text{SCK}}</math><br/>           PD2/SO</p> <p>2 pins</p>  | <p>SCK, SO</p> <p>SIO output enable</p> <p>Port D data</p> <p>Port D direction<br/>"0" when reset</p> <p>Data bus</p> <p>RD (Port D)</p> <p>Schmitt input only for PD1</p> <p>IP</p> <p>* Large current 12mA</p> <p>SCK only</p>   | <p>Hi-Z</p>   |
| <p>Port E</p> <p>PE0/TO/ADJ</p> <p>1 pin</p>   | <p>Internal reset signal</p> <p>Port E data<br/>"1" when reset</p> <p>TO</p> <p>ADJ16K*<sup>1</sup></p> <p>ADJ2K*<sup>1</sup></p> <p>MPX</p> <p>Port E function selection (Upper)</p> <p>Port E function selection (Lower)</p> <p>Port E direction<br/>"1" when reset</p> <p>Data bus</p> <p>RD (Port E)</p> <p>*<sup>1</sup> ADJ signals are frequency dividing outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.</p> <p>*<sup>2</sup> Pull-up resistors approx. 150k<math>\Omega</math></p> | <p>High level<br/>(with the resistor of pull-up transistor ON when reset)</p> |

| Pin   | Circuit format   | When reset                               |
|---|--|--|
| <p>PE1/PWM</p> <p>1 pin</p>   | <p>Port E</p>    | <p>High level</p>                        |
| <p>PE2/TEX/<math>\overline{\text{INT0}}</math><br/>PE3/TX</p> <p>2 pins</p> | <p>Port E</p>   | <p>Oscillation halted<br/>Port input</p> |
| <p>PE4/YM<br/>PE5/YS<br/>PE6/I</p> <p>3 pins</p>                            | <p>Port E</p>  <p>Writing data to output polarity register and port data register brings output to active.</p> | <p>Hi-Z</p>                              |



| Pin  | Circuit format   | When reset                |
|--|--|---------------------------|
| <p>PF4/SCL0<br/>PF5/SCL1/PWM4<br/>PF6/SDA0<br/>PF7/SDA1/PWM5</p> <p>4 pins</p> | <p>Port F</p> <p>SCL, SDA</p> <p>I2C bus enable</p> <p>PWM4, PWM5</p> <p>Port F function selection<br/>"0" when reset</p> <p>Port F data<br/>"1" when reset</p> <p>Schmitt input</p> <p>SCL, SDA<br/>(I2C bus circuit)</p> <p>* Large current 12mA</p> <p>To internal I2C pins<br/>(SCL1 for SCL0)</p> <p>BUS SW</p> | <p>Hi-Z</p>               |
| <p>R<br/>G<br/>B</p> <p>3 pins</p>   | <p>R, G, B</p> <p>Output polarity<br/>"0" when reset</p> <p>Writing data to output polarity register brings output to active.</p>  | <p>Hi-Z</p>               |
| <p>EXLC<br/>XLC</p> <p>2 pins</p>  | <p>Oscillation control</p> <p>EXLC</p> <p>XLC</p> <p>OSD display clock</p>   | <p>Oscillation halted</p> |
| <p>EXTAL<br/>XTAL</p> <p>2 pins</p>  | <p>EXTAL</p> <p>XTAL</p> <ul style="list-style-type: none"> <li>• Diagram shows the circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop mode. (This device does not enter the stop mode.)</li> </ul>   | <p>Oscillation</p>        |
| <p>RST</p> <p>1 pin</p>  | <p>Pull-up resistor</p> <p>Mask option</p> <p>Schmitt input</p>  | <p>Low level</p>          |

**Absolute Maximum Ratings**

(V<sub>SS</sub> = 0V reference)

| Item                            | Symbol            | Ratings                    | Unit | Remarks   |
|---------------------------------|-------------------|----------------------------|------|---|
| Supply voltage                  | V <sub>DD</sub>   | -0.3 to +7.0               | V    |   |
| Input voltage                   | V <sub>IN</sub>   | -0.3 to +7.0* <sup>1</sup> | V    |   |
| Output voltage                  | V <sub>OUT</sub>  | -0.3 to +7.0* <sup>1</sup> | V    |   |
| Medium drive output voltage     | V <sub>OUTP</sub> | -0.3 to +15.0              | V    |   |
| High level output current       | I <sub>OH</sub>   | -5                         | mA   |   |
| High level total output current | ∑I <sub>OH</sub>  | -50                        | mA   | Total of all output pins                                  |
| Low level output current        | I <sub>OL</sub>   | 15                         | mA   | Ports excluding large current output (value per pin)      |
|                                 | I <sub>OLC</sub>  | 20                         | mA   | Large current output ports (value per pin* <sup>2</sup> ) |
| Low level total output current  | ∑I <sub>OL</sub>  | 130                        | mA   | Total of all output pins                                  |
| Operating temperature           | T <sub>opr</sub>  | -20 to +75                 | °C   |   |
| Storage temperature             | T <sub>stg</sub>  | -55 to +150                | °C   |   |
| Allowable power dissipation     | P <sub>D</sub>    | 375                        | mW   | 52-pin SDIP   |

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> should not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The large current output port is Port D (PD) and Port F (PF).

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

**Recommended Operating Conditions**

(V<sub>SS</sub> = 0V reference)

| Item                     | Symbol            | Min.                  | Max.                  | Unit | Remarks   |
|--------------------------|-------------------|-----------------------|-----------------------|------|---|
| Supply voltage           | V <sub>DD</sub>   | 4.5                   | 5.5                   | V    | Guaranteed operation range for 1/2 and 1/4 frequency dividing modes       |
|                          |                   | 3.5                   | 5.5                   | V    | Guaranteed operation range for 1/16 frequency dividing mode or sleep mode |
|                          |                   | 2.7                   | 5.5                   | V    | Guaranteed operation range for TEX mode                                   |
|                          |                   | —                     | —                     | V    | Guaranteed data hold range for stop mode* <sup>5</sup>                    |
| High level input voltage | V <sub>IH</sub>   | 0.7V <sub>DD</sub>    | V <sub>DD</sub>       | V    | * <sup>1</sup>  |
|                          | V <sub>IHS</sub>  | 0.8V <sub>DD</sub>    | V <sub>DD</sub>       | V    | * <sup>2</sup>  |
|                          | V <sub>IHEX</sub> | V <sub>DD</sub> - 0.4 | V <sub>DD</sub> + 0.3 | V    | EXTAL pin* <sup>3</sup> , TEX pin* <sup>4</sup>                           |
| Low level input voltage  | V <sub>IL</sub>   | 0                     | 0.3V <sub>DD</sub>    | V    | * <sup>1</sup>  |
|                          | V <sub>ILS</sub>  | 0                     | 0.2V <sub>DD</sub>    | V    | * <sup>2</sup>  |
|                          | V <sub>ILEX</sub> | -0.3                  | 0.4                   | V    | EXTAL pin* <sup>3</sup> , TEX pin* <sup>4</sup>                           |
| Operating temperature    | T <sub>opr</sub>  | -20                   | +75                   | °C   |   |

\*<sup>1</sup> PA1 to 5, PB3 to 7, PD2, PE0, PE1, PE3, SCL0 to 1, SDA0 to 1 pins

\*<sup>2</sup> V<sub>SYNC</sub>, H<sub>SYNC</sub>, INT2, SCK, SI, HS0, HS1, RMC, EC, INT0, INT1, RST, PB0, PB1, PB2 pins

\*<sup>3</sup> Specifies only during external clock input.

\*<sup>4</sup> Specifies only during external event count input.

\*<sup>5</sup> This device does not enter the stop mode.

Electrical Characteristics

DC characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

| Item  | Symbol            | Pins   | Conditions  | Min.   | Typ. | Max. | Unit |
|---|-------------------|--|---|--|------|------|------|
| High level output voltage   | V <sub>OH</sub>   | PA, PB, PD, PE0 to PE1, PE4 to PE6, PG7, R, G, B             | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA  | 4.0  |      |      | V    |
|   |                   |  | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA  | 3.5  |      |      | V    |
| Low level output voltage  | V <sub>OL</sub>   | PA, PB, PD, PE0 to PE1, PE4 to PE6, PF0 to PF3, PG7, R, G, B | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA   |  |      | 0.4  | V    |
|   |                   |  | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA   |  |      | 0.6  | V    |
|   |                   | PD, PF   | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA  |  |      | 1.5  | V    |
|   |                   | PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)                          | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.0mA   |  |      | 0.4  | V    |
|   |                   |  | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 4.0mA   |  |      | 0.6  | V    |
| Input current   | I <sub>IHE</sub>  | EXTAL  | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V  | 0.5  |      | 40   | μA   |
|   | I <sub>ILE</sub>  |  |   | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V | -0.5 |      | -40  |
|   | I <sub>IHT</sub>  | TEX  | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V  | 0.1  |      | 10   | μA   |
|   | I <sub>ILT</sub>  |  |   | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V | -0.1 |      | -10  |
|   | I <sub>ILR</sub>  | RST*1  | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V  | -1.5   |      | -400 | μA   |
| I/O leakage current   | I <sub>Iz</sub>   | PA, PB, PD, PE, R, G, B, RST*1                               | V <sub>DD</sub> = 5.5V, V <sub>I</sub> = 0, 5.5V  |  |      | ±10  | μA   |
| Open drain I/O leakage current (in N-ch Tr off state)                     | I <sub>LOH</sub>  | PF0 to PF3   | V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 12.0V   |  |      | 50   | μA   |
|   |                   | PF4 to PF7   | V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 5.5V  |  |      | 10   | μA   |
| I <sup>2</sup> C bus switch connection impedance (in output Tr off state) | R <sub>BS</sub>   | SCL0: SCL1<br>SDA0: SDA1                                     | V <sub>DD</sub> = 4.5V<br>V <sub>SCL0</sub> = V <sub>SCL1</sub> = 2.25V<br>V <sub>SDA0</sub> = V <sub>SDA1</sub> = 2.25V        |  |      | 120  | Ω    |
| Supply current*2  | I <sub>DD1</sub>  | V <sub>DD</sub>  | 1/2 frequency dividing mode<br>V <sub>DD</sub> = 5.5V,<br>16MHz crystal oscillation<br>(C <sub>1</sub> = C <sub>2</sub> = 15pF) |  | 18   | 28   | mA   |
|   | I <sub>DD2</sub>  |  | V <sub>DD</sub> = 3.3V,<br>32MHz crystal oscillation<br>(C <sub>1</sub> = C <sub>2</sub> = 47pF)                                |  | 30   | 80   | μA   |
|   | I <sub>DDS1</sub> |  | SLEEP mode<br>V <sub>DD</sub> = 5.5V,<br>16MHz crystal oscillation<br>(C <sub>1</sub> = C <sub>2</sub> = 15pF)                  |  | 1.2  | 2.1  | mA   |
|   |                   |  | V <sub>DD</sub> = 3.3V,<br>32MHz crystal oscillation<br>(C <sub>1</sub> = C <sub>2</sub> = 47pF)                                |  | 12   | 35   | μA   |
|   | I <sub>DDS3</sub> |  | STOP mode*3<br>V <sub>DD</sub> = 5.5V,<br>termination of 16MHz<br>and 32MHz oscillation   |  | —    | —    | —    |

| Item              | Symbol          | Pins   | Conditions                                    | Min. | Typ. | Max. | Unit |
|-------------------|-----------------|--|---|------|------|------|------|
| Input capacitance | C <sub>IN</sub> | PA, PB, PD, PE0 to PE3, R, G, B, PF4 to PF7, EXTAL, TEX, EXLC, $\overline{\text{RST}}$ | Clock 1MHz<br>0V other than the measured pins |      | 10   | 20   | pF   |

\*1 For  $\overline{\text{RST}}$  pin, specifies the input current when pull-up resistance is selected, and specifies the leakage current when non-resistor is selected.

\*2 When all output pins are left open. Specifies only when the OSD oscillation is halted.

\*3 This device does not enter the stop mode.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

| Item  | Symbol                               | Pins            | Conditions   | Min.                 | Typ.   | Max | Unit |
|---|--------------------------------------|-----------------|--|----------------------|--------|-----|------|
| System clock frequency                      | fc                                   | XTAL<br>EXTAL   | Fig. 1, Fig. 2   | 8                    |        | 16  | MHz  |
| System clock input pulse width              | t <sub>XL</sub> ,<br>t <sub>XH</sub> | EXTAL           | Fig. 1, Fig. 2<br>External clock drive                                   | 28                   |        |     | ns   |
| System clock input rise and fall times      | t <sub>CR</sub> ,<br>t <sub>CF</sub> | EXTAL           | Fig. 1, Fig. 2<br>External clock drive                                   |                      |        | 200 | ns   |
| Event count input clock pulse width         | t <sub>EH</sub> ,<br>t <sub>EL</sub> | $\overline{EC}$ | Fig. 3   | 4t <sub>sys</sub> *1 |        |     | ns   |
| Event count input clock rise and fall times | t <sub>ER</sub> ,<br>t <sub>EF</sub> | $\overline{EC}$ | Fig. 3   |                      |        | 20  | ms   |
| System clock frequency                      | fc                                   | TEX<br>TX       | V <sub>DD</sub> = 2.7 to 5.5V<br>Fig. 2 (32kHz clock applied conditions) |                      | 32.768 |     | kHz  |
| Event count input clock pulse width         | t <sub>TL</sub> ,<br>t <sub>TH</sub> | TEX             | Fig. 3   | 10                   |        |     | μs   |
| Event count input clock rise and fall times | t <sub>TR</sub> ,<br>t <sub>TF</sub> | TEX             | Fig. 3   |                      |        | 20  | ms   |

\*1 t<sub>sys</sub> indicates three values according to the contents of the clock control register (CLC: 00FEh) upper 2 bits (CPU clock selection).

t<sub>sys</sub> (ns) = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Fig. 1. Clock timing

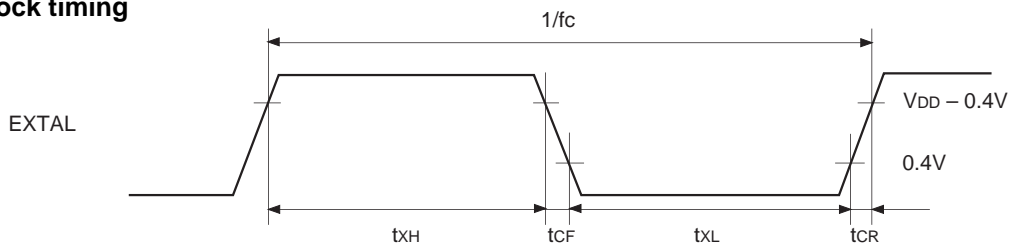


Fig.2. Clock applied conditions

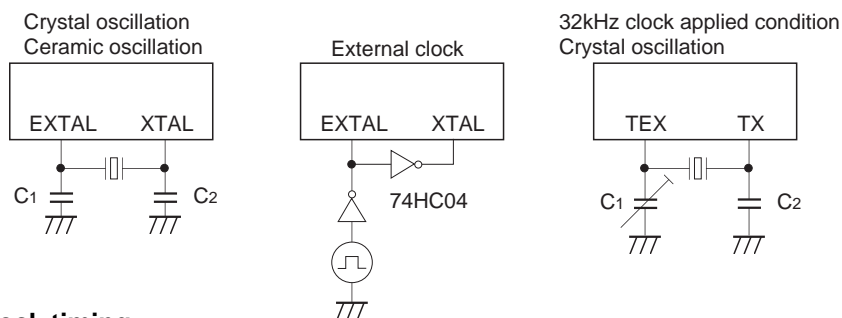
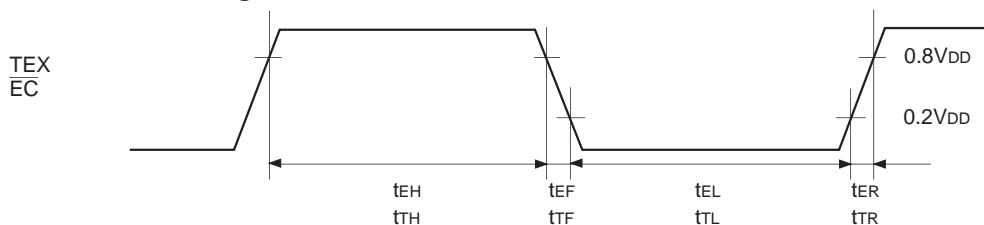


Fig. 3. Event count clock timing



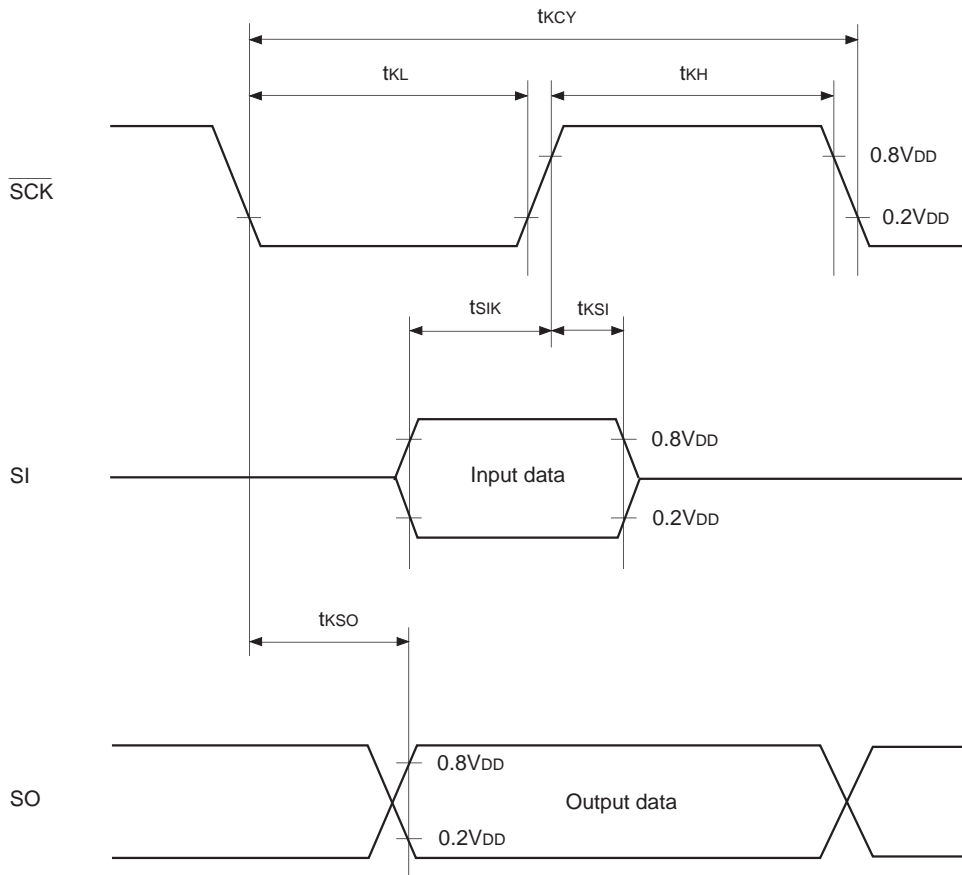
(2) Serial transfer

( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

| Item  | Symbol           | Pins                    | Conditions                          | Min.            | Max. | Unit |
|---|------------------|-------------------------|-------------------------------------|-----------------|------|------|
| $\overline{\text{SCK}}$ cycle time                                  | $t_{\text{KCY}}$ | $\overline{\text{SCK}}$ | Input mode                          | 1000            |      | ns   |
|   |                  |                         | Output mode                         | $8000/f_c$      |      | ns   |
| $\overline{\text{SCK}}$ High and Low level width                    | $t_{\text{KH}}$  | $\overline{\text{SCK}}$ | $\overline{\text{SCK}}$ input mode  | 400             |      | ns   |
|   | $t_{\text{KL}}$  |                         | $\overline{\text{SCK}}$ output mode | $4000/f_c - 50$ |      | ns   |
| SI input setup time (for $\overline{\text{SCK}} \uparrow$ )         | $t_{\text{SIK}}$ | SI                      | $\overline{\text{SCK}}$ input mode  | 100             |      | ns   |
|   |                  |                         | $\overline{\text{SCK}}$ output mode | 200             |      | ns   |
| SI hold time (for $\overline{\text{SCK}} \uparrow$ )                | $t_{\text{KSI}}$ | SI                      | $\overline{\text{SCK}}$ input mode  | 200             |      | ns   |
|   |                  |                         | $\overline{\text{SCK}}$ output mode | 100             |      | ns   |
| $\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time | $t_{\text{KSO}}$ | SO                      | $\overline{\text{SCK}}$ input mode  |                 | 200  | ns   |
|   |                  |                         | $\overline{\text{SCK}}$ output mode |                 | 100  | ns   |

Note) The load of  $\overline{\text{SCK}}$  output mode and SO output delay time is  $50\text{pF} + 1\text{TTL}$ .

Fig. 4. Serial transfer timing

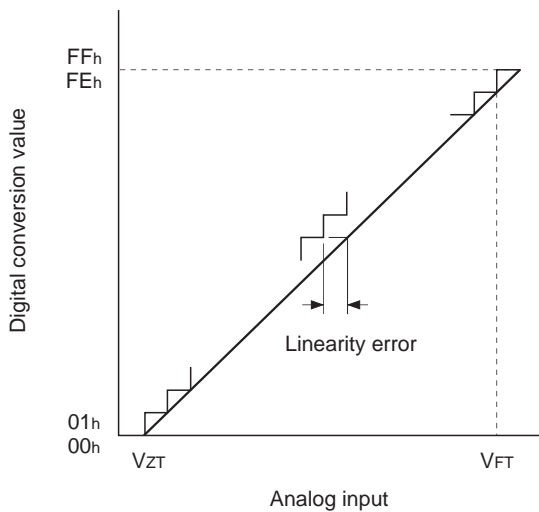


(3) A/D converter

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

| Item                          | Symbol             | Pins       | Conditions                          | Min.                   | Typ. | Max.            | Unit |
|-------------------------------|--------------------|------------|-------------------------------------|------------------------|------|-----------------|------|
| Resolution                    |                    |            |                                     |                        |      | 8               | Bits |
| Linearity error               |                    |            |                                     |                        |      | ±3              | LSB  |
| Zero transition voltage       | V <sub>ZT</sub> *1 |            | Ta = 25°C<br>VDD = 5.0V<br>Vss = 0V | -10                    | 10   | 70              | mV   |
| Full-scale transition voltage | V <sub>FT</sub> *2 |            |                                     | 4910                   | 4970 | 5030            | mV   |
| Conversion time               | t <sub>CONV</sub>  |            |                                     | 26/f <sub>ADC</sub> *3 |      |                 | µs   |
| Sampling time                 | t <sub>SAMP</sub>  |            |                                     | 6/f <sub>ADC</sub> *3  |      |                 | µs   |
| Analog input voltage          | V <sub>IAN</sub>   | AN0 to AN5 |                                     | 0                      |      | V <sub>DD</sub> | V    |

Fig. 5. Definitions of A/D converter terms



\*1 V<sub>ZT</sub>: Value at which the digital conversion value changes from 00h to 01h and vice versa.

\*2 V<sub>FT</sub>: Value at which the digital conversion value changes from FEh to FFh and vice versa.

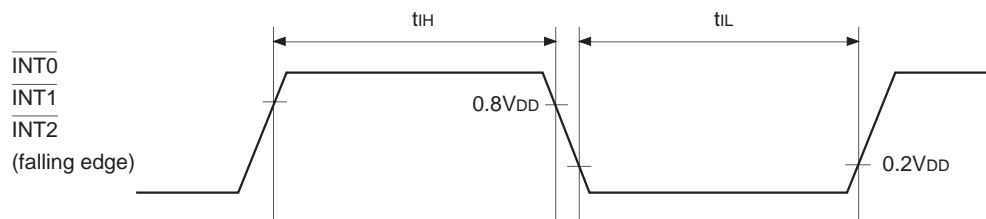
\*3 f<sub>ADC</sub> indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F6h):

$$f_{ADC} = f_c \text{ (CKS = "0")}, f_c/2 \text{ (CKS = "1")}$$

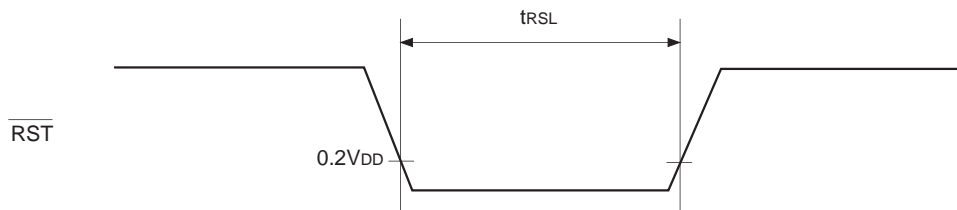
**(4) Interruption, reset input** ( $T_a = -20$  to  $+75^\circ\text{C}$ ,  $V_{DD} = 4.5$  to  $5.5\text{V}$ ,  $V_{SS} = 0\text{V}$  reference)

| Item   | Symbol               | Pins   | Conditions | Min.     | Max. | Unit          |
|--|----------------------|--|------------|----------|------|---------------|
| External interruption High,<br>Low level width | $t_{IH}$<br>$t_{IL}$ | $\overline{\text{INT0}}$<br>$\overline{\text{INT1}}$<br>$\overline{\text{INT2}}$ |            | 1        |      | $\mu\text{s}$ |
| Reset input Low level width                    | $t_{RSL}$            | $\overline{\text{RST}}$  |            | $32/f_c$ |      | $\mu\text{s}$ |

**Fig. 6. Interruption input timing**



**Fig. 7.  $\overline{\text{RST}}$  input timing**





(5) I<sup>2</sup>C bus timing

(Ta = -20 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                                   | Symbol               | Pins     | Conditions | Min. | Max. | Unit |
|--|----------------------|----------|------------|------|------|------|
| SCL clock frequency                    | f <sub>SCL</sub>     | SCL      |            | 0    | 100  | kHz  |
| Bus-free time before starting transfer | t <sub>BUF</sub>     | SDA, SCL |            | 4.7  |      | μs   |
| Hold time for starting transfer        | t <sub>HD; STA</sub> | SDA, SCL |            | 4.0  |      | μs   |
| Clock Low level width                  | t <sub>LOW</sub>     | SCL      |            | 4.7  |      | μs   |
| Clock High level width                 | t <sub>HIGH</sub>    | SCL      |            | 4.0  |      | μs   |
| Setup time for repeated transfers      | t <sub>SU; STA</sub> | SDA, SCL |            | 4.7  |      | μs   |
| Data hold time                         | t <sub>HD; DAT</sub> | SDA, SCL |            | 0*1  |      | μs   |
| Data setup time                        | t <sub>SU; DAT</sub> | SDA, SCL |            | 250  |      | ns   |
| SDA, SCL rise time                     | t <sub>R</sub>       | SDA, SCL |            |      | 1    | μs   |
| SDA, SCL fall time                     | t <sub>F</sub>       | SDA, SCL |            |      | 300  | ns   |
| Setup time for transfer completion     | t <sub>SU; STO</sub> | SDA, SCL |            | 4.7  |      | μs   |

\*1 The data hold time should be 300ns or more because the SCL rise time (300ns Max.) is not included in it.

Fig. 8. I<sup>2</sup>C bus transfer timing

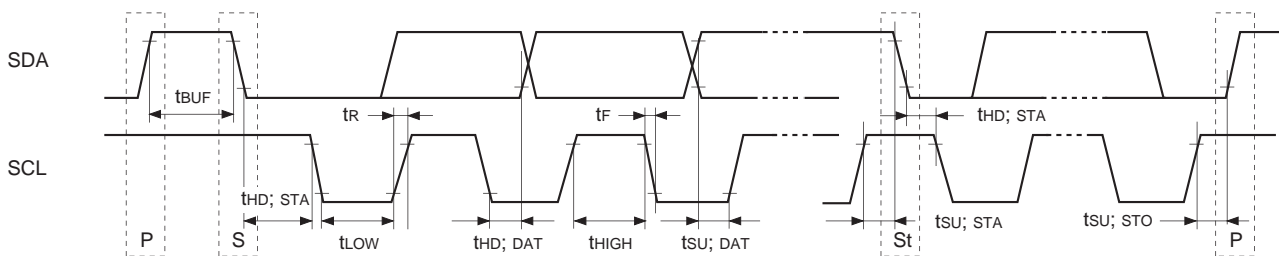
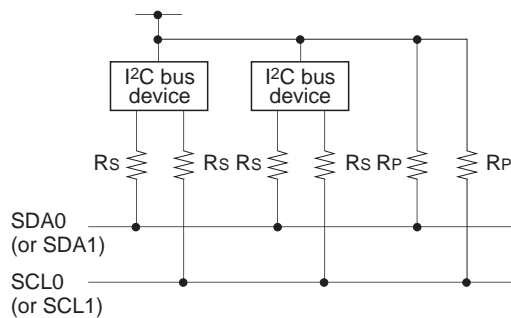


Fig. 9. I<sup>2</sup>C bus device recommended circuit



- A pull-up resistor (Rp) must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- The SDA0 (or SDA1) and SCL0 (or SCL1) series resistance (Rs) can be used to reduce the spike noise caused by CRT flashover.

**(6) OSD timing** (Ta = -20 to +75°C, VDD = 4.5 to 5.5V, Vss = 0V reference)

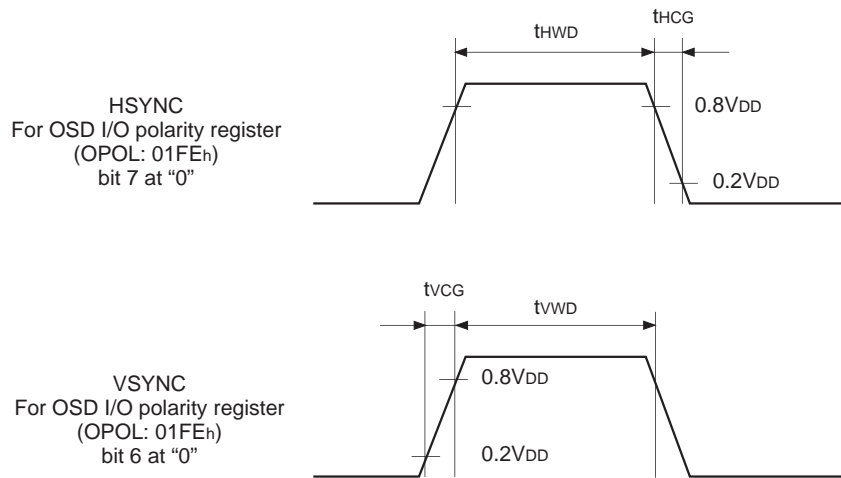
| Item                                  | Symbol | Pins        | Conditions | Min. | Max  | Unit |
|---------------------------------------|--------|-------------|------------|------|------|------|
| OSD clock frequency                   | fosc   | EXLC<br>XLC | Fig. 11    | 4    | 28*1 | MHz  |
| HSYNC pulse width                     | tHWD   | HSYNC       | Fig. 10    | 2    |      | µs   |
| VSYNC pulse width                     | tVWD   | VSYNC       | Fig. 10    | 1    |      | H*2  |
| HSYNC afterwrite rise and fall times  | tHCG   | HSYNC       | Fig. 10    |      | 200  | ns   |
| VSYNC beforewrite rise and fall times | tVCG   | VSYNC       | Fig. 10    |      | 1.0  | µs   |

\*1 The maximum value of fosc is specified with the following equation.

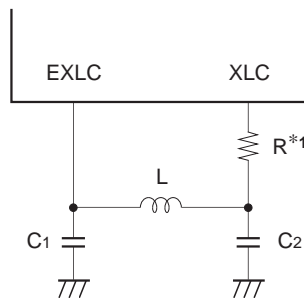
$$f_{osc} [max] \leq f_c \times 1.9$$

\*2 H indicates 1HSYNC period.

**Fig. 10. OSD timing**



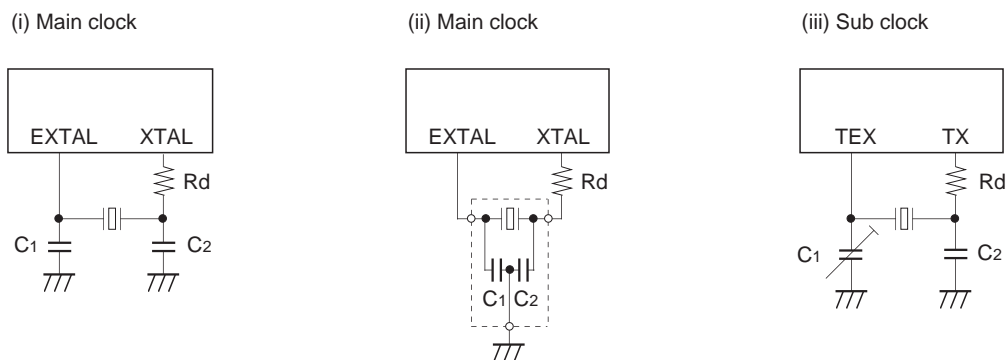
**Fig. 11. LC oscillation circuit connection**



\*1 The series resistor for XLC is used to reduce the frequency of occurrence of the undesired radiation.

Appendix

Fig. 12. Recommended oscillation circuit



| Manufacture            | Model           | fc (MHz)  | C <sub>1</sub> (pF) | C <sub>2</sub> (pF) | R <sub>d</sub> ( $\Omega$ ) | Circuit example |
|------------------------|-----------------|-----------|---------------------|---------------------|-----------------------------|-----------------|
| MURATA MFG CO., LTD    | CSA10.0MTZ      | 10.0      | 30                  | 30                  | 0* <sup>1</sup>             | (i)             |
|                        | CSA12.0MTZ      | 12.0      |                     |                     |                             |                 |
|                        | CSA16.00MXZ040  | 16.0      | 5                   | 5                   |                             |                 |
|                        | CST10.0MTW*     | 10.0      | 30                  | 30                  |                             | (ii)            |
|                        | CST12.0MTW*     | 12.0      |                     |                     |                             |                 |
|                        | CST16.00MXW0C1* | 16.0      | 5                   | 5                   |                             |                 |
| RIVER ELETEC CO., LTD. | HC-49/U03       | 8.0       | 18                  | 18                  | 330* <sup>1</sup>           | (i)             |
|                        |                 | 12.0      | 12                  | 12                  |                             |                 |
|                        |                 | 16.0      | 10                  | 10                  |                             |                 |
| KINSEKI LTD.           | HC-49/U (-S)    | 8.0       | 10                  | 10                  | 0* <sup>1</sup>             |                 |
|                        |                 | 12.0      | 5                   | 5                   |                             |                 |
|                        |                 | 16.0      | OPEN                | OPEN                |                             |                 |
|                        | P3              | 32.768kHz | 30                  | 33                  | 120k                        | (iii)           |

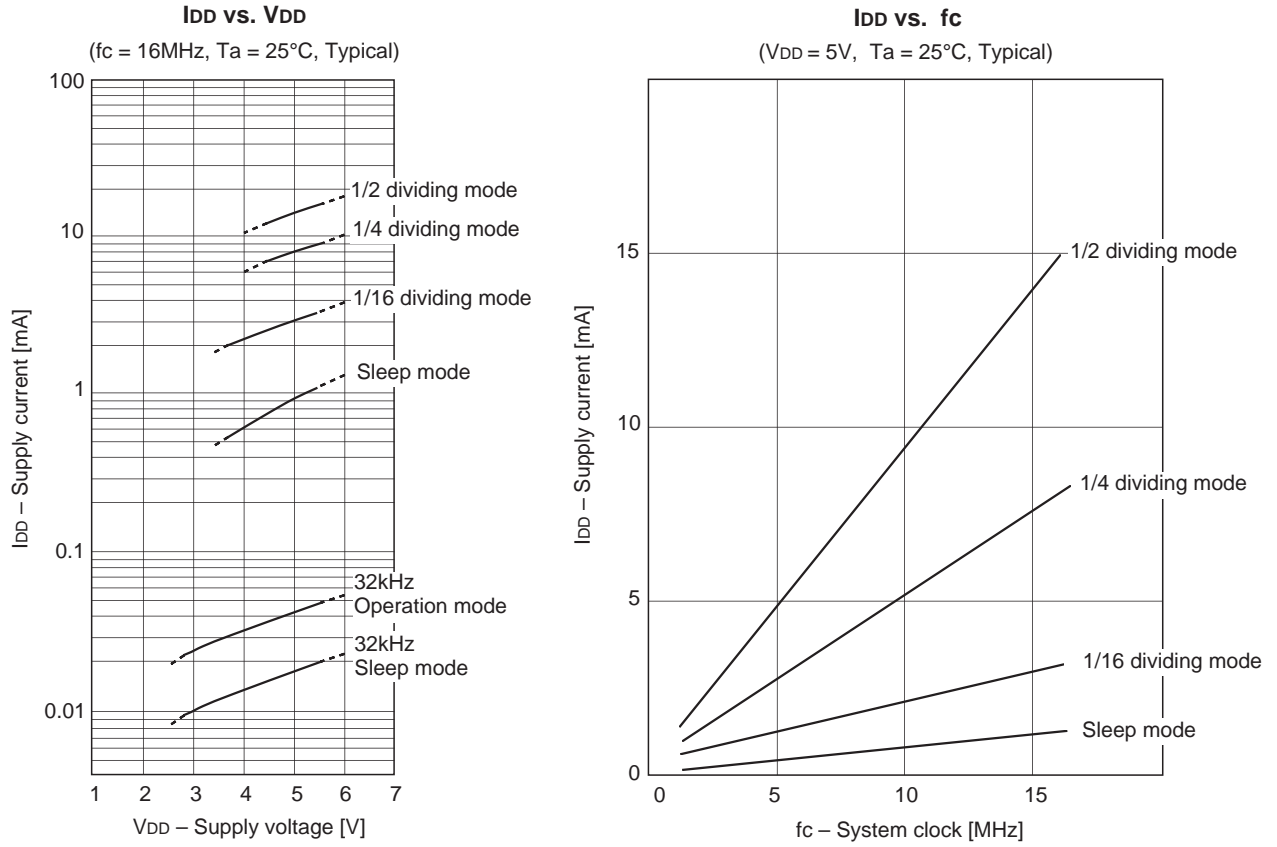
\* Models with an asterisk have the built-in ground capacitance (C<sub>1</sub>, C<sub>2</sub>).

\*<sup>1</sup> The series resistor for XTAL can reduce the effect of the noise caused by the electrostatic discharge.

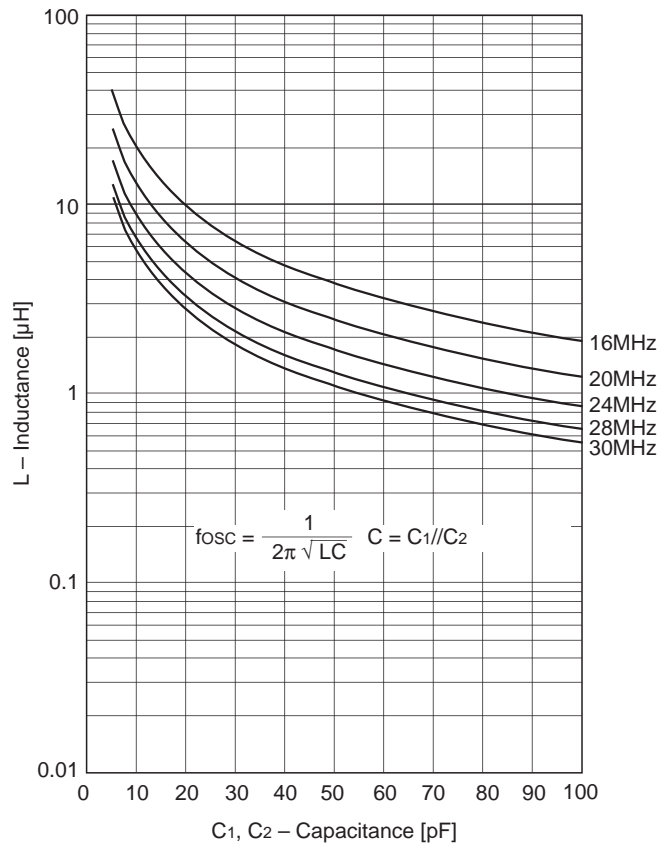
Mask Option Table

| Item                       | Content      |          |
|----------------------------|--------------|----------|
| Reset pin pull-up resistor | Non-existent | Existent |

Fig. 13. Characteristic curves



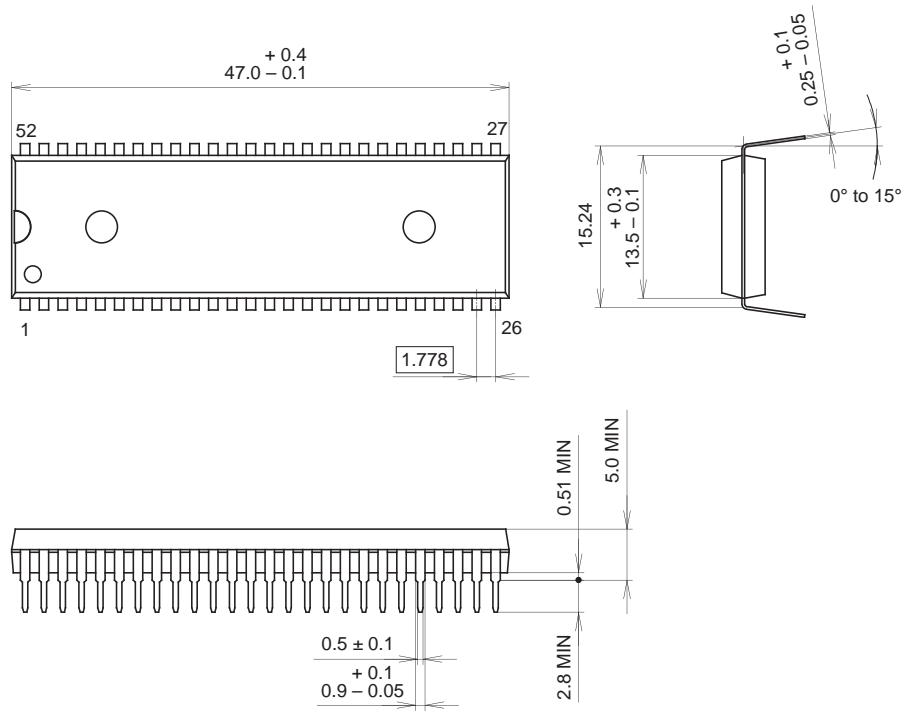
Parameter curve for OSD oscillation L vs. C  
(theoretically calculated value)



**Package Outline**

Unit: mm

**52PIN SDIP (PLASTIC)**



**PACKAGE STRUCTURE**

|            |                |
|------------|----------------|
| SONY CODE  | SDIP-52P-01    |
| EIAJ CODE  | SDIP052-P-0600 |
| JEDEC CODE | _____          |

|                  |                          |
|------------------|--------------------------|
| PACKAGE MATERIAL | EPOXY RESIN              |
| LEAD TREATMENT   | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL    | COPPER ALLOY             |
| PACKAGE MASS     | 5.6g                     |

**NOTE : PALLADIUM PLATING**

This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).