SONY

CXP87532/87540

CMOS 8-bit Single Chip Microcomputer

Description

The CXP87532/87540 is a CMOS 8-bit micro-computer which consists of arithmetic coprocessor, A/D converter, serial interface, timer/counter, time base timer, vector interruption, high precision timing pattern generation circuit, PWM generator and the measuring circuit which measures signals of capstan FG, drum FG/PG, reel FG and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also this IC provides power on reset function, sleep/stop function which enables to lower power consumption.

100 pin QFP (Plastic)   100 pin LQFP (Plastic)

Structure

Silicon gate CMOS IC

Features

- A wide instruction set (213 instructions) which covers various types of data
  — 16-bit operation multiplycation and division/boolean bit operation instructions
- Minimum instruction cycle   During operation 326ns/12.288MHz
- Incorporated ROM capacity   32K bytes (CXP87532)
                                     40K bytes (CXP87540)
- Incorporated RAM capacity   1344 bytes
- Peripheral functions
  — Arithmetic coprocessor   Multiplying with code, sum of products with code, high speed execution of many bits shift rotation operation
  — A/D converter   8-bit, 8-channel, successive approximation system (Conversion time 13µs/12.288MHz) Incorporated 3-stage FIFO for A/D conversion data
  — Serial interface   Incorporated buffer RAM for data (1 to 128 bytes auto transfer) 2-channel
  — Timer   8-bit timer, 8-bit timer/counter, 19-bit time base timer
  — High precision timing pattern generator   PPG (11 pins) 32-stage programmable
  — PWM output   12-bit, 2-channel (Repeated frequency 48kHz) 8-bit, 3-channel (Repeated frequency 48kHz)
  — Servo input control   Capstan FG, Drum FG/PG, Reel FG input
  — FRC capture unit   Incorporated 28-bit and 8-stage FIFO
- Interruption   12 factors, 12 vectors, multi-interruption possible
- Standby mode   Sleep/stop
- Package   100-pin plastic QFP/LQFP
- Piggyback/Evaluation   CXP87500 100-pin ceramic QFP/LQFP
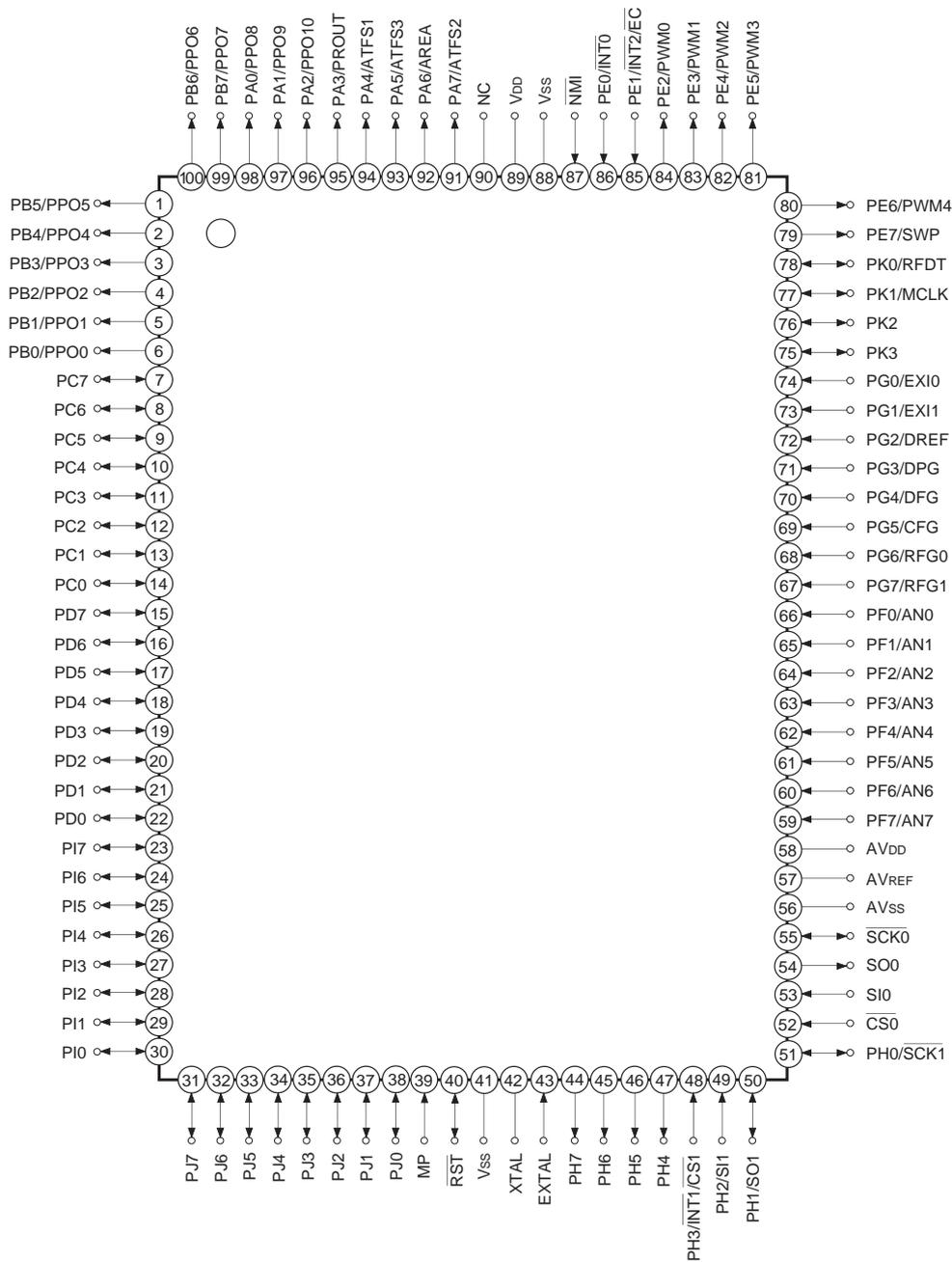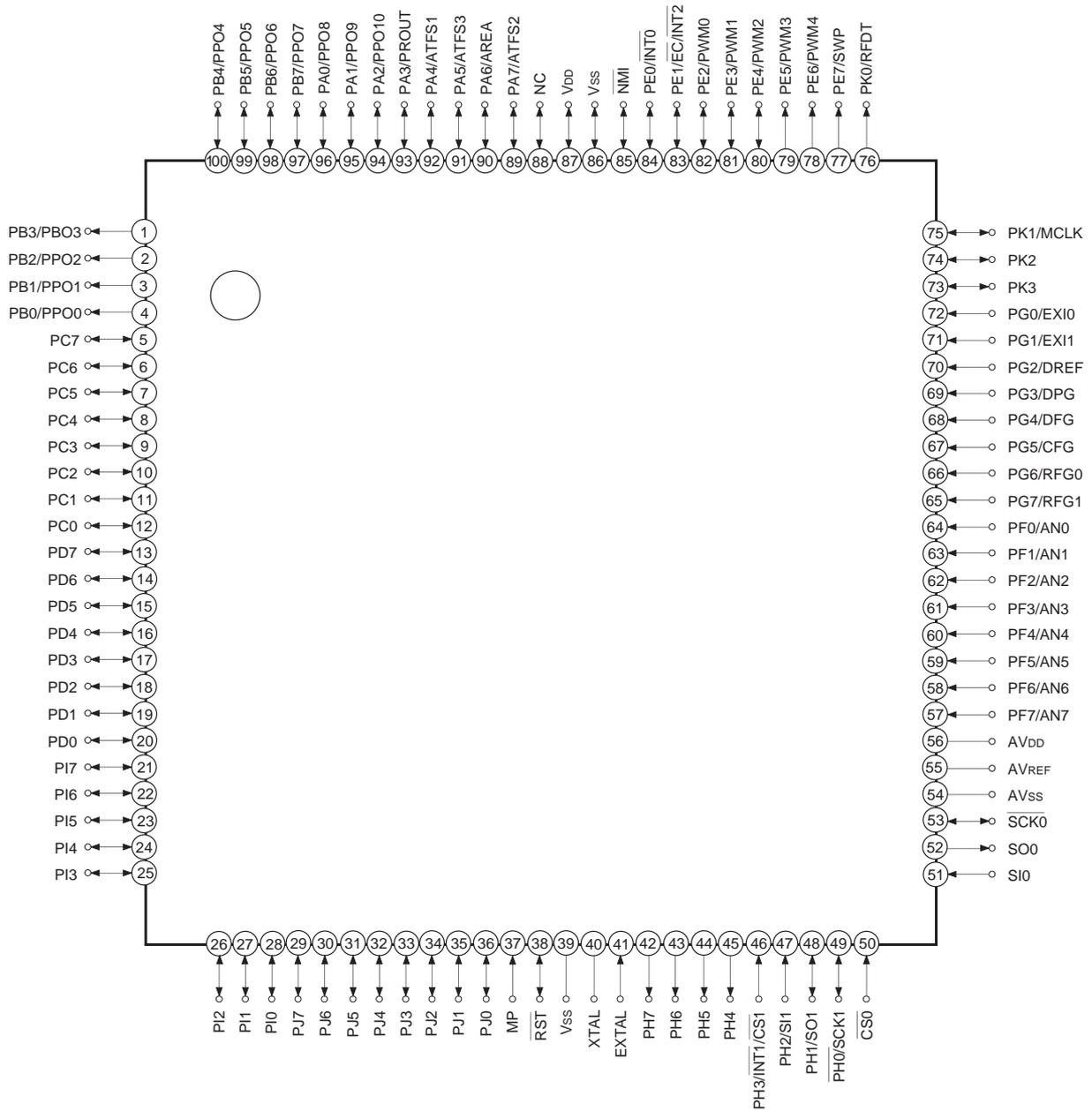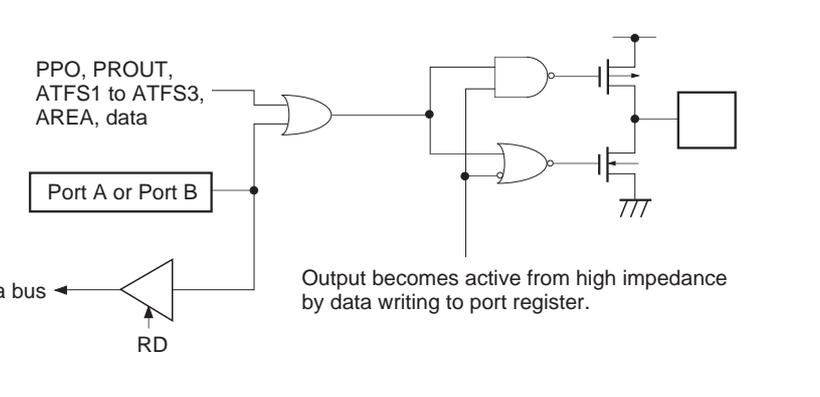
E93820A81-PS

Block Diagram

Pin Assignment 1 (Top View) 100pin QFP

Note) 1. NC (Pin 90) is always connected to V$_{DD}$.

       2. V$_{SS}$ (Pins 41 and 88) are both connected to GND.

       3. MP (Pin 39) is always connected to V$_{SS}$.
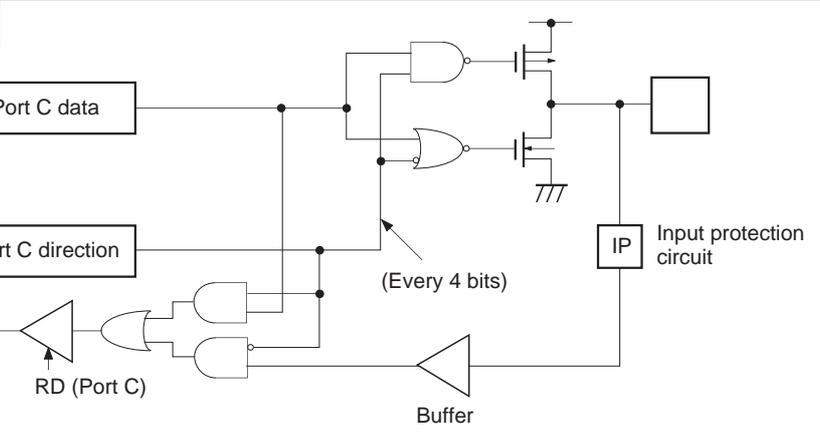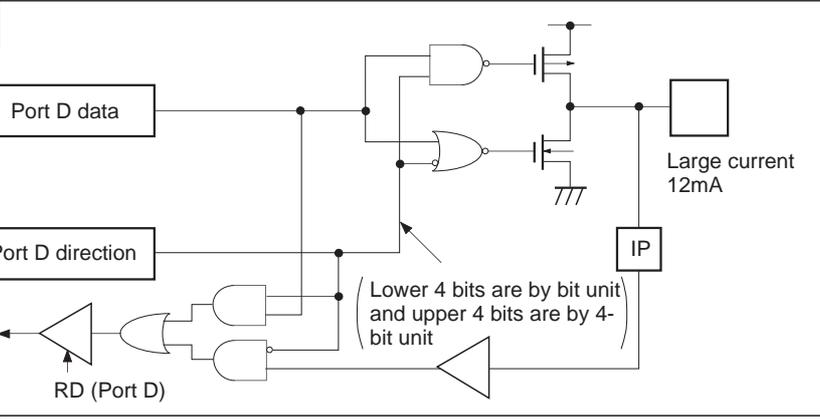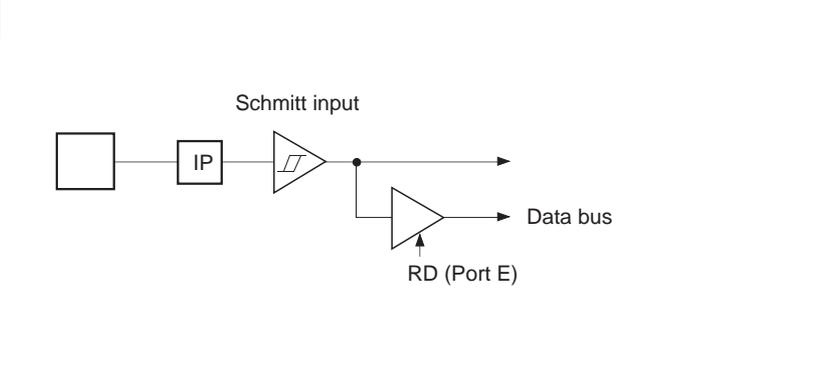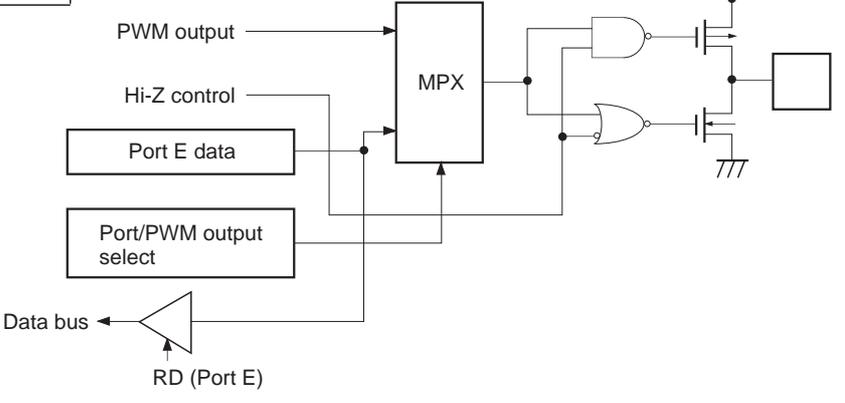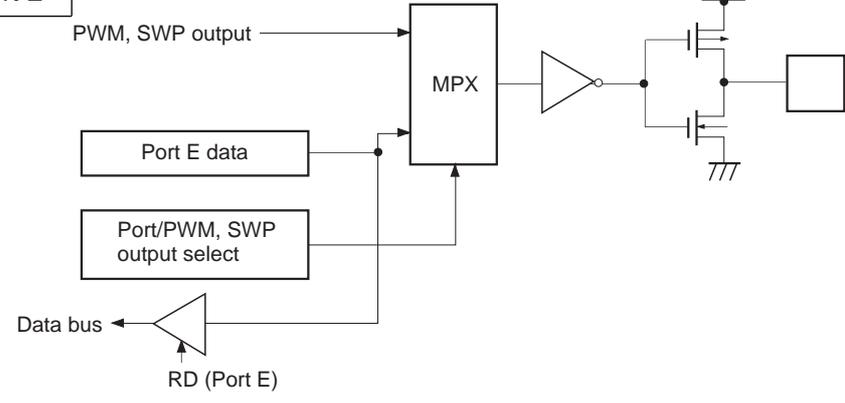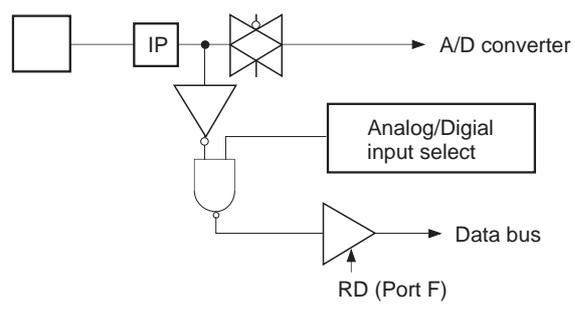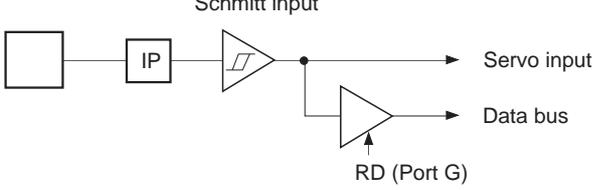
Pin Assignment 2 (Top View) 100pin LQFP

Pin labels (top, pins 100–76): PB4/PPO4, PB5/PPO5, PB6/PPO6, PB7/PPO7, PA0/PPO8, PA1/PPO9, PA2/PPO10, PA3/PROUT, PA4/ATFS1, PA5/ATFS3, PA6/AREA, PA7/ATFS2, NC, VDD, VSS, NMI, PE0/INT0, PE1/EC/INT2, PE2/PWM0, PE3/PWM1, PE4/PWM2, PE5/PWM3, PE6/PWM4, PE7/SWP, PK0/RFDT

Left side (pins 1–25): PB3/PBO3 (1), PB2/PPO2 (2), PB1/PPO1 (3), PB0/PPO0 (4), PC7 (5), PC6 (6), PC5 (7), PC4 (8), PC3 (9), PC2 (10), PC1 (11), PC0 (12), PD7 (13), PD6 (14), PD5 (15), PD4 (16), PD3 (17), PD2 (18), PD1 (19), PD0 (20), PI7 (21), PI6 (22), PI5 (23), PI4 (24), PI3 (25)

Right side (pins 75–51): PK1/MCLK (75), PK2 (74), PK3 (73), PG0/EXI0 (72), PG1/EXI1 (71), PG2/DREF (70), PG3/DPG (69), PG4/DFG (68), PG5/CFG (67), PG6/RFG0 (66), PG7/RFG1 (65), PF0/AN0 (64), PF1/AN1 (63), PF2/AN2 (62), PF3/AN3 (61), PF4/AN4 (60), PF5/AN5 (59), PF6/AN6 (58), PF7/AN7 (57), AVDD (56), AVREF (55), AVSS (54), SCK0 (53), SO0 (52), SI0 (51)

Bottom (pins 26–50): PI2, PI1, PI0, PJ7, PJ6, PJ5, PJ4, PJ3, PJ2, PJ1, PJ0, MP, RST, VSS, XTAL, EXTAL, PH7, PH6, PH5, PH4, PH3/INT1/CS1, PH2/SI1, PH1/SO1, PH0/SCK1, CS0

Note) 1. NC (Pin 88) is always connected to VDD.

2. VSS (Pins 39 and 86) are both connected to GND.

3. MP (Pin 37) is always connected to VSS.

Pin Description

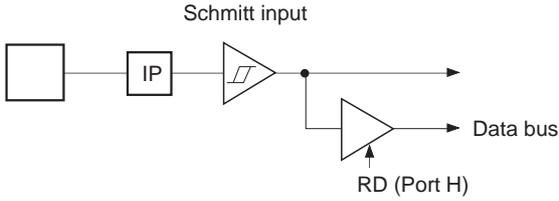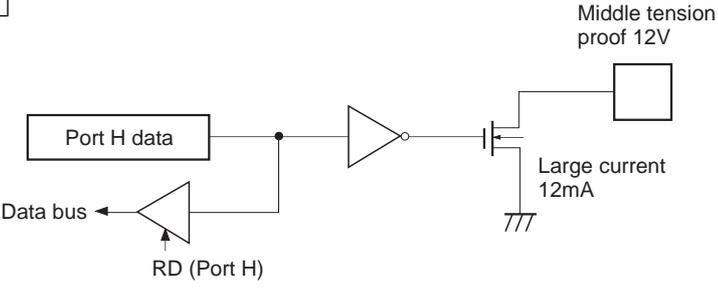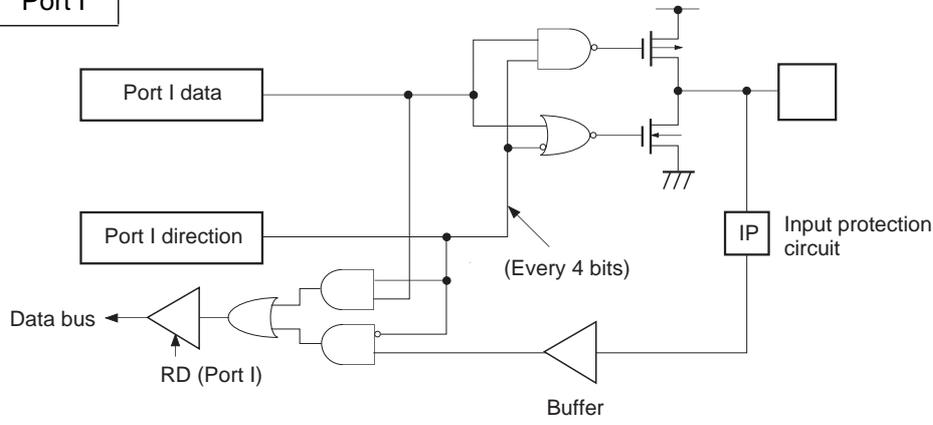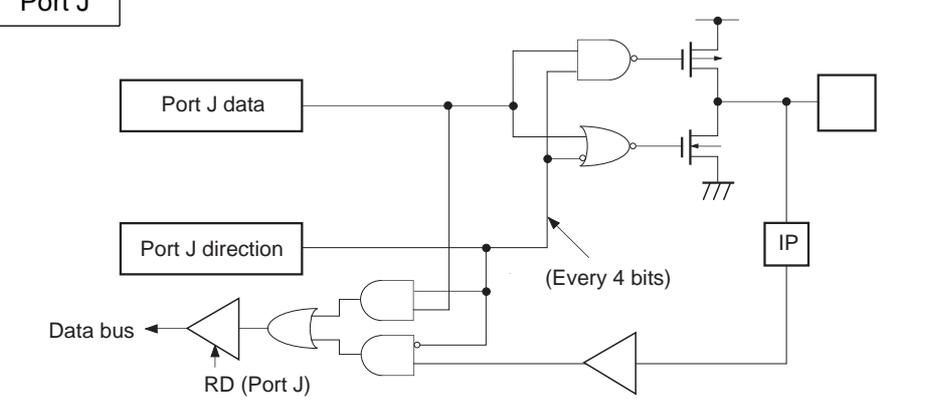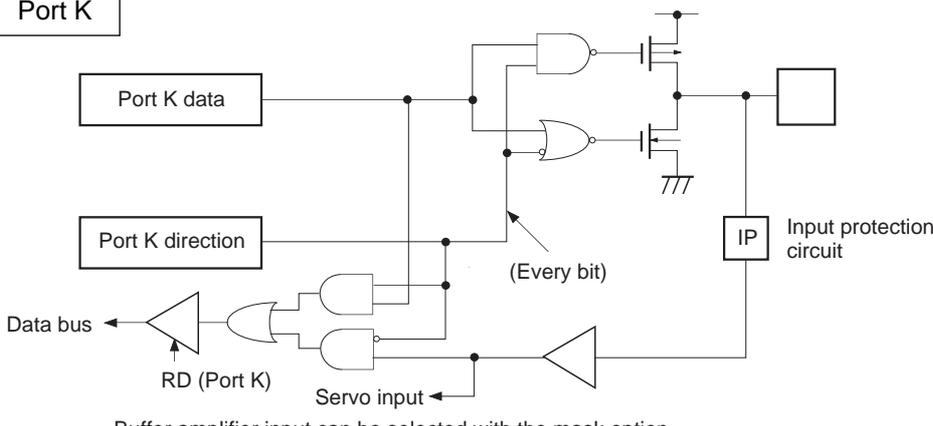| Symbol	I/O	Description	
PA0/PPO8 PA1/PPO9 PA2/PPO10 PA3/PROUT	Output/ Real time output	(Port A) 8-bit output port. Data is gated with PPO (3 pins), monitor signal (4 pins) in relation to ATF, control signal (1 pin) for capstan servo by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) Output (3 pins) and capstan servo control signal (1 pin).
PA4/ATFS1 PA5/ATFS3 PA6/AREA PA7/ATFS2	Output/ Monitor output		Monitor output in relation to ATF. (4 pins)
PB0/PPO0 to PB7/PPO7	Output/ Real time output	(Port B) 8-bit output port. Data is gated with PPO by OR-gate and they are output. (8 pins)	Programmable pattern generator (PPG) output. (8 pins)
PC0 to PC7	I/O	(Port C) 8-bit input/output port, enables to specify input/output by 4-bit unit. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit input/output port. Lower 4 bits can be specified as input/output by bit unit and upper 4 bits can be specified as input/output by 4-bit unit. (8 pins)	
PE0/$\overline{INT0}$	Input/Input	(Port E) 8-bit port. Lower 2 bits are input pins and upper 6 bits are output pins. (8 pins)	Input pin to request external interruption. Active when falling edge.
PE1/$\overline{EC}$/$\overline{INT2}$	Input/Input/ Input		External event input pin for timer/counter. / Input pin to request external interruption. Active when falling edge.
PE2/PWM0 to PE6/PWM4	Output/Output		PWM output pins (5 pins)
PE7/SWP	Output/Output		SWP output pin.
PF0/AN0 to PF7/AN7	Input/Input	(Port F) 8-bit input port. (8 pins) Upper 4 bits serve as standby release input pin.	Analog input pins to A/D converter. (8 pins)
PG0/EXI0	Input/Input	(Port G) 8-bit input port. (8 pins)	External input pin 0.
PG1/EXI1	Input/Input		External input pin 1.
PG2/DREF	Input/Input		Drum reference signal input pin.
PG3/DPG	Input/Input		Drum PG input pin.
PG4/DFG	Input/Input		Drum FG input pin.
PG5/CFG	Input/Input		Capstan FG input pin.
PG6/RFG0	Input/Input		Reel FG input pin.
PG7/RFG1	Input/Input		

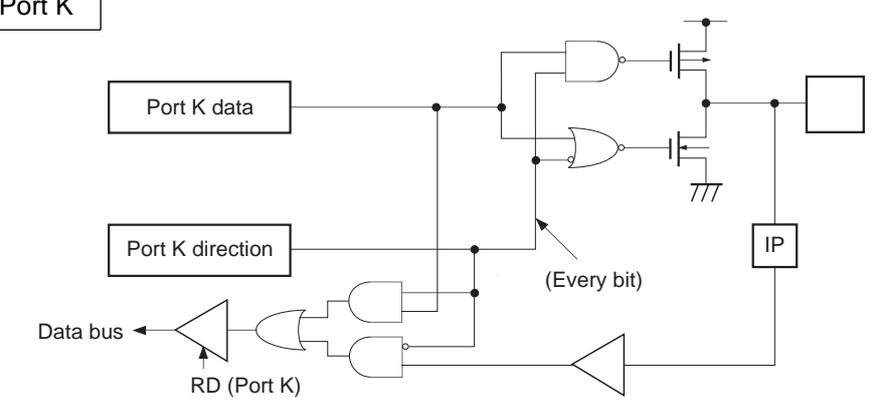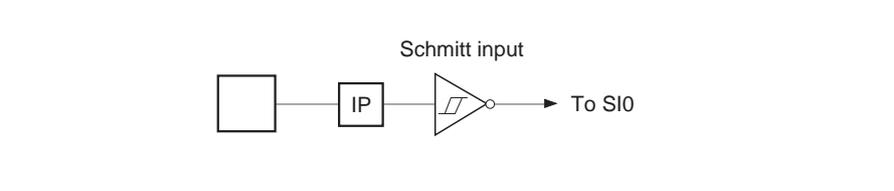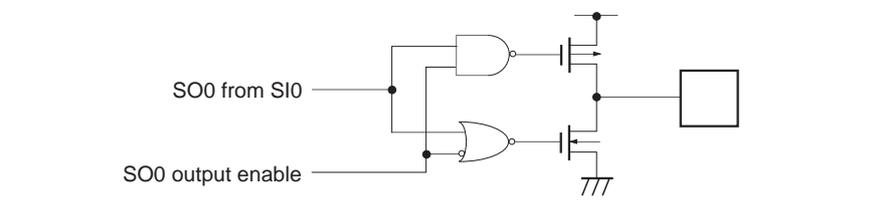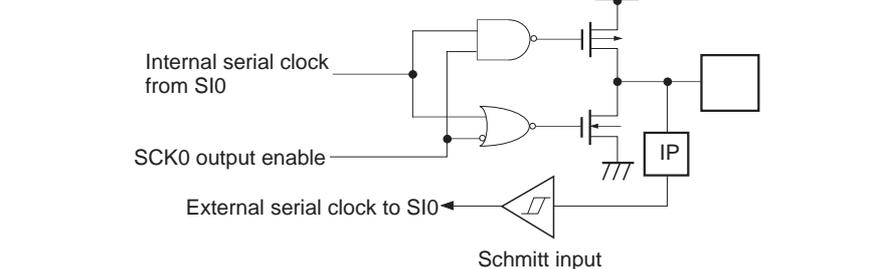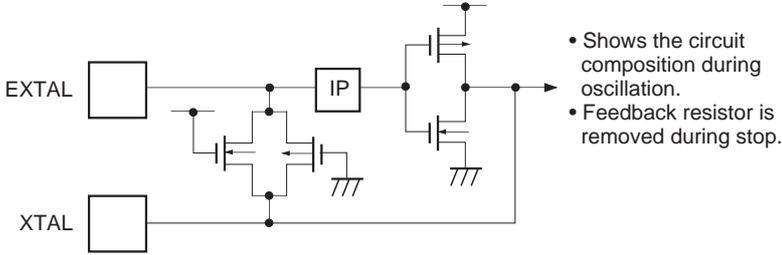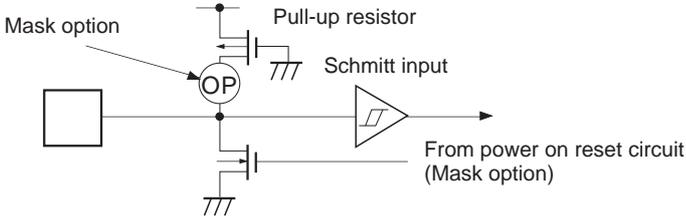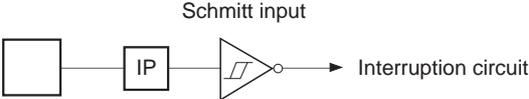| Symbol	I/O	Description		
PH0/$\overline{\text{SCK1}}$	Input/I/O	(Port H) 4-bit input port. (4 pins)		Serial clock input/output pin.
PH1/SO1	Input/Output			Serial data output pin.
PH2/SI1	Input/Input			Serial data input pin.
PH3/$\overline{\text{INT1}}$/ $\overline{\text{CS1}}$	Input/Input/Input		Input pin to request external interruption. Active when falling edge.	Chip select input pin to serial interface.
PH7 to PH4	Output	(Port H) 4-bit output port. N-ch open drain output of middle tension proof (12V) and large current (12mA). (4 pins)		
PI0 to PI7	I/O	(Port I) 8-bit input/output port, enables to specify input/output by 4-bit unit. (8 pins)		
PJ0 to PJ7	I/O	(Port J) 8-bit input/output port, enables to specify input/output by 4-bit unit. (8 pins)		
PK0/RFDT	I/O/Input	(Port K) 4-bit input/output port, enables to specify input/ output by bit unit. (4 pins)		Playback data input pin.
PK1/MCLK	I/O/Input			Channel clock input pin.
PK2, PK3	I/O			
$\overline{\text{SCK0}}$	I/O	Serial clock input/output pin.		
SO0	Output	Serial data output pin.		
SI0	Input	Serial data input pin.		
$\overline{\text{CS0}}$	Input	Chip select input pin to serial interface.		
$\overline{\text{NMI}}$	Input	Non-maskable interrupt request pin. Active during falling edge.		
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input the external clock to EXTAL pin and set XTAL pin to open.		
XTAL	Output			
$\overline{\text{RST}}$	I/O	System reset pin of active "L" level. $\overline{\text{RST}}$ pin is input/output pin, which output "L" level by incorporated power on reset function when power ON. (Mask option)		
MP	Input	Test mode pin. This pin is always connected to GND.		
AV$_{DD}$		Positive power supply pin of A/D converter. Set the same voltage as V$_{DD}$.		
AV$_{REF}$	Input	Reference voltage input pin of A/D converter.		
AV$_{SS}$		GND pin of A/D converter.		
V$_{DD}$		Positive power supply pin.		
V$_{SS}$		GND pin. Connect both V$_{SS}$ pins to GND.		

I/O Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO8 to PA2/PPO10 PA3/PROUT PA4/ATFS1 PA5/ATFS3 PA6/AREA PA7/ATFS2 PB0/PPO0 to PB7/PPO7 16 pins	Port A / Port B — PPO, PROUT, ATFS1 to ATFS3, AREA, data; Port A or Port B; Data bus; RD; Output becomes active from high impedance by data writing to port register.	Hi-Z
PC0 to PC7 8 pins	Port C — Port C data; Port C direction; (Every 4 bits); Data bus; RD (Port C); Buffer; IP Input protection circuit	Hi-Z
PD0 to PD7 8 pins	Port D — Port D data; Port D direction; Lower 4 bits are by bit unit and upper 4 bits are by 4-bit unit; Large current 12mA; IP; Data bus; RD (Port D)	Hi-Z
PE0/INT0 PE1/EC/ INT2 2 pins	Port E — IP; Schmitt input; Data bus; RD (Port E)	Hi-Z

Pin	Circuit format	When reset
PE2/PWM0 PE3/PWM1 PE4/PWM2 PE5/PWM3 4 pins	Port E PWM output → MPX Hi-Z control → Port E data → Port/PWM output select → Data bus ← RD (Port E)	Hi-Z
PE6/PWM4 PE7/SWP 2 pins	Port E PWM, SWP output → MPX Port E data → Port/PWM, SWP output select → Data bus ← RD (Port E)	H level
PF0/AN0 to PF7/AN7 8 pins	Port F Input multiplexer IP → A/D converter Analog/Digial input select Data bus RD (Port F)	Hi-Z
PG0/EXI0 PG1/EXI1 PG2/DREF PG3/DPG PG4/DFG PG5/CFG PG6/RFG0 PG7/RFG1 8 pins	Port G Schmitt input IP → Servo input Data bus RD (Port G) For PG0/EXI0 to PG7/RFG1, TTL schmitt input can be selected with the mask option.	Hi-Z

Pin	Circuit format	When reset
PH0/$\overline{SCK1}$ 1 pin	Port H Internal serial clock from SI0 SCK1 output enable IP Schmitt input External serial clock to SI0 Data bus ◄ RD (Port H)	Hi-Z
PH1/SO1 1 pin	Port H SO1 from SI0 SO1 output enable IP Data bus ◄ RD (Port H)	Hi-Z
PH2/SI1 PH3/$\overline{CS1}$/ $\overline{INT1}$ 2 pins	Port H Schmitt input IP Data bus RD (Port H)	Hi-Z
PH4 to PH7 4 pins	Port H Middle tension proof 12V Port H data Data bus ◄ Large current 12mA RD (Port H)	Open
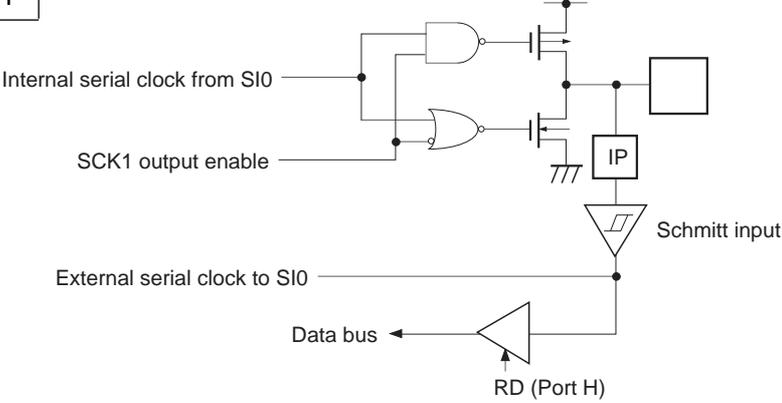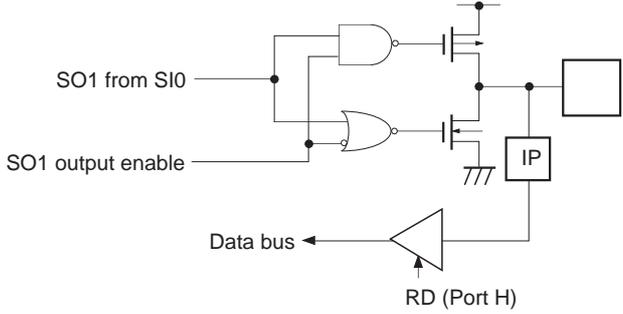
Pin	Circuit format	When reset
PI0 to PI7 8 pins	**Port I** Port I data Port I direction Data bus RD (Port I) (Every 4 bits) IP Input protection circuit Buffer	Hi-Z
PJ0 to PJ7 8 pins	**Port J** Port J data Port J direction Data bus RD (Port J) (Every 4 bits) IP	Hi-Z
PK0/RFDT 1 pin	**Port K** Port K data Port K direction Data bus RD (Port K) Servo input (Every bit) IP Input protection circuit Buffer amplifier input can be selected with the mask option.	Hi-Z When buffer amplifier input is selected, pulled up internally during standby.

Pin	Circuit format	When reset
PK1/MCLK 1 pin	Port K Port K data Port K direction (Every bit) IP Input protection circuit Data bus ◀ RD (Port K) Servo input ◀ TTL schmitt input can be selected with the mask option.	Hi-Z
PK2 to PK3 2 pins	Port K Port K data Port K direction (Every bit) IP Data bus ◀ RD (Port K)	Hi-Z
$\overline{\text{CS0}}$ SI0 2 pins	Schmitt input IP ▷○ → To SI0	Hi-Z
SO0 1 pin	SO0 from SI0 SO0 output enable	Hi-Z
$\overline{\text{SCK0}}$ 1 pin	Internal serial clock from SI0 SCK0 output enable IP External serial clock to SI0 ◀ Schmitt input	Hi-Z
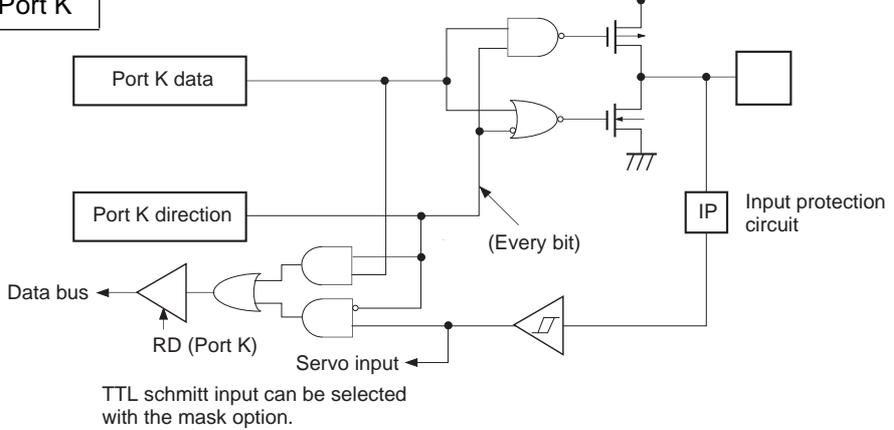
Pin	Circuit format	When reset
EXTAL XTAL 2 pins	EXTAL / XTAL oscillation circuit • Shows the circuit composition during oscillation. • Feedback resistor is removed during stop.	Oscillation
$\overline{RST}$ 1 pin	Mask option — Pull-up resistor, Schmitt input OP From power on reset circuit (Mask option)	L level
$\overline{NMI}$ 1 pin	Schmitt input IP — Interruption circuit	Hi-Z

Absolute Maximum Ratings   (V_{SS} = 0V reference)

Item	Symbol	Ratings	Unit	Remarks
Power supply voltage	V_{DD}	−0.3 to +7.0	V	
	AV_{DD}	AV_{SS} to +7.0[*1]	V	
	AV_{SS}	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0[*2]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*2]	V	
Middle tension proof output voltage	V_{OUTP}	−0.3 to +15.0	mA	PH pin
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of entire output pins
Low level output current	I_{OL}	15	mA	Other than large current output pins : per pin
	I_{OLC}	20	mA	Large current port pin [*3] : per pin
Low level total output current	ΣI_{OL}	130	mA	Total of entire output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package
		380		LQFP package

[*1] AV_{DD} and V_{DD} should be set to the same voltage.

[*2] V_{IN} and V_{OUT} should not exceed V_{DD} + 0.3V

[*3] The large current operation transistors are the N-ch transistors of the PD and PH4 to PH7.

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (V$_{SS}$ = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Power supply voltage	V$_{DD}$	4.5	5.5	V	Guaranteed range during operation
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog voltage	AV$_{DD}$	4.5	5.5	V	*1
High level input voltage	V$_{IH}$	0.7V$_{DD}$	V$_{DD}$	V	*2
	V$_{IHS}$	0.8V$_{DD}$	V$_{DD}$	V	CMOS schmitt input *3
	V$_{IHTS}$	2.2	V$_{DD}$	V	TTL schmitt input *4
	V$_{IHEX}$	V$_{DD}$ – 0.4	V$_{DD}$ + 0.3	V	EXTAL pin *5
Low level input voltage	V$_{IL}$	0	0.3V$_{DD}$	V	*2
	V$_{ILS}$	0	0.2V$_{DD}$	V	CMOS schmitt input *3
	V$_{ILTS}$	0	0.8	V	TTL schmitt input *4
	V$_{ILEX}$	–0.3	0.4	V	EXTAL pin *5
Operating temperature	Topr	–20	+75	°C	

*1 AV$_{DD}$ and V$_{DD}$ should be set to the same voltage.

*2 Normal input port (Each pin of PC, PD, PF and PH1).

*3 Each pin of $\overline{\text{NMI}}$, $\overline{\text{CS0}}$, SI0, $\overline{\text{SCK0}}$, $\overline{\text{RST}}$, PE0/$\overline{\text{INT0}}$, PE1/$\overline{\text{EC}}$/$\overline{\text{INT2}}$, PH0/$\overline{\text{SCK1}}$, PH2/SI1, PH3/$\overline{\text{INT1}}$/$\overline{\text{CS1}}$, PG and PK1/MCLK (when CMOS schmitt input is selected with mask option for PG, PK1/MCLK).

*4 Each pin of PG and PK1/MCLK (when TTL schmitt input is selected with mask option).

*5 Specified only during external clock input.

DC Characteristics

(Ta = −20 to +75°C, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE2 to PE7, PH0, PH1, SO0, $\overline{SCK0}$ PH4 to PH7	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}	(V_{OL} only) $\overline{RST}$*1 (V_{OL} only) PI to PK	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PD, PH4 to PH7	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	μA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	μA
	I_{ILR}	$\overline{RST}$*2	V_{DD} = 5.5V, V_{IL} = 0.4V	−1.5		−400	μA
I/O leakage current	I_{IZ}	PA to PG PH0 to PH3, $\overline{CS0}$, SI0, SO0, $\overline{SCK0}$, NMI, $\overline{RST}$*2 PI to PK*3	V_{DD} = 5.5V V_I = 0, 5.5V			±10	μA
Open drain output leakage current (N-ch Tr OFF in state)	I_{LOH}	PH4 to PH7	V_{DD} = 5.5V V_{OH} = 12V			50	μA
Current power supply	I_{DD}	V_{DD}	Operating mode (1/2 dividing clock) 12.288MHz crystal oscillation (C_1 = C_2 = 12pF) Entire output pins open		20	45	mA
	I_{DDSL}		Sleep mode		5	17	mA
	I_{DDST}		Stop mode			10	μA
Input capacity	C_{IN}	Other than V_{DD}, V_{SS}, AV_{DD}, and AV_{SS} pins	Clock 1MHz 0V other than the measured pins		10	20	pF

*1 $\overline{RST}$ pin specifies only when the power on reset circuit is selected with mask option.

*2 $\overline{RST}$ pin specifies the input current when the pull-up resistance is selected, and specifies leakage current when non-resistance is selected.

*3 PK0 pin specifies only when the normal input circuit is selected with mask option.

AC Characteristics

(1) Clock timing (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1	12.288	MHz
System clock input pulse width	t_{XL}, t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	36		ns
System clock input rising and falling times	t_{CR}, t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive		200	ns
Event count input clock pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 50[1]		ns
Event count input clock rising and falling times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3		20	ms

[1] t_{sys} indicates three values according to the contents of the clock control register (address : 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/f_c (Upper 2 bits = "00"), 4000/f_c (Upper 2 bits = "01"), 16000/f_c (Upper 2 bits = "11")
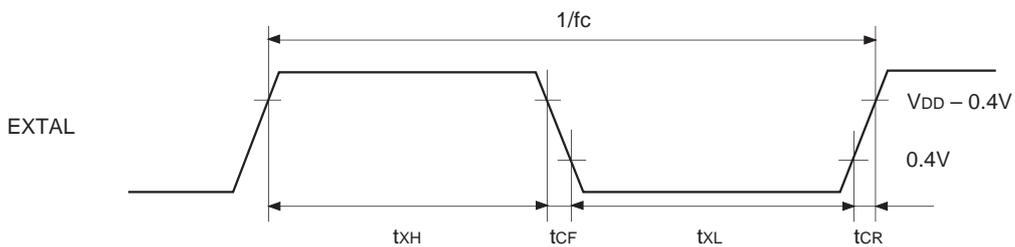
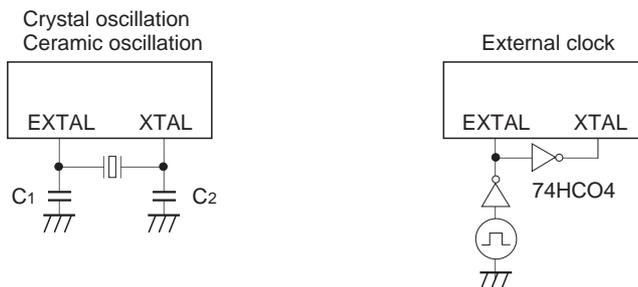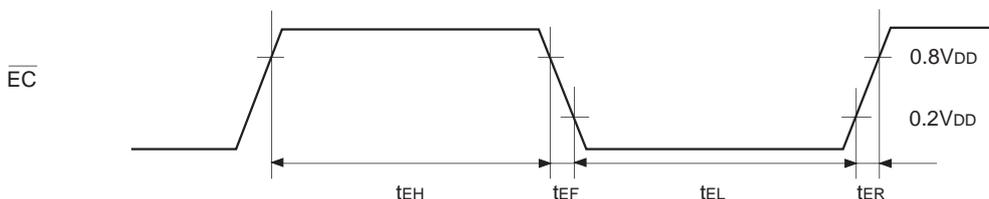**Fig. 1. Clock timing**

Fig. 2. Clock applying condition

Fig. 3. Event count clock timing

(2) Serial transfer   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

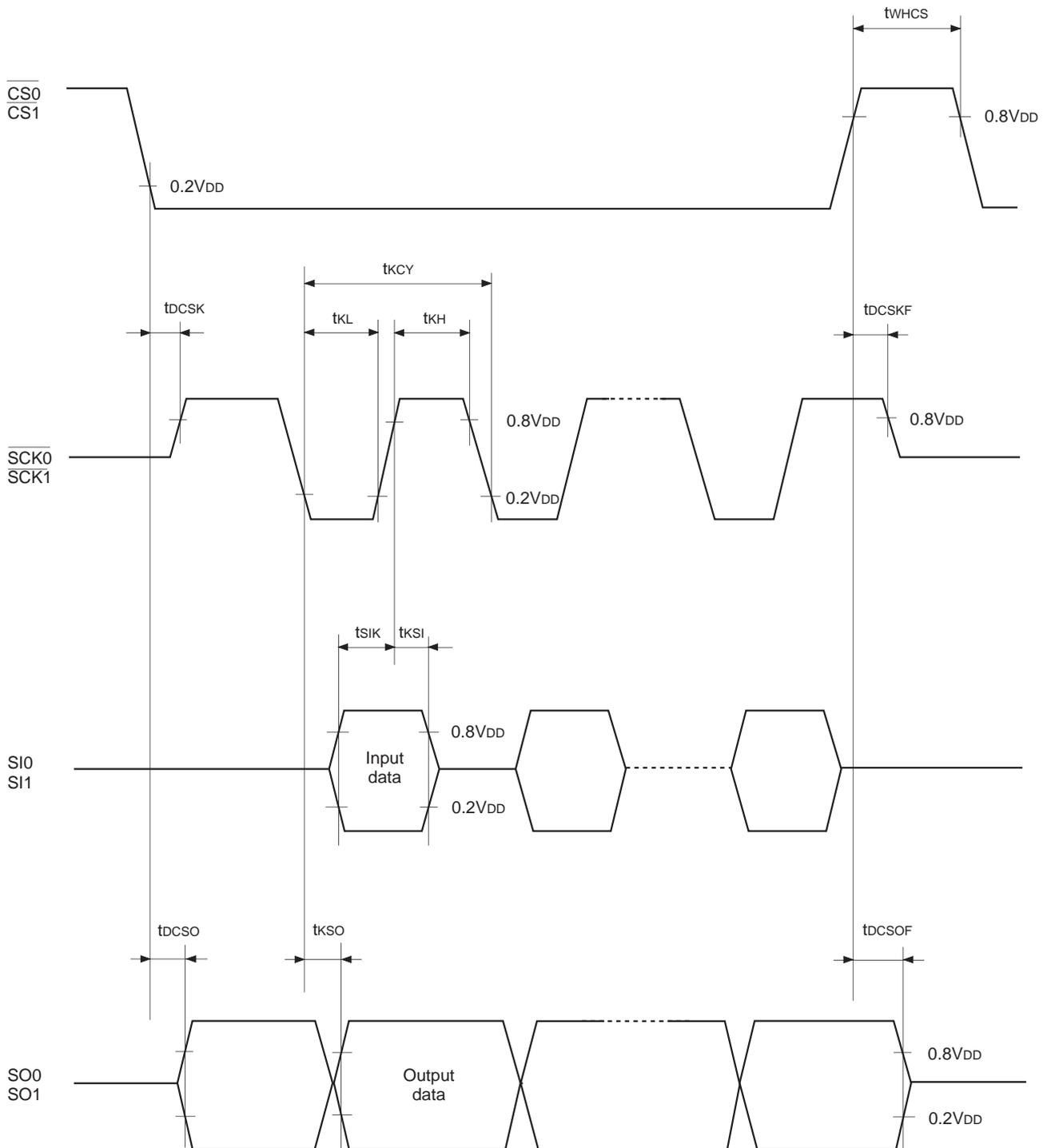| Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS}$ ↓ → $\overline{SCK}$ delay time	t_{DCSK}	$\overline{SCK0}$, $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = Output mode)		tsys + 200	ns
$\overline{CS}$ ↑ → $\overline{SCK}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$, $\overline{SCK1}$	Chip select transfer mode ($\overline{SCK}$ = Output mode)		tsys + 200	ns
$\overline{CS}$ ↓ → SO delay time	t_{DCSO}	SO0, SO1	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ ↑ → SO floating delay time	t_{DCSOF}	SO0, SO1	Chip select transfer mode		tsys + 200	ns
$\overline{CS}$ high level width	t_{WHCS}	CS0, CS1	Chip select transfer mode	tsys + 200		ns
$\overline{SCK}$ cycle time	t_{KCY}	$\overline{SCK0}$, $\overline{SCK1}$	Input mode	2tsys + 200		ns
			Output mode	8000/fc		ns
$\overline{SCK}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$, $\overline{SCK1}$	Input mode	tsys + 100		ns
			Output mode	4000/fc − 50		ns
SI input setup time (against $\overline{SCK}$ ↑)	t_{SIK}	SI0, SI1	$\overline{SCK}$ input mode	−tsys + 100		ns
			$\overline{SCK}$ output mode	200		ns
SI input hold time (against $\overline{SCK}$ ↑)	t_{KSI}	SI0, SI1	$\overline{SCK}$ input mode	2tsys + 100		ns
			$\overline{SCK}$ output mode	100		ns
$\overline{SCK}$ ↓ → SO delay time	t_{KSO}	SO0, SO1	$\overline{SCK}$ input mode		2tsys + 200	ns
			$\overline{SCK}$ output mode		100	ns

Note 1) tsys indicates three values according to the contents of the clock control register (address : 00FEH) upper 2 bits (CPU clock selection).

   tsys [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The marks $\overline{CS}$, $\overline{SCK}$, SI and SO respectivery mean pins of $\overline{CS}$ → $\overline{CS0}$, $\overline{CS1}$, $\overline{SCK}$ → $\overline{SCK0}$, $\overline{SCK1}$, SI → SI0, SI1 and SO → SO0, SO1.

Note 3) The load of $\overline{SCK}$ output mode and SO output delay time is 50pF + 1TTL.
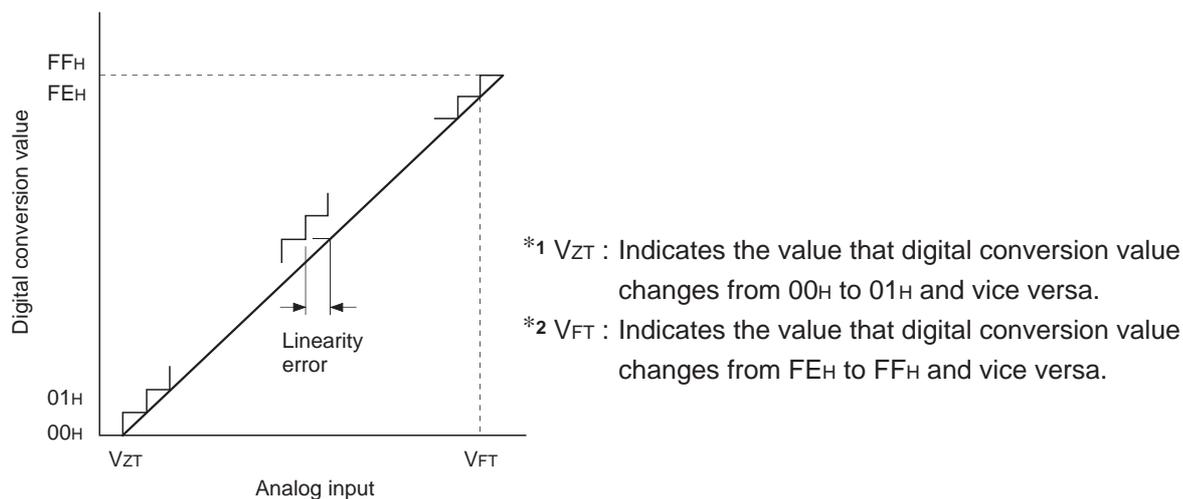
Fig. 4. Serial transfer timing

(3) A/D converter characteristics

(Ta = −20 to +75°C, V_{DD} = AV_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	bits
Linearity error						±1	LSB
Zero transition voltage	V_{ZT}*1		Ta = 25°C V_{DD} = AV_{DD} = 5.0V V_{SS} = AV_{SS} = 0V	−10	30	70	mV
Full scale transition voltage	V_{FT}*2			4930	4970	5010	mV
Conversion time	t_{CONV}			160/fc			µs
Sampling time	t_{SAMP}			12/fc			µs
Reference input voltage	V_{REF}	AV_{REF}		AV_{DD}−0.5		AV_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV$_{REF}$ current	I_{REF}	AV_{REF}	Operating mode		0.6	1.0	mA
	I_{REFS}		Sleep mode Stop mode			10	µA

Fig. 5. Definitions of A/D converter terms

*1 V_{ZT} : Indicates the value that digital conversion value changes from 00$_H$ to 01$_H$ and vice versa.

*2 V_{FT} : Indicates the value that digital conversion value changes from FE$_H$ to FF$_H$ and vice versa.

(4) Interruption, reset input (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t_{IH} t_{IL}	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$		1		µs
Reset input low level width	t_{RSL}	$\overline{RST}$		8/fc		µs

Fig. 6. Interruption input timing
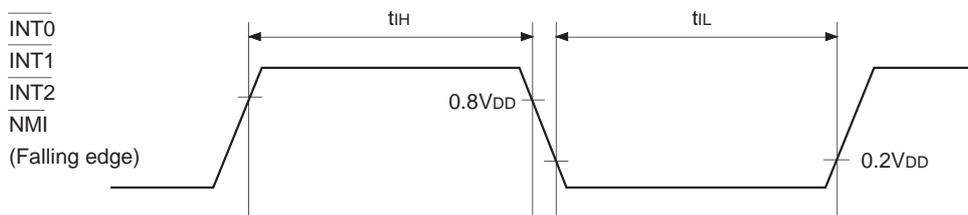
Fig. 7. $\overline{RST}$ input timing
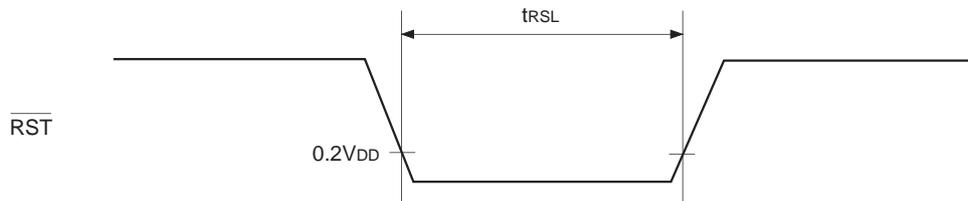
(5) Power on reset

Power on reset* (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
Power supply rising time	t_R	V_{DD}	Power on reset	0.05	50	ms
Power supply cut-off time	t_{OFF}		Repetitive power on reset	1		ms

* Specifies only when power on reset function is selected.

Fig. 8. Power on reset
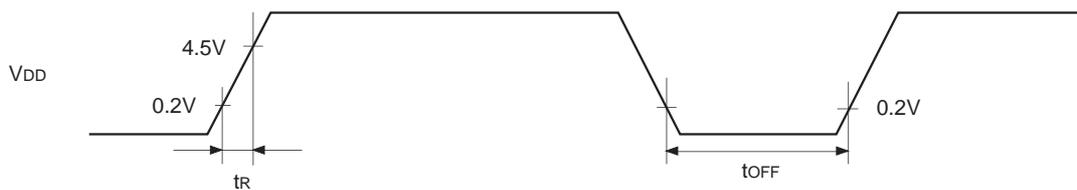

The power supply should rise smoothly.

(6) Others (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
RFDT input high and low level widths	t_{RDH} t_{RDL}	RFDT		$2.5t_{MCK}$[*1]		ns
MCLK input high and low level widths	t_{MCH} t_{MCL}	MCLK		326/fc		ns
DREF input high and low level widths	t_{DRH} t_{DRL}	DREF		t_{sys} + 200		ns
DPG input high and low level widths	t_{DPH} t_{DPL}	DPG		t_{sys} + 200		ns
DFG input high and low level widths	t_{DFH} t_{DFL}	DFG		t_{sys} + 200		ns
CFG input high and low level widths	t_{CFH} t_{CFL}	CFG		t_{sys} + 200		ns
RFG input high and low level widths	t_{RFH} t_{RFL}	RFG0 RFG1		t_{sys} + 200		ns
EXI input high and low level widths	t_{EIH} t_{EIL}	EXI0 EXI1	t_{sys} = 2000/fc	t_{sys} + 200		ns

[*1] t_{MCK} indicates three values according to the contents of the ATF control register (address : 01EE$_H$) bits 5 and 4 (MCLK input control).

t_{MCK} [ns] = t_{MCH} or t_{MCL} (bits 5 and 4 = "00"), $2t_{MCH}$ or $2t_{MCL}$ (bits 5 and 4 = "01"), $4t_{MCH}$ or $4t_{MCL}$ (bits 5 and 4 = "10").

Fig. 9. Other timing
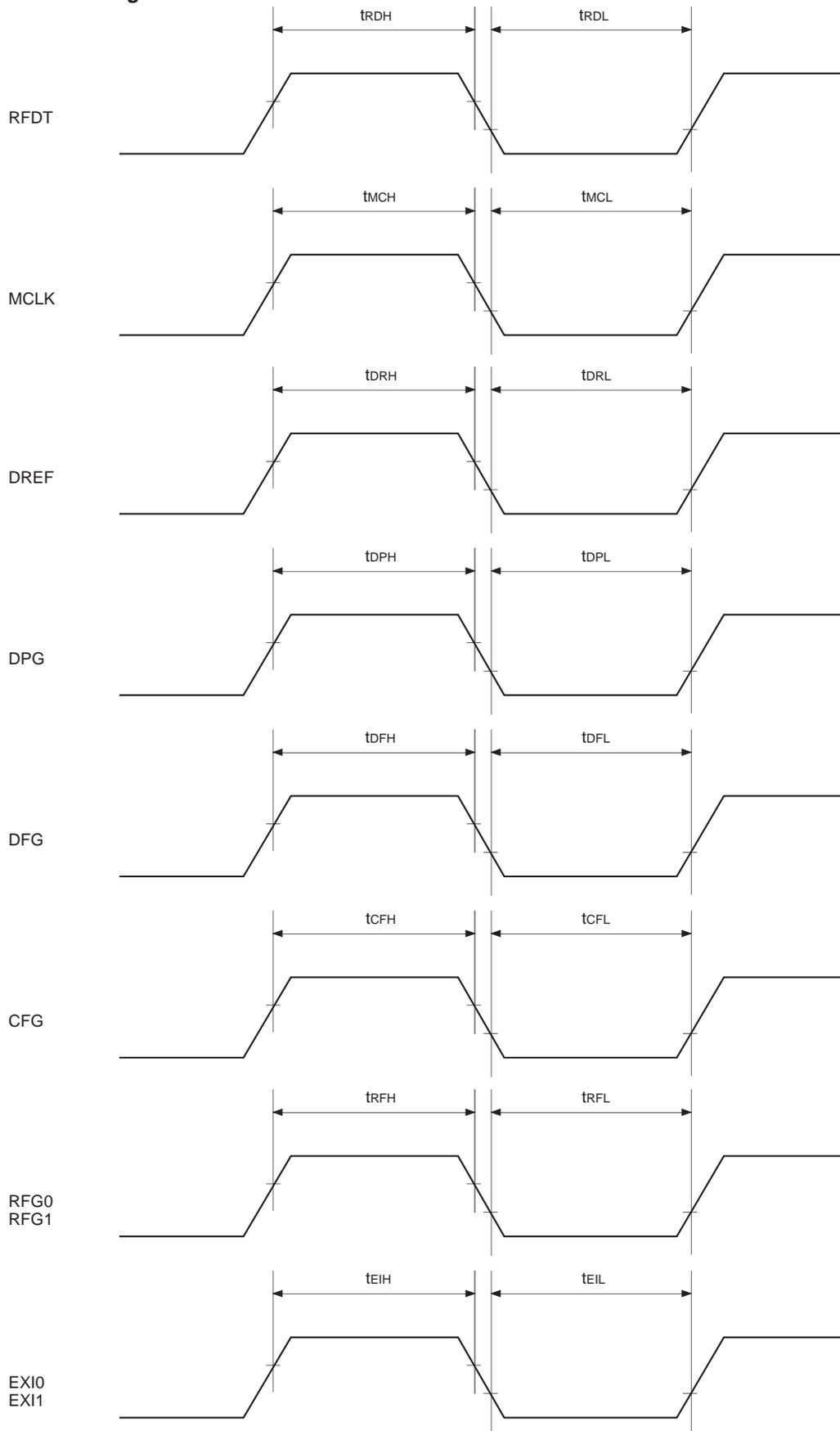
(7) Buffer amplifier function   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

| Item	Symbol	Pin	Condition	Min.	Max.	Unit
Buffer amplifier input voltage[*1] (Peak to peak value)	V_{APP}	RFDT	When inputting 400kHz sine wave on Fig. 10 circuit.	2.0	V_{DD} + 0.3	V

[*1] When buffer amplifier input circuit format of RFDT pin is selected with option.

Fig. 10.

V_{APP} (Refer to Fig. 11.)

C

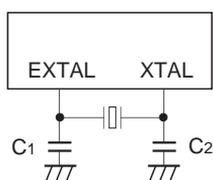V_{DD}

RFDT   C: 4700pF (±5%)

V_{SS}
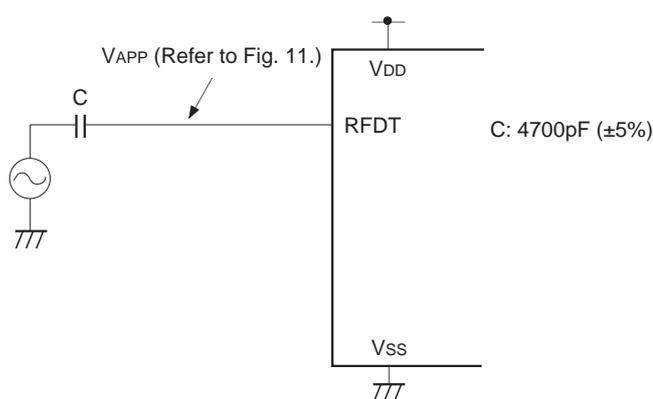
Note) V_{APP} waveform indicates the range like Fig. 11. When composed by circuits other than Fig. 10. (when DC bias does not become V_{DD}/2), it should not exceed V_{DD} + 0.3 (V) and −0.3 (V) (V_{SS} = 0V).

Fig. 11.

V_{APP}

V_{DD}/2
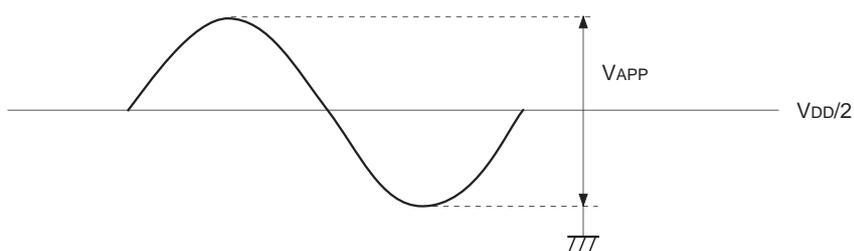
Supplement

Fig. 12. SPC700 series recommended oscillation circuit

Manufacturer	Model	Frequency f (MHz)	C_1, C_2 (pF)
RIVER ELETEC CORPORATION	HC-49/U-03	6.00	12
		8.00	12
		12.000	10

Mask option table

| Item	Contents	
Reset pin pull-up resistor	Non-existent	Existent
Power on reset circuit	Non-existent	Existent
Input circuit format[*1]	CMOS Schmitt	TTL Schmitt
	Buffer amplifier	Normal input

[*1] On PG0/EXI0 pin to PG7/RFG1 pin and PK1/MCLK pin, the input circuit format of CMOS schmitt or TTL schmitt can be selected to every pin.
On PK0/RFDT pin, buffer amplifier or normal input circuit format can be selected.

Package Outline   Unit: mm
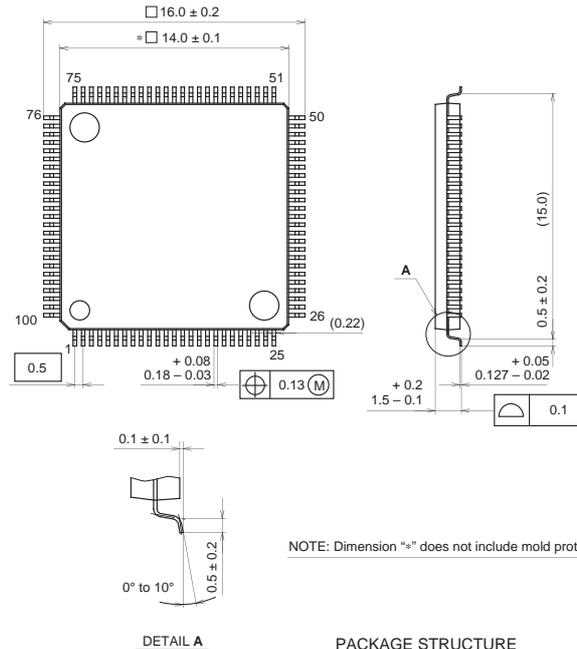
100PIN QFP (PLASTIC)
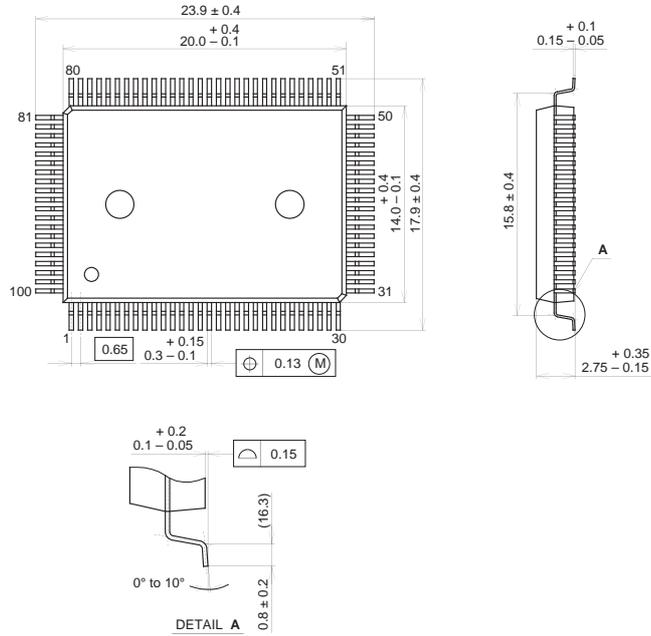
SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

100PIN LQFP (PLASTIC)

NOTE: Dimension "∗" does not include mold protrusion.

SONY CODE	LQFP-100P-L01
EIAJ CODE	LQFP100-P-1414
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.8g