



SCCS061 - July 1994 - Revised March 2000

CY74FCT16652T CY74FCT162652T

16-Bit Registered Transceivers

Features

- FCT-E speed at 3.8 ns
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V_{CC} = 5V ± 10%

CY74FCT16652T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C

CY74FCT162652T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C

Functional Description

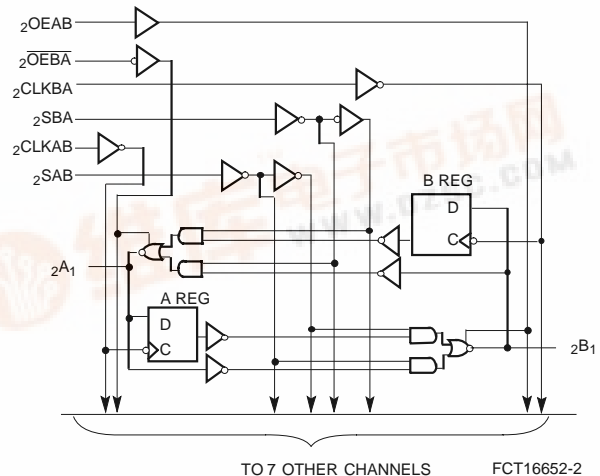
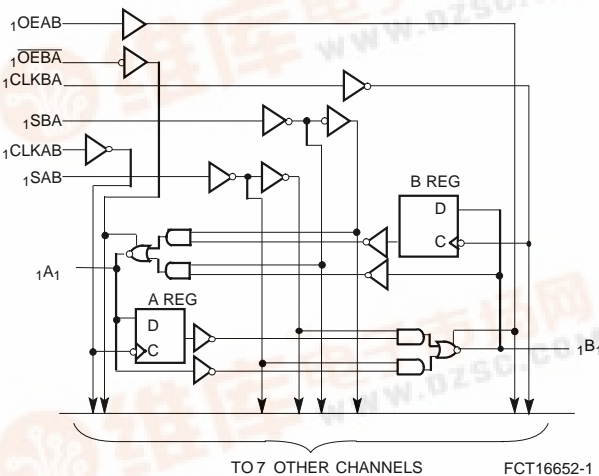
These 16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and OEBA control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and OEBA. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. The output buffers are designed with a power-off disable feature that allows live insertion of boards.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.

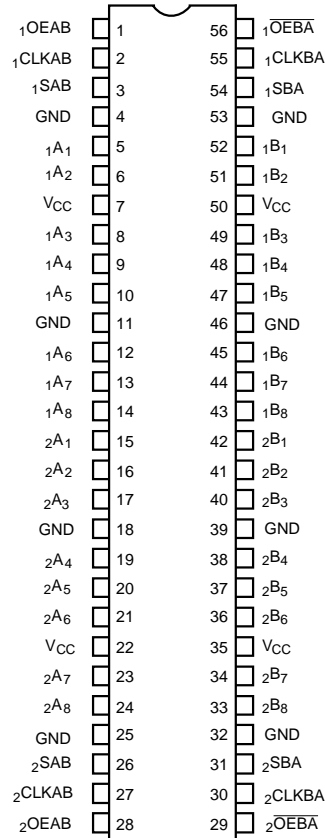
Logic Block Diagrams



Pin Configuration

SSOP/TSSOP

Top View



FCT16652-3

Pin Description

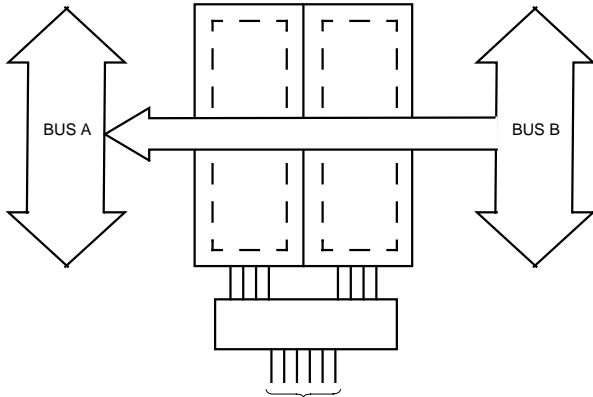
| Name | Description |
|-------------------------|---|
| A | Data Register A Inputs Data Register B Outputs |
| B | Data Register B Inputs Data Register A Outputs |
| CLKAB, CLKBA | Clock Pulse Inputs |
| SAB, SBA | Output Data Source Select Inputs |
| OEAB, \overline{OEBA} | Output Enable Inputs |

Function Table^[1]

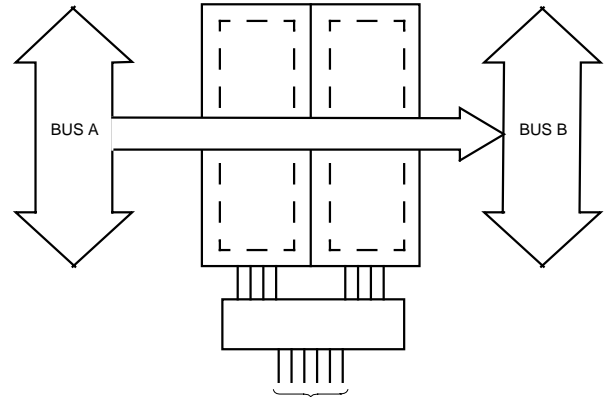
| Inputs | | | | | | Data I/O ^[2] | | Operation or Function |
|--------|--------------------------|-------------|-------------|-----------------------|-----------------------|----------------------------|--------------------------------------|--|
| OEAB | $\overline{\text{OEBA}}$ | CLKAB | CLKBA | SAB | SBA | A | B | |
| L L | H H | H or L ┐ | H or L ┐ | X X | X X | Input | Input | Isolation Store A and B Data |
| X H | H H | ┐ ┐ | H or L ┐ | X X ^[3] | X X | Input Input | Unspecified ^[2] Output | Store A, Hold B Store A in Both Registers |
| L L | X L | H or L ┐ | ┐ ┐ | X X | X X ^[3] | Unspecified ^[2] | Input Input | Hold A, Store B Store B in both Registers |
| L L | L L | X X | X H or L | X X | L H | Output | Input | Real Time B Data to A Bus Stored B Data to A Bus |
| H H | H H | X H or L | X X | L H | X X | Input | Output | Real Time A Data to B Bus Stored A Data to B Bus |
| H | L | H or L | H or L | H | H | Output | Output | Stored A Data to B Bus and Stored B Data to A Bus |

Notes:

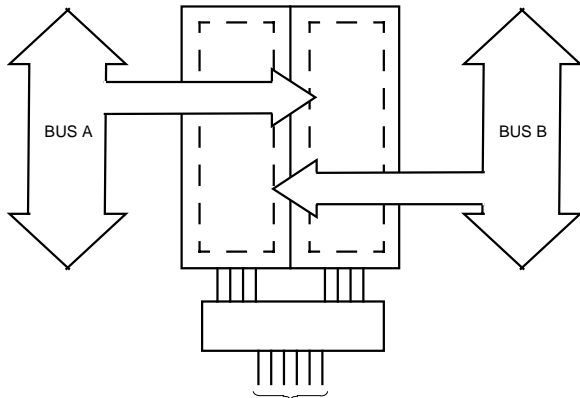
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
┐ = LOW-to-HIGH Transition
- The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
- Select control=L; clocks can occur simultaneously.
Select control=H; clocks must be staggered to load both registers.



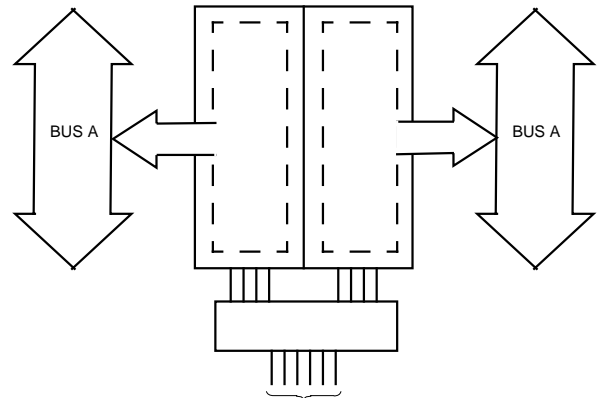
OEAB L $\overline{\text{OEBA}}$ L CLKAB X CLKBA X SAB X SBA L
**Real-Time Transfer
Bus B to Bus A**



OEAB H $\overline{\text{OEBA}}$ L CLKAB X CLKBA X SAB L SBA X
**Real-Time Transfer
Bus A to Bus B**



OEAB X $\overline{\text{OEBA}}$ H CLKAB \downarrow CLKBA \downarrow SAB X SBA X
 L X X X X X
**Storage from
A and/or B**



OEAB H $\overline{\text{OEBA}}$ L CLKAB H or L CLKBA H or L SAB H SBA H
**Transfer Stored Data
to A and/or B**

Maximum Ratings^[4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage TemperatureCom'l -55°C to +125°C

Ambient Temperature with
Power AppliedCom'l -55°C to +125°C

DC Input Voltage-0.5V to +7.0V

DC Output Voltage-0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin)-60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V
(per MIL-STD-883, Method 3015)

Operating Range

| Range | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40°C to +85°C | 5V ± 10% |

Note:

- Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions ^[5] | Min. | Typ. ^[6] | Max. | Unit |
|------------------|--|--|------|---------------------|------|------|
| V _{IH} | Input HIGH Voltage | Logic HIGH Level | 2.0 | | | V |
| V _{IL} | Input LOW Voltage | Logic LOW Level | | | 0.8 | V |
| V _H | Input Hysteresis | | | 100 | | mV |
| V _{IK} | Input Clamp Diode Voltage | V _{CC} =Min., I _{IN} =-18 mA | | -0.7 | -1.2 | V |
| I _{IH} | Input HIGH Current | V _{CC} =Max., V _I =V _{CC} | | | ±1 | μA |
| I _{IL} | Input LOW Current | V _{CC} =Max., V _I =GND | | | ±1 | μA |
| I _{OZH} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =2.7V | | | ±1 | μA |
| I _{OZL} | High Impedance Output Current (Three-State Output pins) | V _{CC} =Max., V _{OUT} =0.5V | | | ±1 | μA |
| I _{OS} | Short Circuit Current ^[8] | V _{CC} =Max., V _{OUT} =GND | -80 | -140 | -200 | mA |
| I _O | Output Drive Current ^[8] | V _{CC} =Max., V _{OUT} =2.5V | -50 | | -180 | mA |
| I _{OFF} | Power-Off Disable | V _{CC} =0V, V _{OUT} ≤4.5V ^[7] | | | ±1 | μA |

Output Drive Characteristics for CY74FCT16652T

| Parameter | Description | Test Conditions ^[5] | Min. | Typ. ^[6] | Max. | Unit |
|-----------------|---------------------|--|------|---------------------|------|------|
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-3 mA | 2.5 | 3.5 | | V |
| | | V _{CC} =Min., I _{OH} =-15 mA | 2.4 | 3.5 | | |
| | | V _{CC} =Min., I _{OH} =-32 mA | 2.0 | 3.0 | | |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =64 mA | | 0.2 | 0.55 | V |

Output Drive Characteristics for CY74FCT162652T

| Parameter | Description | Test Conditions ^[5] | Min. | Typ. ^[6] | Max. | Unit |
|------------------|------------------------------------|---|------|---------------------|------|------|
| I _{ODL} | Output LOW Current ^[8] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | 60 | 115 | 150 | mA |
| I _{ODH} | Output HIGH Current ^[8] | V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V | -60 | -115 | -150 | mA |
| V _{OH} | Output HIGH Voltage | V _{CC} =Min., I _{OH} =-24 mA | 2.4 | 3.3 | | V |
| V _{OL} | Output LOW Voltage | V _{CC} =Min., I _{OL} =24 mA | | 0.3 | 0.55 | V |

Capacitance (T_A = +25°C, f = 1.0 MHz)

| Parameter | Description ^[10] | Test Conditions | Typ. | Max. | Unit |
|------------------|-----------------------------|-----------------------|------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 4.5 | 6.0 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 5.5 | 8.0 | pF |

Notes:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC}=5.0V, +25°C ambient.
- Tested at T_A= +25°C.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Duration of the condition cannot exceed one second.
- This parameter is measured at characterization but not tested.

Power Supply Characteristics

| Param. | Description | Test Conditions ^[11] | | Min. | Typ. ^[12] | Max. | Unit |
|------------------|---|--|---|------|----------------------|----------------------|------------|
| I _{CC} | Quiescent Power Supply Current | V _{CC} =Max. | V _{IN} ≤0.2V V _{IN} ≥V _{CC} -0.2V | — | 5 | 500 | μA |
| ΔI _{CC} | Quiescent Power Supply Current TTL Inputs HIGH | V _{CC} = Max. V _{IN} =3.4V ^[13] | | — | 0.5 | 1.5 | mA |
| I _{CCD} | Dynamic Power Supply Current ^[14] | V _{CC} =Max. Outputs Open OEAB=OEAB=GND One Input Toggling 50% Duty Cycle | V _{IN} =V _{CC} or V _{IN} =GND | — | 75 | 120 | μA/ MHz |
| I _C | Total Power Supply Current ^[15] | V _{CC} =Max. Outputs Open f ₀ =10 MHz (CLKBA) 50% Duty Cycle OEAB=OEBA=GND One-Bit Toggling f ₁ =5 MHz 50% Duty Cycle | V _{IN} =V _{CC} or V _{IN} =GND | — | 0.8 | 1.7 | mA |
| | | | V _{IN} =3.4V or V _{IN} =GND | — | 1.3 | 3.2 | mA |
| | | V _{CC} =Max. Outputs Open f ₀ =10 MHz (CLKBA) 50% Duty Cycle OEAB=OEBA=GND Sixteen Bits Toggling f ₁ =2.5 MHz 50% Duty Cycle | V _{IN} =V _{CC} or V _{IN} =GND | — | 3.8 | 6.5 ^[16] | mA |
| | | | V _{IN} =3.4V or V _{IN} =GND | — | 8.3 | 20.0 ^[16] | mA |

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at V_{CC}=5.0V +25° ambient.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[17]

| Parameter | Description | CY74FCT16652AT CY74FCT162652AT | | Unit | Fig. No. ^[18] |
|--------------------------------------|--|-----------------------------------|------|------|--------------------------|
| | | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Bus to Bus | 1.5 | 6.3 | ns | 1, 3 |
| t _{PZH} t _{PHL} | Output Enable Time OEAB or \overline{OEBA} to Bus | 1.5 | 9.8 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time OEAB or \overline{OEBA} to Bus | 1.5 | 6.3 | ns | 1, 7, 8 |
| t _{PLH} t _{PHL} | Propagation Delay Clock to Bus | 1.5 | 6.3 | ns | 1, 5 |
| t _{PLH} t _{PHL} | Propagation Delay SBA or SAB to Bus | 1.5 | 7.7 | ns | 1, 5 |
| t _{SU} | Set-Up time HIGH or LOW Bus to Clock | 2.0 | — | ns | 4 |
| t _H | Hold Time HIGH or LOW Bus to Clock | 1.5 | — | ns | 4 |
| t _W | Clock Pulse Width HIGH or LOW | 5.0 | — | ns | 5 |
| t _{SK(O)} | Output Skew ^[19] | — | 0.5 | ns | |

| Parameter | Description | CY74FCT16652CT CY74FCT162652CT | | CY74FCT16652ET CY74FCT162652ET | | Unit | Fig. No. ^[18] |
|--------------------------------------|---|-----------------------------------|------|-----------------------------------|------|------|--------------------------|
| | | Min. | Max. | Min. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay Bus to Bus | 1.5 | 5.4 | 1.5 | 3.8 | ns | 1, 3 |
| t _{PZH} t _{PHL} | Output Enable Time OEAB or \overline{OEBA} to Bus | 1.5 | 7.8 | 1.5 | 4.8 | ns | 1, 7, 8 |
| t _{PHZ} t _{PLZ} | Output Disable Time OEAB or \overline{OEBA} to Bus | 1.5 | 6.3 | 1.5 | 4.0 | ns | 1, 7, 8 |
| t _{PLH} t _{PHL} | Propagation Delay Clock to Bus | 1.5 | 5.7 | 1.5 | 3.8 | ns | 1, 5 |
| t _{PLH} t _{PHL} | Propagation Delay SBA or SAB to Bus | 1.5 | 6.2 | 1.5 | 4.2 | ns | 1, 5 |
| t _{SU} | Set-Up Time HIGH or LOW Bus to Clock | 2.0 | — | 2.0 | — | ns | 4 |
| t _H | Hold Time HIGH or LOW Bus to Clock | 1.5 | — | 0.0 | — | ns | 4 |
| t _W | Clock Pulse Width HIGH or LOW | 5.0 | — | 3.0 | — | ns | 5 |
| t _{SK(O)} | Output Skew ^[19] | — | 0.5 | — | 0.5 | ns | |

Notes:

17. Minimum limits are specified, but not tested, on propagation delays.

18. See "Parameter Measurement Information" in the General Information section.

19. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT16652

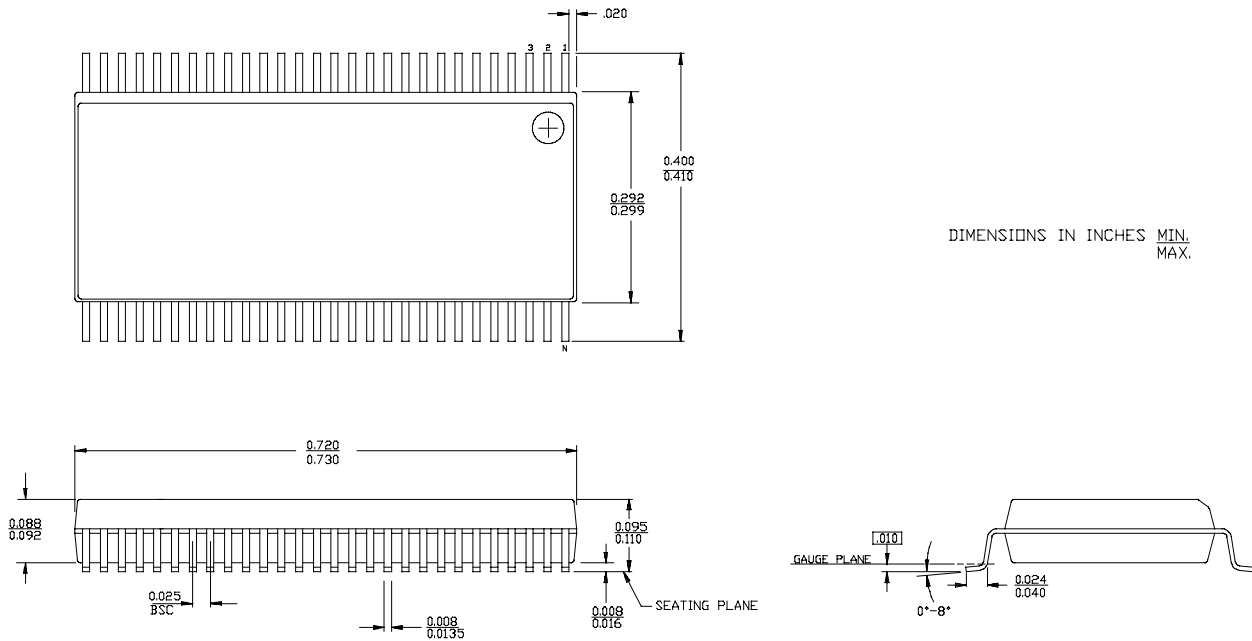
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|------------------------|--------------|-------------------------|-----------------|
| 3.8 | CY74FCT16652ETPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT16652ETPVC/PVCT | O56 | 56-Lead (300-Mil) SSOP | |
| 5.4 | CY74FCT16652CTPVC/PVCT | O56 | 56-Lead (300-Mil) SSOP | Industrial |
| 6.3 | CY74FCT16652ATPVC/PVCT | O56 | 56-Lead (300-Mil) SSOP | Industrial |

Ordering Information CY74FCT162652

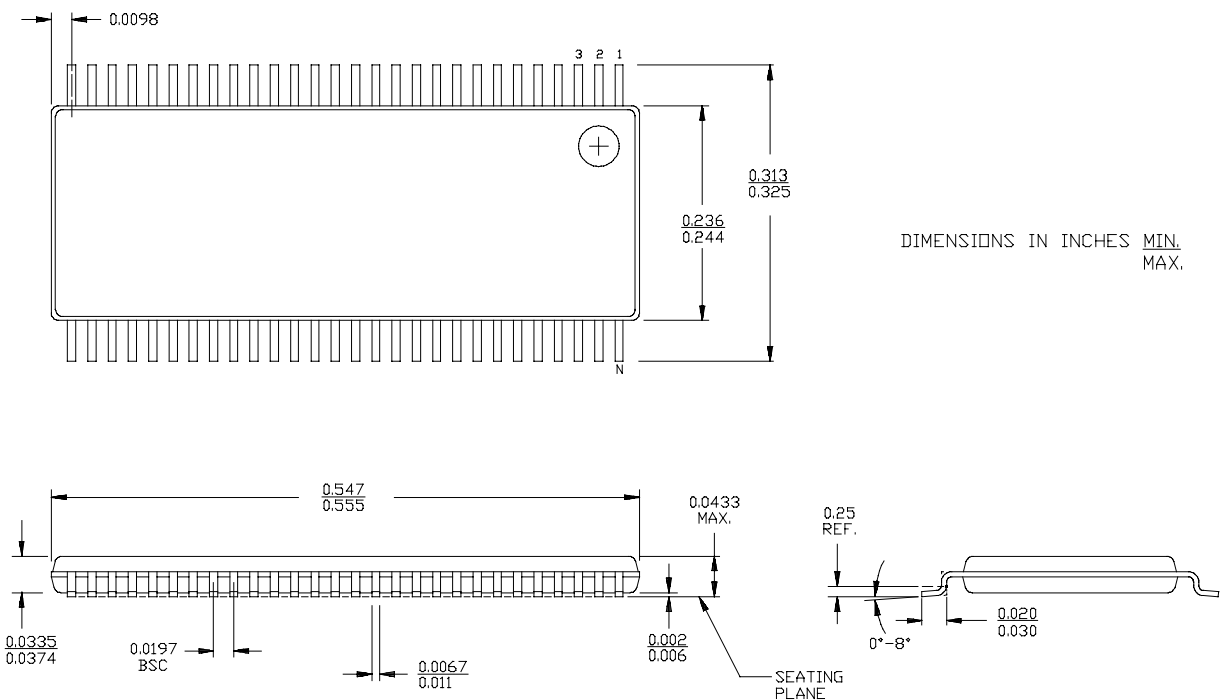
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|--------------------|--------------|-------------------------|-----------------|
| 3.8 | 74FCT162652ETPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162652ETPVC | O56 | 56-Lead (300-Mil) SSOP | |
| | 74FCT162652ETPVCT | O56 | 56-Lead (300-Mil) SSOP | |
| 5.4 | 74FCT162652CTPACT | Z56 | 56-Lead (240-Mil) TSSOP | Industrial |
| | CY74FCT162652CTPVC | O56 | 56-Lead (300-Mil) SSOP | |
| | 74FCT162652CTPVCT | O56 | 56-Lead (300-Mil) SSOP | |
| 6.3 | CY74FCT162652ATPVC | O56 | 56-Lead (300-Mil) SSOP | Industrial |
| | 74FCT162652ATPVCT | O56 | 56-Lead (300-Mil) SSOP | |

Package Diagrams

56-Lead Shrunken Small Outline Package O56



56-Lead Thin Shrunken Small Outline Package Z56



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