



SCCS058 - March 1997 - Revised March 2000

## CY74FCT163646

### 16-Bit Registered Transceiver

#### Features

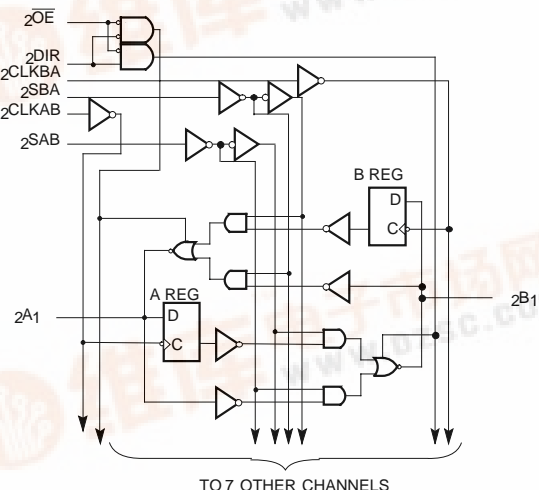
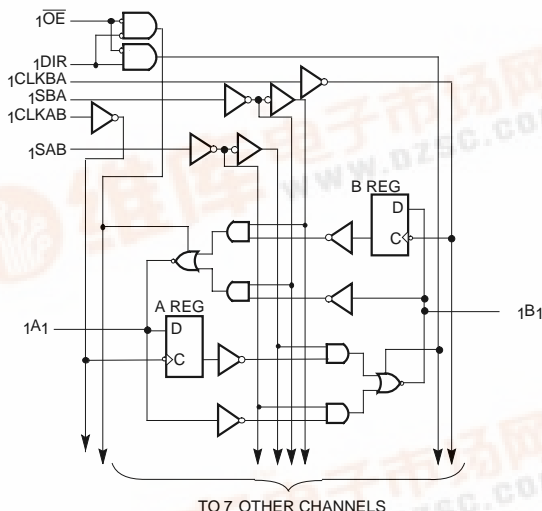
- Low power, pin-compatible replacement for LCX and LPT families
- 5V tolerant inputs and outputs
- 24 mA balanced drive outputs
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for reduced noise
- FCT-C speed at 5.4 ns
- Latch-up performance exceeds JEDEC standard no. 17
- ESD > 2000V per MIL-STD-883D, Method 3015
- Typical output skew < 250 ps
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- TSSOP (19.6-mil pitch) or SSOP (25-mil pitch)
- Typical  $V_{OLP}$  (ground bounce) performance exceeds Mil Std 883D
- $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$

#### Functional Description

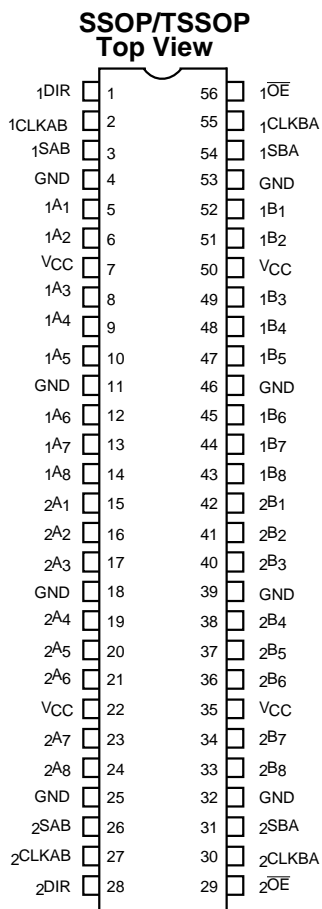
The CY74FCT163646 16-bit transceiver is a three-state, D-type register, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes to a HIGH logic level. Output Enable ( $\overline{OE}$ ) and direction pins (DIR) are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register, or in both. The select controls can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the Output Enable ( $\overline{OE}$ ) is Active LOW. In the isolation mode (Output Enable ( $\overline{OE}$ ) HIGH), A data may be stored in the B register and/or B data may be stored in the A register.

The CY74FCT163646 has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The inputs and outputs were designed to be capable of being driven by 5.0V buses, allowing them to be used in mixed voltage systems as translators. The outputs are also designed with a power-off disable feature enabling them to be used in applications requiring live insertion.

#### Logic Block Diagrams



## Pin Configuration



## Pin Description

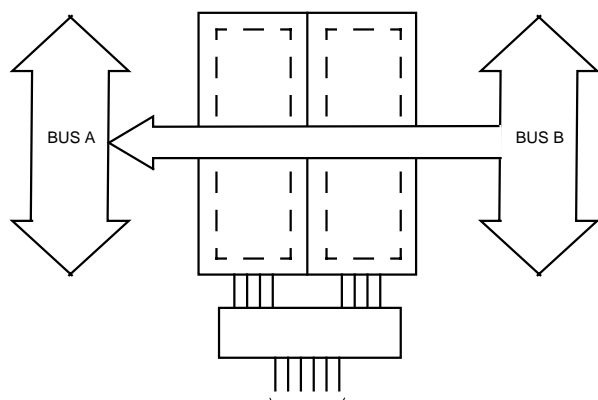
Pin Names	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR	Direction
$\overline{O}E$	Output Enable (Active LOW)

## Function Table<sup>[1]</sup>

Inputs						Data I/O <sup>[2]</sup>		Function
$\overline{O}E$	DIR	CLKAB	CLKBA	SAB	SBA	A	B	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	$\text{┐}$	$\text{┐}$	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

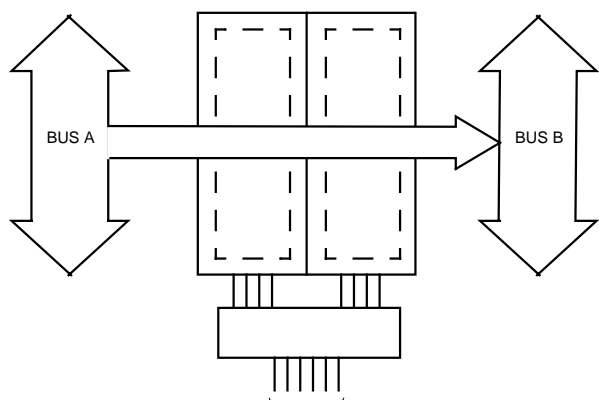
### Notes:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care,  $\text{┐}$  = LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the  $\overline{O}E$  or DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.



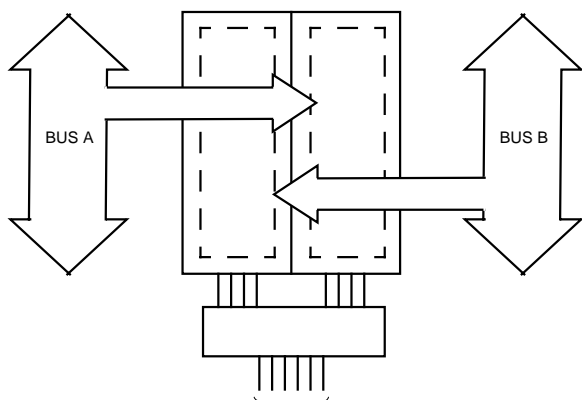
DIR L     $\overline{\text{OE}}$  L    CLKAB X    CLKBA X    SAB X    SBA L

Real-Time Transfer  
Bus B to Bus A



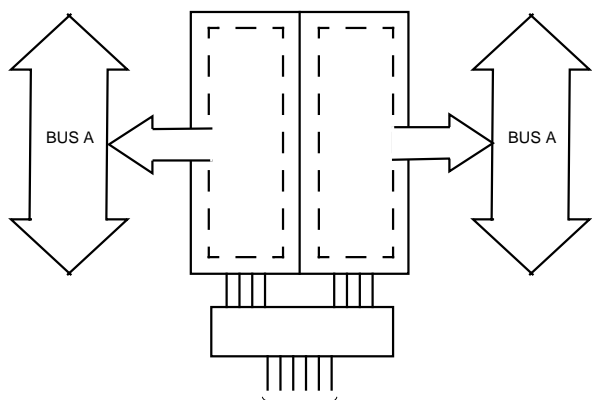
DIR H     $\overline{\text{OE}}$  L    CLKAB X    CLKBA X    SAB L    SBA X

Real-Time Transfer  
Bus A to Bus B



DIR H L X     $\overline{\text{OE}}$  L L H    CLKAB X L    CLKBA X L    SAB X X X    SBA X X X

Storage from  
A and/or B



DIR<sup>[3]</sup> L H     $\overline{\text{OE}}$  L L    CLKAB X H or L    CLKBA H or L X    SAB X H    SBA H X

Transfer Stored Data  
to A and/or B

## Maximum Ratings<sup>[4]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -55°C to +125°C  
Ambient Temperature with  
Power Applied ..... -55°C to +125°C  
Supply Voltage Range ..... 0.5V to +4.6V  
DC Input Voltage ..... -0.5V to +7.0V  
DC Output Voltage ..... -0.5V to +7.0V

## DC Output Current

(Maximum Sink Current/Pin) ..... -60 to +120 mA  
Power Dissipation ..... 1.0W  
Static Discharge Voltage..... >2001V  
(per MIL-STD-883, Method 3015)

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	2.7V to 3.6V

### Notes:

- Cannot transfer data to A-bus and B-bus simultaneously.
- Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Electrical Characteristics** Over the Operating Range  $V_{CC}=2.7V$  to  $3.6V$ 

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
$V_{IH}$	Input HIGH Voltage	All Inputs	2.0		5.5	V
$V_{IL}$	Input LOW Voltage				0.8	V
$V_H$	Input Hysteresis <sup>[6]</sup>			100		mV
$V_{IK}$	Input Clamp Diode Voltage	$V_{CC}=\text{Min.}$ , $I_{IN}=-18\text{ mA}$		-0.7	-1.2	V
$I_{IH}$	Input HIGH Current	$V_{CC}=\text{Max.}$ , $V_I=5.5V$			$\pm 1$	$\mu A$
$I_{IL}$	Input LOW Current	$V_{CC}=\text{Max.}$ , $V_I=\text{GND}$			$\pm 1$	$\mu A$
$I_{OZH}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$ , $V_{OUT}=5.5V$			$\pm 1$	$\mu A$
$I_{OZL}$	High Impedance Output Current (Three-State Output pins)	$V_{CC}=\text{Max.}$ , $V_{OUT}=\text{GND}$			$\pm 1$	$\mu A$
$I_{ODL}$	Output LOW Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	45		180	mA
$I_{ODH}$	Output HIGH Dynamic Current <sup>[7]</sup>	$V_{CC}=3.3V$ , $V_{IN}=V_{IH}$ or $V_{IL}$ , $V_{OUT}=1.5V$	-45		-180	mA
$V_{OH}$	Output HIGH Voltage	$V_{CC}=\text{Min.}$ , $I_{OH}=-0.1\text{ mA}$	$V_{CC}-0.2$			V
		$V_{CC}=3.0V$ , $I_{OH}=-8\text{ mA}$	2.4 <sup>[8]</sup>	3.0		
		$V_{CC}=3.0V$ , $I_{OH}=-24\text{ mA}$	2.0	3.0		
$V_{OL}$	Output LOW Voltage	$V_{CC}=\text{Min.}$ , $I_{OL}=0.1\text{ mA}$			0.2	V
		$V_{CC}=\text{Min.}$ , $I_{OL}=24\text{ mA}$		0.3	0.5	
$I_{OS}$	Short Circuit Current <sup>[7]</sup>	$V_{CC}=\text{Max.}$ , $V_{OUT}=\text{GND}$	-60	-135	-240	mA
$I_{OFF}$	Power-Off Disable	$V_{CC}=0V$ , $V_{OUT}\leq 4.5V$			$\pm 100$	$\mu A$

**Capacitance<sup>[5]</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Symbol	Description <sup>[9]</sup>	Conditions	Typ.	Max.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6.0	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8.0	pF

**Notes:**

- Typical values are at  $V_{CC}=3.3V$ ,  $T_A=+25^\circ\text{C}$  ambient.
- This parameter is specified but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametrics tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.
- $V_{OH}=V_{CC}-0.6\text{ V}$  at rated current.
- This parameter is measured at characterization but not tested.

**Power Supply Characteristics**

Parameter	Description	Test Conditions		Typ. <sup>[5]</sup>	Max.	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$	0.1	10	$\mu A$
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{[10]}$	2.0	30	$\mu A$
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC} = \text{Max.}$ , Outputs Open DIR=OE=GND One-Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	50	75	$\mu A/\text{MHz}$
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_0 = 10 \text{ MHz}$ (CLKBA) 50% Duty Cycle DIR=OE=GND One-Bit Toggling, $f_1 = 5 \text{ MHz}$ , 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ or $V_{IN} = \text{GND}$	0.5	0.8	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_0 = 10 \text{ MHz}$ (CLKBA) 50% Duty Cycle DIR=OE=GND Sixteen-Bits Toggling $f_1 = 2.5 \text{ MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ or $V_{IN} = \text{GND}$	2.5	3.8 <sup>[13]</sup>	
			$V_{IN} = V_{CC} - 0.6V$ or $V_{IN} = \text{GND}$	2.6	4.1 <sup>[13]</sup>	

**Notes:**

10. Per TTL driven input); all other inputs at  $V_{CC}$  or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_0 N_C / 2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $N_C$  = Number of clock inputs changing at  $f_1$   
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range  $V_{CC}=3.0V$  to  $3.6V$ <sup>[14,15]</sup>

Parameter	Description	CY74FCT163646C		Unit	Fig. No. <sup>[16]</sup>
		Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Bus to Bus	1.5	5.4	ns	1, 2
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR or $\overline{OE}$ to Bus	1.5	7.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR or $\overline{OE}$ to Bus	1.5	6.3	ns	1, 7, 8
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Clock to Bus	1.5	5.7	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay SBA or SAB to Bus	1.5	6.2	ns	1,5
t <sub>SU</sub>	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	ns	4
t <sub>H</sub>	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t <sub>W</sub>	Clock Pulse Width HIGH or LOW	5.0	—	ns	6
t <sub>SK(O)</sub>	Output Skew <sup>[17]</sup>	—	0.5	ns	—

**Ordering Information CY74FCT163646**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT163646CPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT163646CPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

**Notes:**

14. Minimum limits are specified but not tested on Propagation Delays.

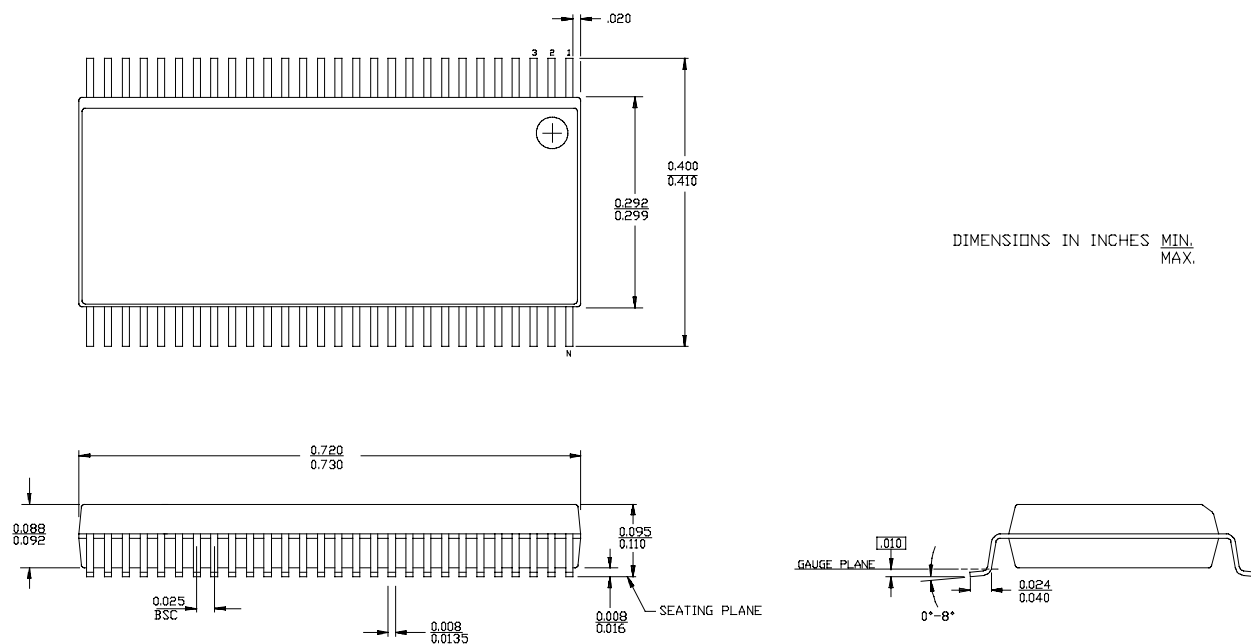
15. For  $V_{CC}=2.7$ , propagation delay, output enable and output disable times should be degraded by 20%.

16. See "Parameter Measurement Information" in the General Information section.

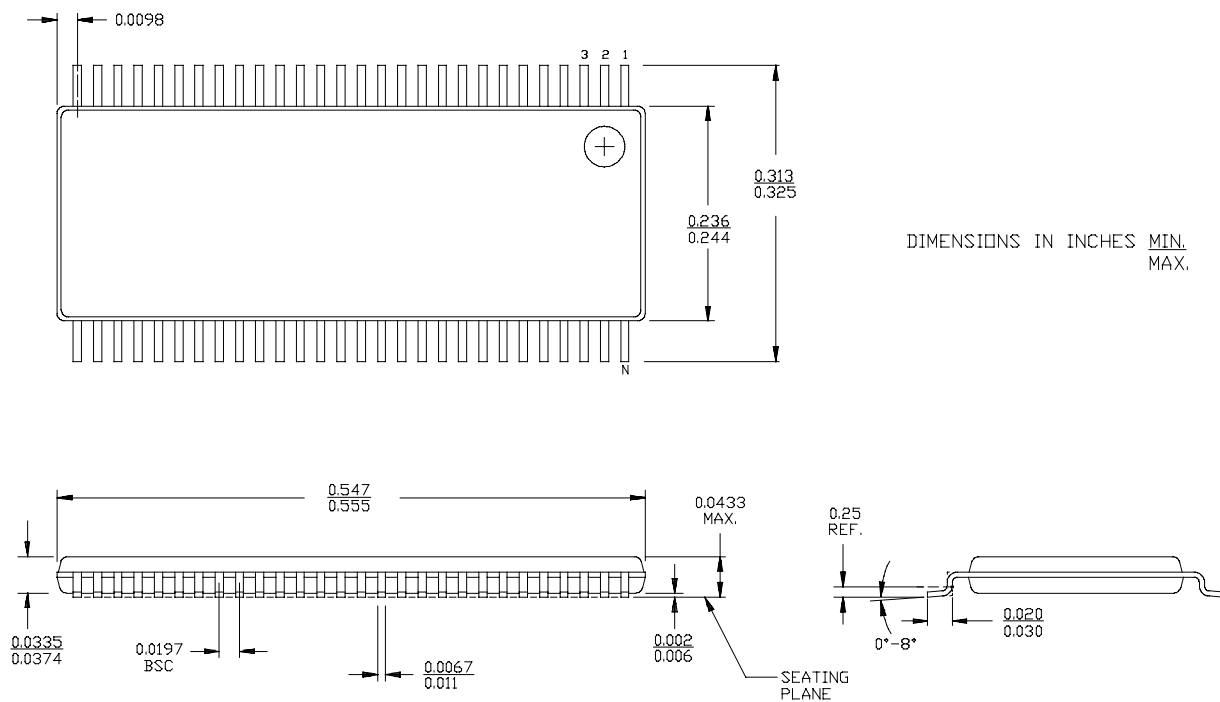
17. Skew any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Package Diagrams**

**56-Lead Shrunk Small Outline Package O56**



**56-Lead Thin Shrunk Small Outline Package Z56**



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