

# 16-Mbit (1M x 16) Static RAM

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 990 mW (max.)
- Operating voltages of  $3.3 \pm 0.3V$
- 2.0V data retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Available in Pb-free and non Pb-free 54-pin TSOP II package

## Functional Description

The CY7C1061BV33 is a high-performance CMOS Static RAM organized as 1,048,576 words by 16 bits.

Writing to the device is accomplished by enabling the chip ( $\overline{CE}$  LOW) while forcing the Write Enable ( $\overline{WE}$ ) input LOW. If Byte

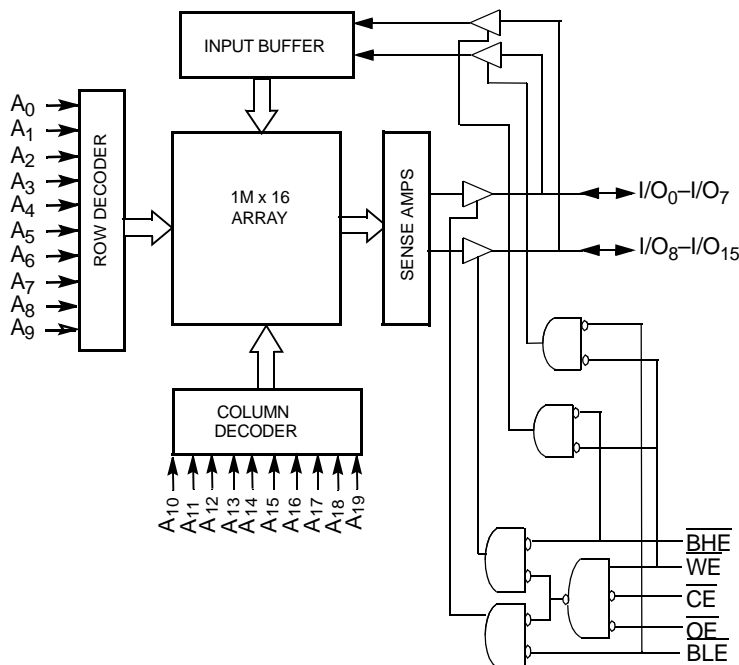
Low Enable ( $\overline{BLE}$ ) is LOW, then data from I/O pins ( $I/O_0$  through  $I/O_7$ ), is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from I/O pins ( $I/O_8$  through  $I/O_{15}$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

Reading from the device is accomplished by enabling the chip by taking  $\overline{CE}$  LOW while forcing the Output Enable ( $\overline{OE}$ ) LOW and the Write Enable ( $\overline{WE}$ ) HIGH. If Byte Low Enable ( $\overline{BLE}$ ) is LOW, then data from the memory location specified by the address pins will appear on  $I/O_0$  to  $I/O_7$ . If Byte High Enable ( $\overline{BHE}$ ) is LOW, then data from memory will appear on  $I/O_8$  to  $I/O_{15}$ . See the truth table at the back of this data sheet for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_{15}$ ) are placed in a high-impedance state when the device is deselected ( $\overline{CE}$  HIGH), the outputs are disabled ( $\overline{OE}$  HIGH), the  $\overline{BHE}$  and  $\overline{BLE}$  are disabled ( $\overline{BHE}$ ,  $\overline{BLE}$  HIGH), or during a Write operation ( $\overline{CE}$  LOW and  $\overline{WE}$  LOW).

The CY7C1061BV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

## Logic Block Diagram



## Pin Configurations<sup>[1, 2]</sup>

### 54-pin TSOP II (Top View)

$I/O_{12}$	1	54	$I/O_{11}$
$V_{CC}$	2	53	$V_{SS}$
$I/O_{13}$	3	52	$I/O_{10}$
$I/O_{14}$	4	51	$I/O_9$
$V_{SS}$	5	50	$V_{CC}$
$I/O_{15}$	6	49	$I/O_8$
$A_4$	7	48	$A_5$
$A_3$	8	47	$A_6$
$A_2$	9	46	$A_7$
$A_1$	10	45	$A_8$
$A_0$	11	44	$A_9$
$\overline{BHE}$	12	43	NC
$\overline{CE}$	13	42	$\overline{OE}$
$V_{CC}$	14	41	$V_{SS}$
$\overline{WE}$	15	40	DNU/ $V_{SS}$
DNU/ $V_{CC}$	16	39	$\overline{BLE}$
$A_{19}$	17	38	$A_{10}$
$A_{18}$	18	37	$A_{11}$
$A_{17}$	19	36	$A_{12}$
$A_{16}$	20	35	$A_{13}$
$A_{15}$	21	34	$A_{14}$
$I/O_0$	22	33	$I/O_7$
$V_{CC}$	23	32	$V_{SS}$
$I/O_1$	24	31	$I/O_6$
$I/O_2$	25	30	$I/O_5$
$V_{SS}$	26	29	$V_{CC}$
$I/O_3$	27	28	$I/O_4$

### Notes:

1. DNU/ $V_{CC}$  Pin (#16) has to be left floating or connected to  $V_{CC}$  and DNU/ $V_{SS}$  Pin (#40) has to be left floating or connected to  $V_{SS}$  to ensure proper application.
2. NC – No Connect Pins are not connected to the die

**Selection Guide**

		-10	-12	Unit
Maximum Access Time		10	12	ns
Maximum Operating Current	Commercial	275	260	mA
	Industrial	275	260	
Maximum CMOS Standby Current	Commercial/Industrial	50	50	mA

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[3]</sup> -0.5V to +4.6VDC  
Voltage Applied to Outputs in High-Z State<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[3]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW)..... 20 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics** Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		Unit
			Min.	Max.	Min.	Max.	
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -4.0 \text{ mA}$	2.4		2.4		V
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 8.0 \text{ mA}$		0.4		0.4	V
$V_{IH}$	Input HIGH Voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V
$V_{IL}$	Input LOW Voltage <sup>[3]</sup>		-0.3	0.8	-0.3	0.8	V
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	μA
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	μA
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}, f = f_{MAX} = 1/t_{RC}$	Commercial	275		260	mA
			Industrial	275		260	mA
$I_{SB1}$	Automatic CE Power-down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		70		70	mA
$I_{SB2}$	Automatic CE Power-down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$		50		50	mA

**Capacitance<sup>[4]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}, f = 1 \text{ MHz}, V_{CC} = 3.3V$	6	pF
$C_{OUT}$	I/O Capacitance		8	pF

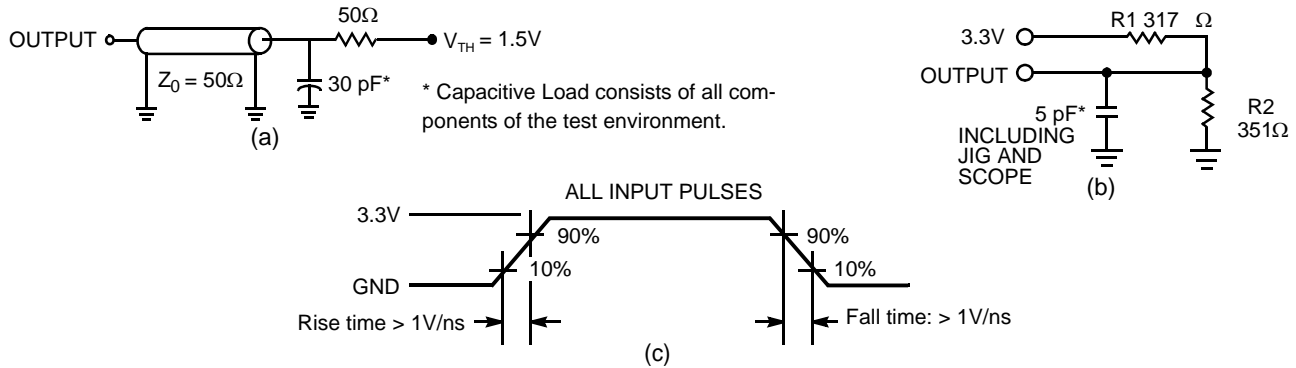
**Thermal Resistance<sup>[4]</sup>**

Parameter	Description	Test Conditions	54-pin TSOP-II	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	49.95	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		3.34	°C/W

**Notes:**

- $V_{IL}(\text{min.}) = -2.0V$  and  $V_{IH}(\text{max.}) = V_{CC} + 0.5V$  for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms<sup>[5]</sup>**



**AC Switching Characteristics Over the Operating Range<sup>[6]</sup>**

Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
<b>Read Cycle</b>						
$t_{power}$	$V_{CC}$ (typical) to the first access <sup>[7]</sup>	1		1		ms
$t_{RC}$	Read Cycle Time	10		12		ns
$t_{AA}$	Address to Data Valid		10		12	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		10		12	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		5		6	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low-Z	1		1		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High-Z <sup>[8]</sup>		5		6	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low-Z <sup>[8]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High-Z <sup>[8]</sup>		5		6	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up <sup>[9]</sup>	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down <sup>[9]</sup>		10		12	ns
$t_{DBE}$	Byte Enable to Data Valid		5		6	ns
$t_{LZBE}$	Byte Enable to Low-Z	1		1		ns
$t_{HZBE}$	Byte Disable to High-Z		5		6	ns

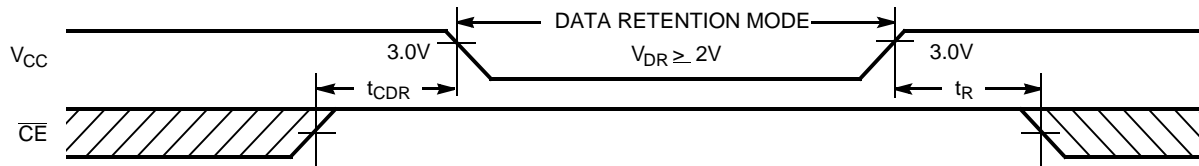
**Notes:**

- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and specified transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{power}$  time has to be provided initially before a Read/Write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZWE}$ ,  $t_{HZBE}$  and  $t_{LZOE}$ ,  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{LZBE}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Chip enables must be active and  $\overline{WE}$  and byte enables must be LOW to initiate a Write, and the transition of any of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**AC Switching Characteristics** Over the Operating Range<sup>[6]</sup> (continued)

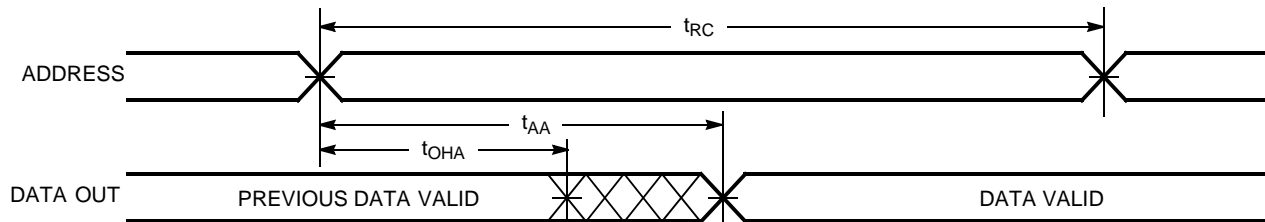
Parameter	Description	-10		-12		Unit
		Min.	Max.	Min.	Max.	
<b>Write Cycle<sup>[10, 11]</sup></b>						
$t_{WC}$	Write Cycle Time	10		12		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	7		8		ns
$t_{AW}$	Address Set-up to Write End	7		7		ns
$t_{SA}$	Address Set-up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	7		8		ns
$t_{SD}$	Data Set-up to Write End	5.5		6		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[8]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[8]</sup>		5		6	ns
$t_{BW}$	Byte Enable to End of Write	7		8		ns
$t_{HA}$	Address Hold from Write End	0		0		ns

**Data Retention Waveform**



**Switching Waveforms**

**Read Cycle No. 1<sup>[12, 13]</sup>**

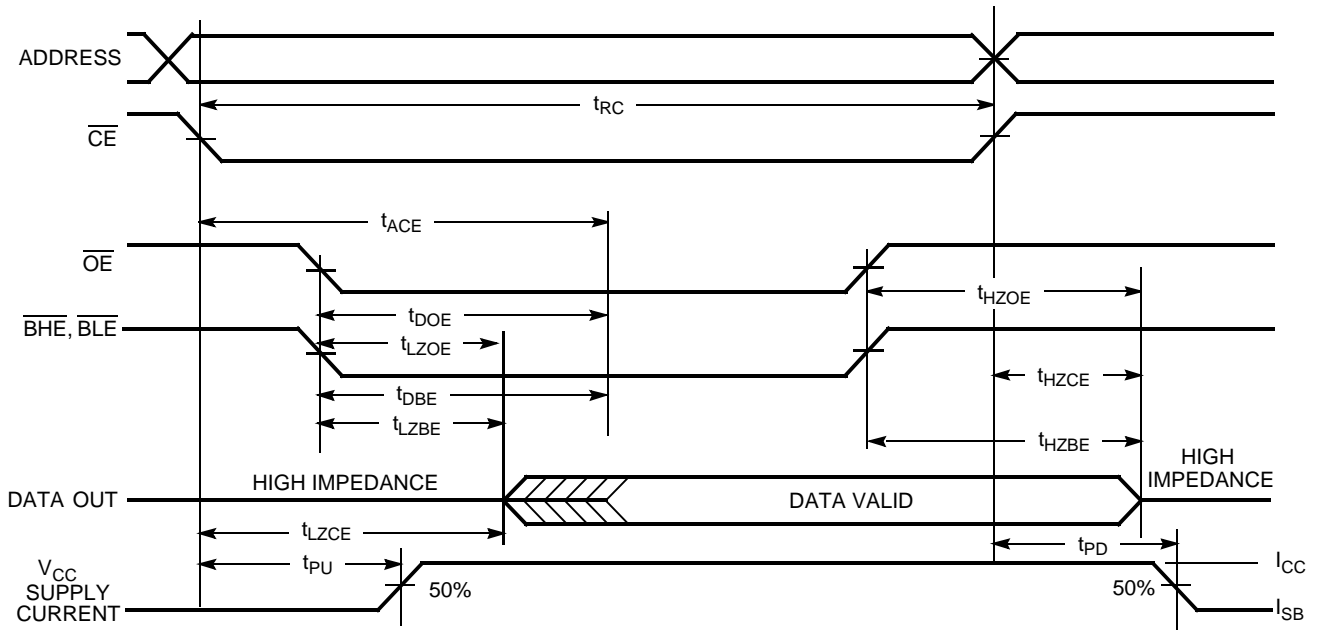


**Notes:**

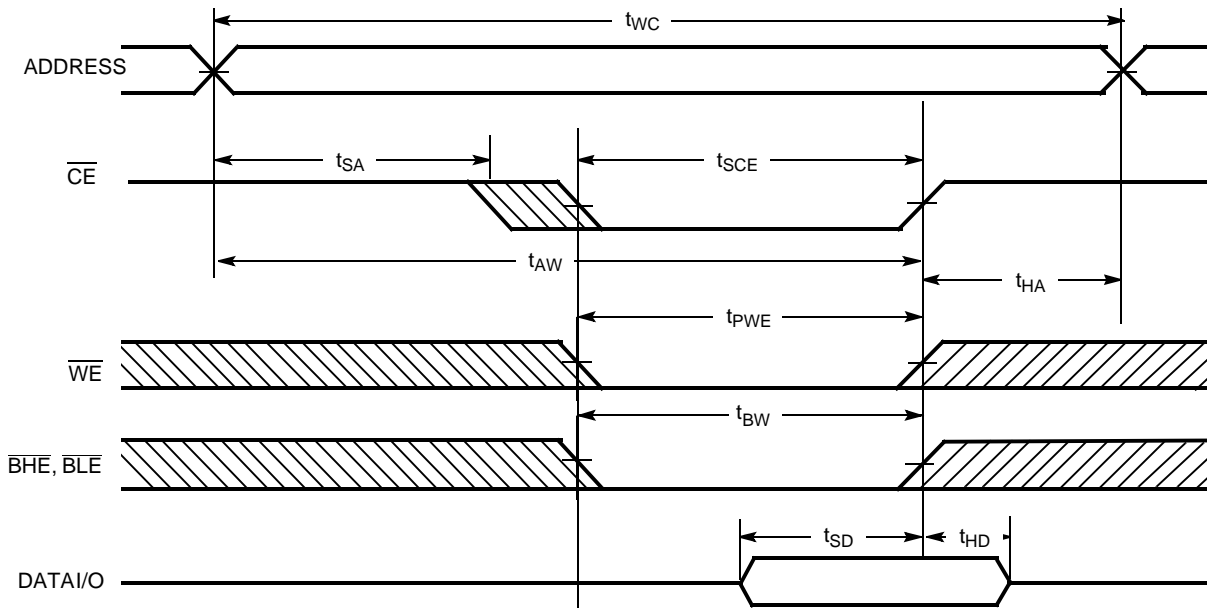
- 12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}$ ,  $\overline{BHE}$  and/or  $\overline{BHE} = V_{IL}$ .
- 13.  $\overline{WE}$  is HIGH for Read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>



Write Cycle No. 1 ( $\overline{CE}$  Controlled)<sup>[15, 16]</sup>

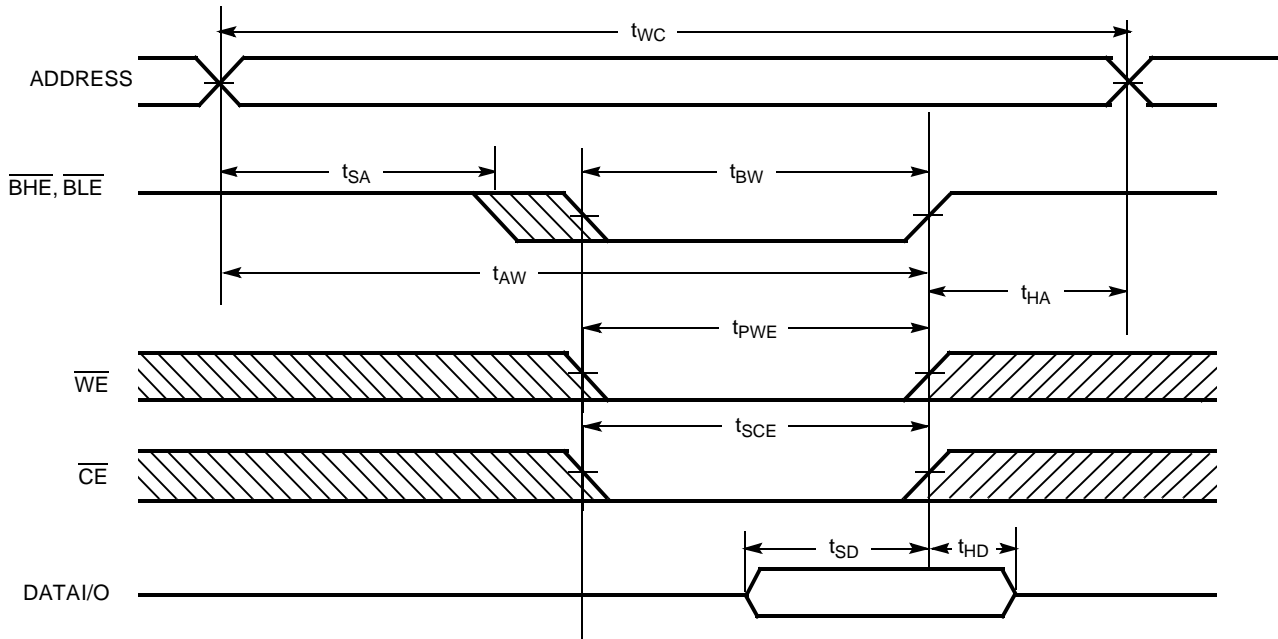


Notes:

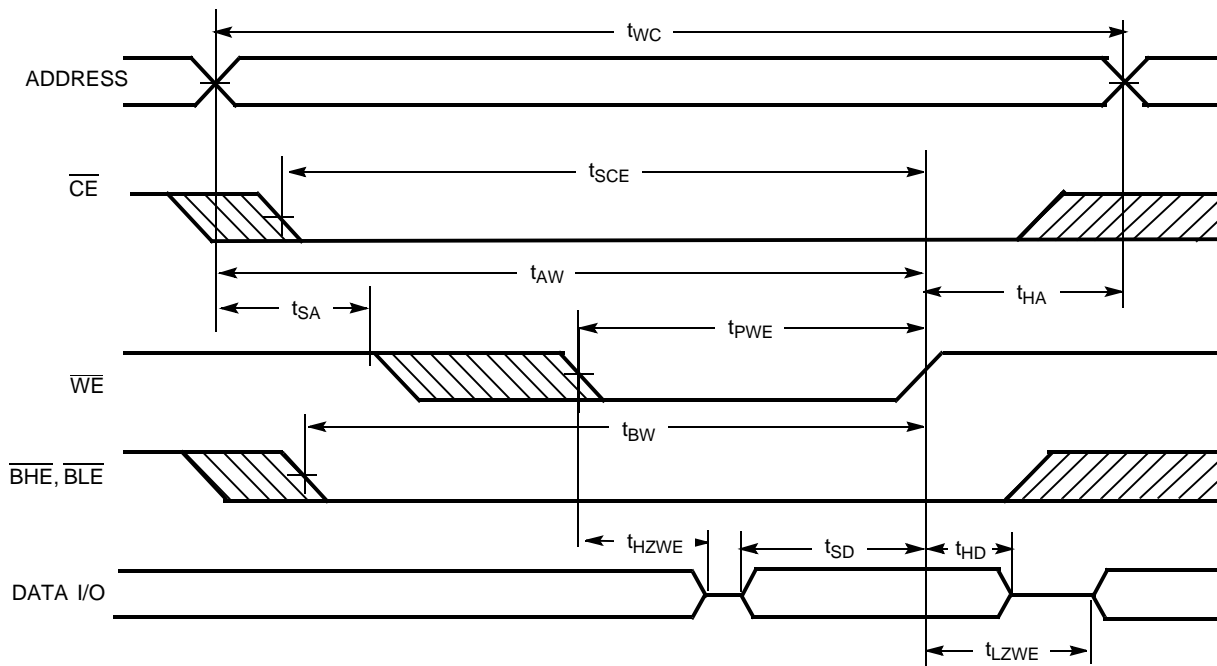
- 14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.
- 15. Data I/O is high-impedance if  $\overline{OE}$  or BHE and/or BLE =  $V_{IH}$ .
- 16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 2 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled)



Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[15, 16]</sup>



**Truth Table**

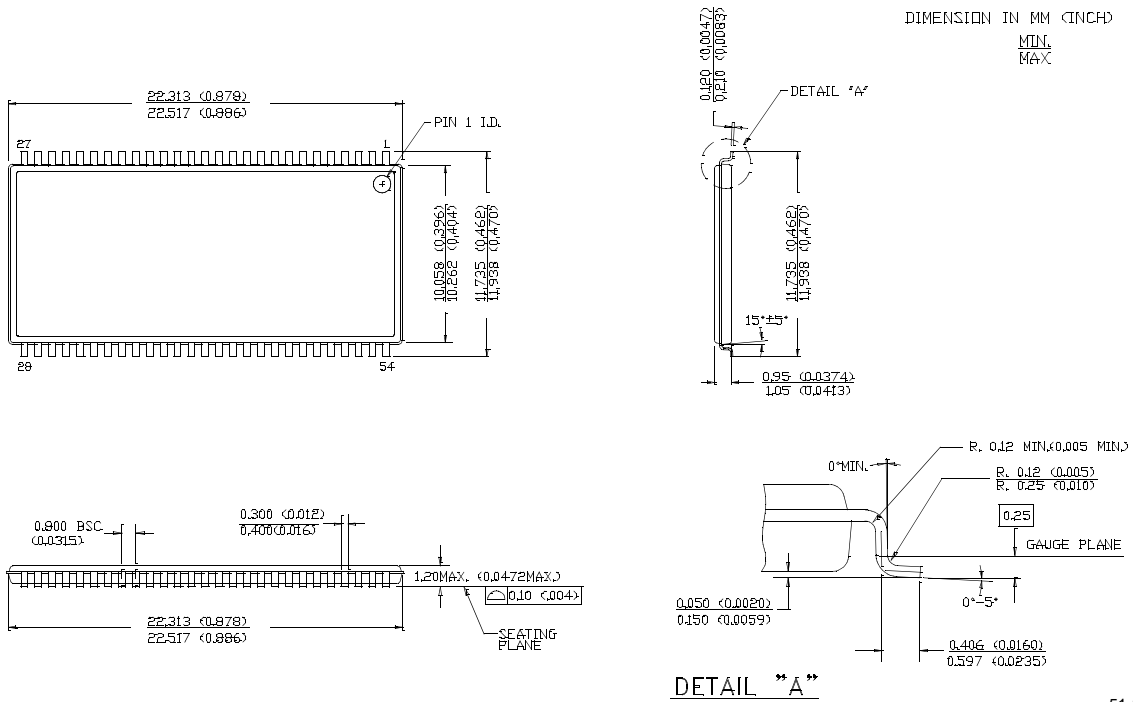
$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{BLE}}$	$\overline{\text{BHE}}$	I/O <sub>0</sub> -I/O <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I <sub>SB</sub> )
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I <sub>CC</sub> )
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I <sub>CC</sub> )
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I <sub>CC</sub> )
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I <sub>CC</sub> )
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I <sub>CC</sub> )
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I <sub>CC</sub> )
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1061BV33-10ZC	51-85160	54-pin TSOP II	Commercial
	CY7C1061BV33-10ZI			Industrial
	CY7C1061BV33-10ZXC		54-pin TSOP II (Pb-free)	Commercial
	CY7C1061BV33-10ZXI			Industrial
12	CY7C1061BV33-12ZC		54-pin TSOP II	Commercial
	CY7C1061BV33-12ZI			Industrial
	CY7C1061BV33-12ZXC		54-pin TSOP II (Pb-free)	Commercial
	CY7C1061BV33-12ZXI			Industrial

Package Diagram

54-pin TSOP II (51-85160)



51-85160-\*\*

All products and company names mentioned in this document may be the trademarks of their respective holders.



**Document History Page**

<b>Document Title: CY7C1061BV33 16-Mbit (1M x 16) Static RAM</b>				
<b>Document Number: 38-05693</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	283950	See ECN	RKF	New data sheet
*A	309453	See ECN	RKF	Final data sheet
*B	492137	See ECN	NXR	Removed 8 ns speed bin Changed the description of $I_{IX}$ from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Updated the Ordering Information Table