Integrated Circuit Systems, Inc.

ICS8701I
LOW SKEW ÷1, ÷2 CLOCK GENERATOR

GENERAL DESCRIPTION

The ICS8701I is a low skew, ÷1, ÷2 Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 20 to 40 by utilizing the ability of the outputs to drive two series terminated lines.

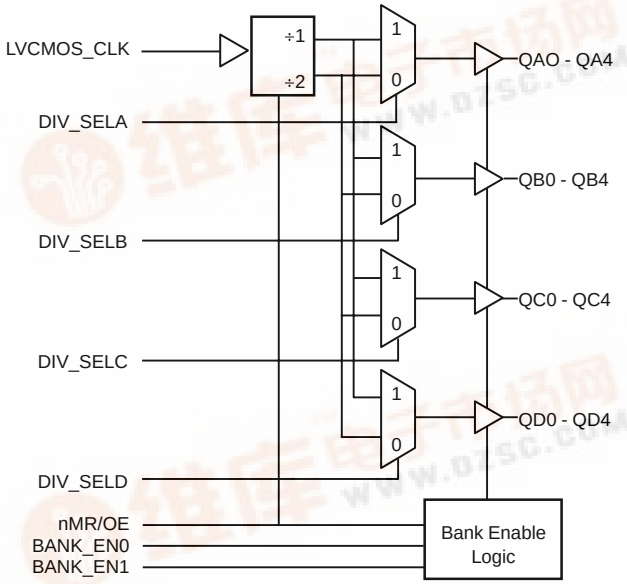
The divide select inputs, DIV_SELx, control the output frequency of each bank. The outputs can be utilized in the ÷1, ÷2 or a combination of ÷1 and ÷2 modes. The bank enable inputs, BANK_EN0:1, support enabling and disabling each bank of outputs individually. The master reset input, nMR/OE, resets the internal frequency dividers and also controls the active and high impedance states of all outputs.

The ICS8701I is characterized at 3.3V and mixed 3.3V input supply, and 2.5V output supply operating modes. Guaranteed bank, output and part-to-part skew characteristics make the ICS8701I ideal for those clock distribution applications demanding well defined performance and repeatability.

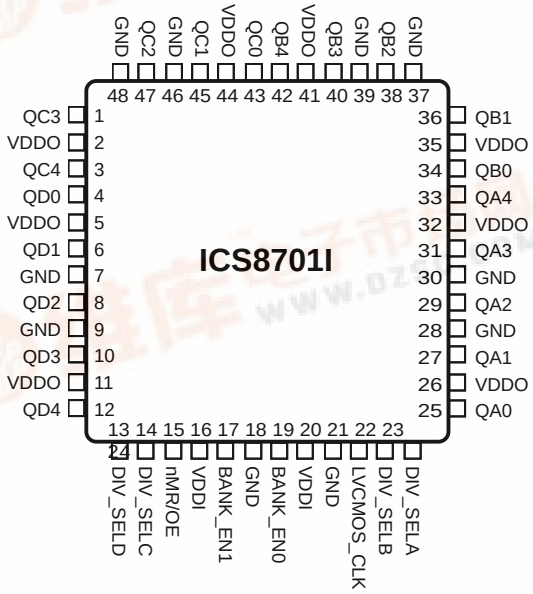
FEATURES

- 20 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 250MHz
- 200ps bank skew, 250ps output skew, 300ps multiple frequency skew, 600ps part-to-part skew
- LVCMOS / LVTTL clock input
- LVCMOS control inputs
- Bank enable logic allows unused banks to be disabled in reduced fanout applications
- 3.3V or mixed 3.3V input, 2.5V output operating supply modes
- 48 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- -40°C to 85°C ambient operating temperature
- Other divide values available on request

BLOCK DIAGRAM



PIN ASSIGNMENT



48-Pin LQFP
Y Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
2, 5, 11, 26, 32, 35, 41, 44	VDDO	Power		Output power supply. Connect to 3.3V or 2.5V.
7, 9, 18, 21, 28, 30, 37, 39, 46, 48	GND	Power		Ground. Connect to ground.
16, 20	VDDI	Power		Input power supply. Connect to 3.3V.
25, 27, 29, 31, 33	QA0, QA1, QA2, QA3, QA4	Output		Bank A outputs. LVCMOS interface levels. 7Ω typical output impedance.
34, 36, 38, 40, 42	QB0, QB1, QB2, QB3, QB4	Output		Bank B outputs. LVCMOS interface levels. 7Ω typical output impedance.
43, 45, 47, 1, 3	QC0, QC1, QC2, QC3, QC4	Output		Bank C outputs. LVCMOS interface levels. 7Ω typical output impedance.
4, 6, 8, 10, 12	QD0, QD1, QD2, QD3, QD4	Output		Bank D outputs. LVCMOS interface levels 7Ω typical output impedance.
22	LVCMOS_CLK	Input	Pulldown	Clock input. LVCMOS interface levels.
13	DIV_SELD	Input	Pullup	Controls frequency division for bank D outputs. LVCMOS interface levels.
14	DIV_SELC	Input	Pullup	Controls frequency division for bank C outputs. LVCMOS interface levels.
23	DIV_SELB	Input	Pullup	Controls frequency division for bank B outputs. LVCMOS interface levels.
24	DIV_SELA	Input	Pullup	Controls frequency division for bank A outputs. LVCMOS interface levels.
17, 19	BANK_EN1, BANK_EN0	Input	Pullup	Enables and disables outputs by banks. LVCMOS interface levels.
15	nMR/OE	Input	Pullup	Master reset and output enable. Enables and disables all outputs. LVCMOS interface levels.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	LVCMOS_CLK					pF
		DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, NMR/OE, BANK_EN1,					
RPULLUP	Input Pullup Resistor				51		KΩ
RPULLDOWN	Input Pulldown Resistor				51		KΩ
CPD	Power Dissipation Capacitance (per output)		VDDI, VDDO = 3.465V				pF
			VDDI = 3.465V, VDDO = 2.625V				pF
ROUT	Output Impedance				7		Ω

TABLE 3. FUNCTION TABLE

Inputs				Outputs				
nMR/OE	BANK_EN1	BANK_EN0	DIV_SELx	QA0 - QA4	QB0 - QB4	QC0 - QC4	QD0 - QD4	Qx frequency
0	X	X	X	Hi Z	Hi Z	Hi Z	Hi Z	zero
1	0	0	0	Active	Hi Z	Hi Z	Hi Z	fIN/2
1	1	0	0	Active	Active	Hi Z	Hi Z	fIN/2
1	0	1	0	Active	Active	Active	Hi Z	fIN/2
1	1	1	0	Active	Active	Active	Active	fIN/2
1	0	0	1	Active	Hi Z	Hi Z	Hi Z	fIN
1	1	0	1	Active	Active	Hi Z	Hi Z	fIN
1	0	1	1	Active	Active	Active	Hi Z	fIN
1	1	1	1	Active	Active	Active	Active	fIN

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDDI=VDDO=3.3V±5%, T_A=-40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDD	Quiescent Power Supply Current	VDDI = VIH = 3.465V VIL = 0V			100	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, VDDI=VDDO=3.3V±5%, T_A=-40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = 3.465V	2		3.8	V
		LVCMOS_CLK	VDDI = 3.465V	2		3.8	V
VIL	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = 3.465V	-0.3		0.8	V
		LVCMOS_CLK	VDDI = 3.465V	-0.3		1.3	V
IIH	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = VIN = 3.465V			5	µA
		LVCMOS_CLK	VDDI = VIN = 3.465V			150	µA
IIL	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = 3.465V, VIN = 0V	-150			µA
		LVCMOS_CLK	VDDI = 3.465V, VIN = 0V	-5			µA
VOH	Output High Voltage		VDDI = VDDO = 3.135V IOH = -36mA	2.6			V
VOL	Output Low Voltage		VDDI = VDDO = 3.135V IOL = 36mA			0.5	V

TABLE 5A. AC CHARACTERISTICS, VDDI=VDDO=3.3V±5%, T_A=-40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				250	MHz
tpLH	Propagation Delay, Low-to-High	0MHZ ≤ f ≤ 200MHz	2.2		3.6	ns
tpHL	Propagation Delay, High-to-Low	0MHZ ≤ f ≤ 200MHz	2.2		3.6	ns
tsk(b)	Bank Skew; NOTE 2	Measured on rising edge at VDDO/2			200	ps
tsk(o)	Output Skew; NOTE 3	Measured on rising edge at VDDO/2			250	ps
tsk(w)	Multiple Frequency Skew; NOTE 4	Measured on rising edge at VDDO/2			300	ps
tsk(pp)	Part to Part Skew; NOTE 5	Measured on rising edge at VDDO/2			600	ps
tR	Output Rise Time; NOTE 6	30% to 70%	200		900	ps
tF	Output Fall Time; NOTE 6	30% to 70%	200		900	ps
tPW	Output Pulse Width	0MHZ ≤ f ≤ 200MHz	tCYCLE/2 - 0.6	tCYCLE/2	tCYCLE/2 + 0.6	ns
		f = 200MHz	1.9	2.5	3.1	ns
tEN	Output Enable Time; NOTE 6	f = 10MHz			6	ns
tDIS	Output Disable Time; NOTE 6	f = 10MHz			6	ns

NOTE 1: All parameters measured at 200MHz unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, VDDI=3.3V±5%, VDDO=2.5V±5%, T_A=-40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
IDD	Quiescent Power Supply Current	VDDI = VIH = 3.465V VIL = 0V			100	mA

TABLE 4B. LVCMOS DC CHARACTERISTICS, VDDI=3.3V±5%, VDDO=2.5V±5%, T_A=-40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = 3.465V	2		3.8	V
		LVCMOS_CLK	VDDI = 3.465V	2		3.8	V
VIL	Input Low Voltage	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VDDI = 3.465V	-0.3		0.8	V
		LVCMOS_CLK	VDDI = 3.465V	-0.3		1.3	V
IIH	Input High Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VIN = 3.465V			5	µA
		LVCMOS_CLK	VIN = 3.465V			150	µA
IIL	Input Low Current	DIV_SELA, DIV_SELB, DIV_SELC, DIV_SELD, BANK_EN0, BANK_EN1, nMR/OE	VIN = 0V	-150			µA
		LVCMOS_CLK	VIN = 0V	-5			µA
VOH	Output High Voltage		VDDI = 3.135V, VDDO = 2.375V IOH = -27mA	1.8			V
VOL	Output Low Voltage		VDDI = 3.135V, VDDO = 2.375V IOH = 27mA			0.5	V

TABLE 5B. AC CHARACTERISTICS, VDDI=3.3V±5%, VDDO=2.5V±5%, T_A=-40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
fMAX	Maximum Input Frequency				250	MHz
tpLH	Propagation Delay, Low-to-High	0MHZ ≤ f ≤ 200MHz	2.4		3.7	ns
tpHL	Propagation Delay, High-to-Low	0MHZ ≤ f ≤ 200MHz	2.4		3.7	ns
tsk(b)	Bank Skew; NOTE 2	Measured on rising edge at VDDO/2			225	ps
tsk(o)	Output Skew; NOTE 3	Measured on rising edge at VDDO/2			250	ps
tsk(w)	Multiple Frequency Skew; NOTE 4	Measured on rising edge at VDDO/2			300	ps
tsk(pp)	Part to Part Skew; NOTE 5	Measured on rising edge at VDDO/2			650	ps
tR	Output Rise Time; NOTE 6	30% to 70%	200		900	ps
tF	Output Fall Time; NOTE 6	30% to 70%	200		900	ps
tPW	Output Pulse Width	0MHZ ≤ f ≤ 200MHz	tCYCLE/2 - 0.6	tCYCLE/2	tCYCLE/2 + 0.6	ns
		f = 200MHz	1.9	2.5	3.1	ns
tEN	Output Enable Time; NOTE 6	f = 10MHz			6	ns
tDIS	Output Disable Time; NOTE 6	f = 10MHz			6	ns

NOTE 1: All parameters measured at 200MHz unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.
NOTE 2: Defined as skew within a bank of outputs at the same supply voltages and with equal load conditions.
NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.
NOTE 4: Defined as skew across banks of outputs operating at different frequency with the same supply voltages and equal load conditions.
NOTE 5: Defined as the skew at different outputs on different devices operating at the same supply voltages and with equal load conditions.
NOTE 6: These parameters are guaranteed by characterization. Not tested in production.

FIGURE 1A, 1B - TIMING DIAGRAMS

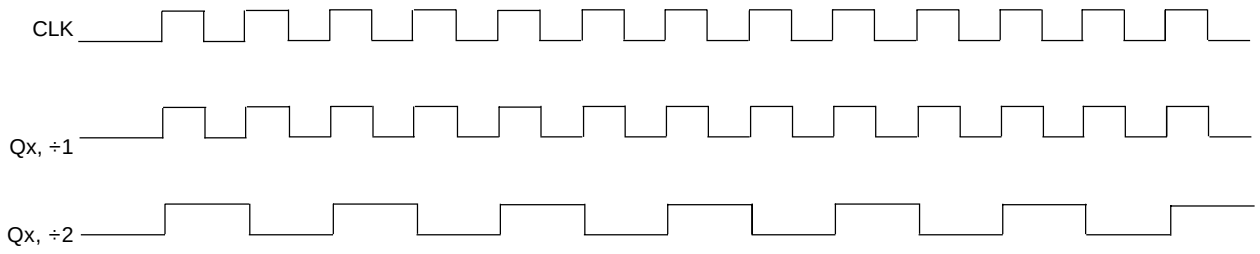


FIGURE 1A - ACTIVE, ÷1, ÷2

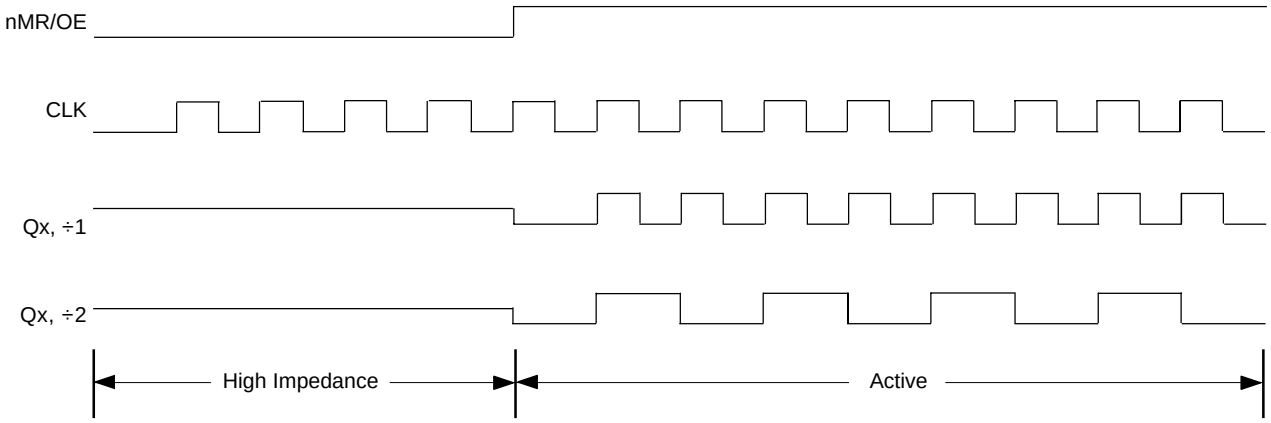


FIGURE 1B - RESET TO ACTIVE, ÷1, ÷2

FIGURE 2A, 2B - TIMING WAVEFORMS

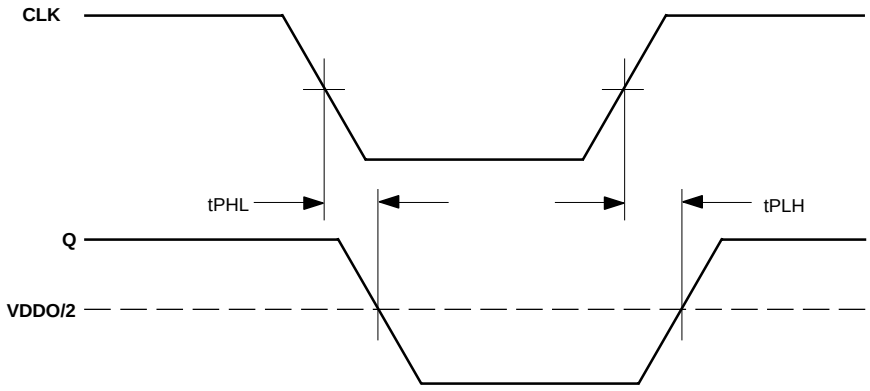


FIGURE 2A - PROPAGATION DELAYS

fin = 200MHz, Vamp = 3.3V, tr = tf = 600ps

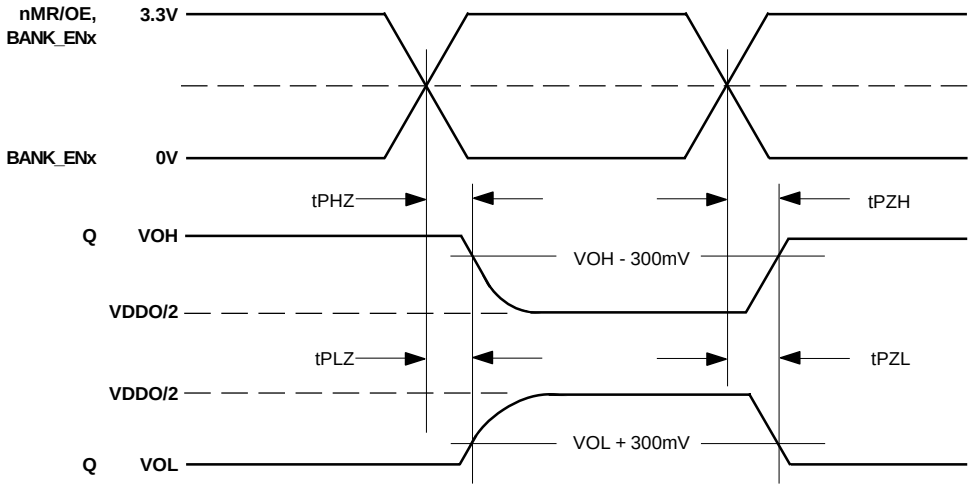


FIGURE 2B - DISABLE AND ENABLE TIMES

fin = 10MHz, Vamp = 3.3V, tr = tf = 600ps

FIGURE 3A, 3B - SKEW DEFINITIONS & WAVEFORMS

Bank Skew - Skew between outputs within a bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

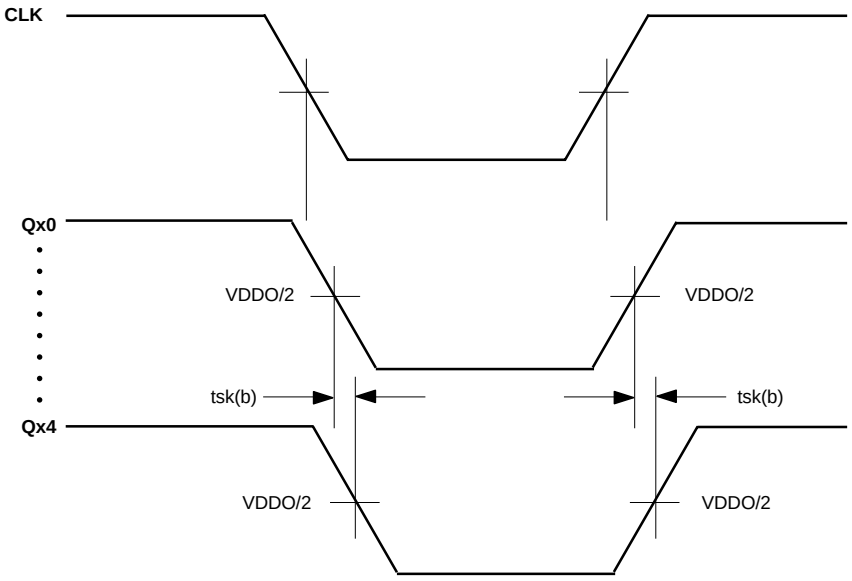


FIGURE 3A - BANK SKEW

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

Output Skew - Skew between outputs of any bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

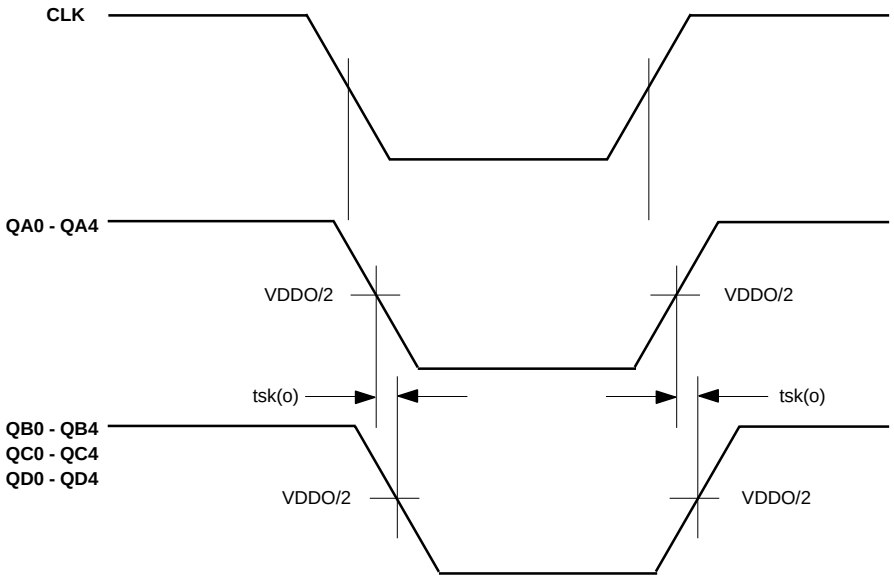


FIGURE 3B - OUTPUT SKEW

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

FIGURE 3C, 3D - SKEW DEFINITIONS & WAVEFORMS

Multiple Frequency Skew - Skew between banks of outputs operating at different frequencies. Outputs operating at the same temperature, supply voltages and with equal load conditions.

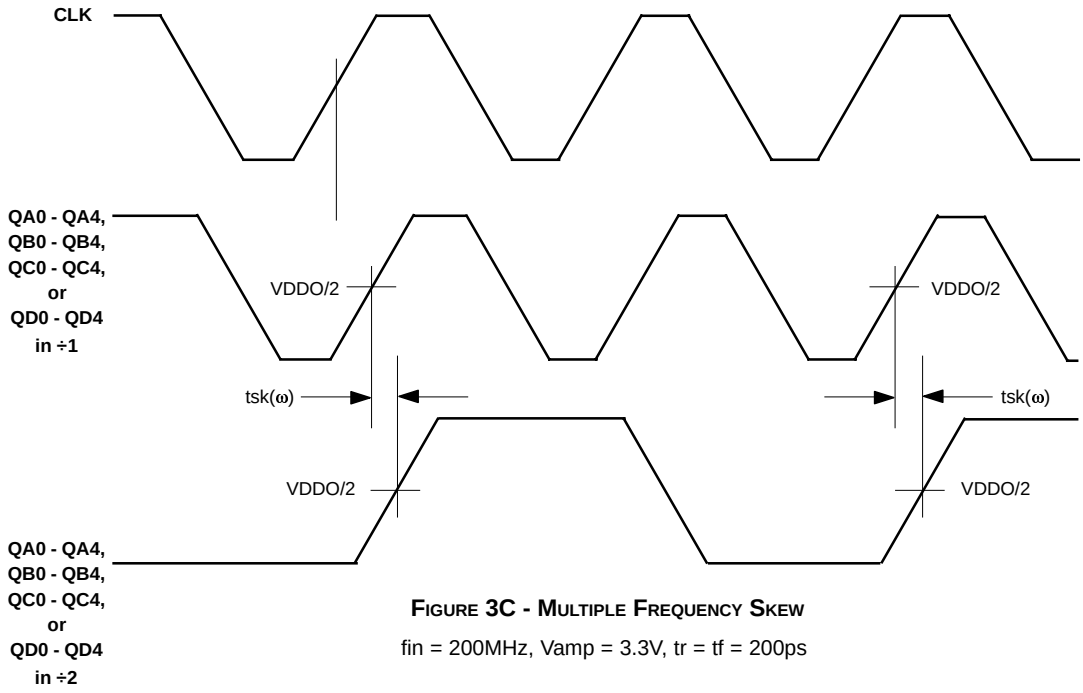


FIGURE 3C - MULTIPLE FREQUENCY SKEW

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

Part to Part Skew - Skew between outputs of any bank on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

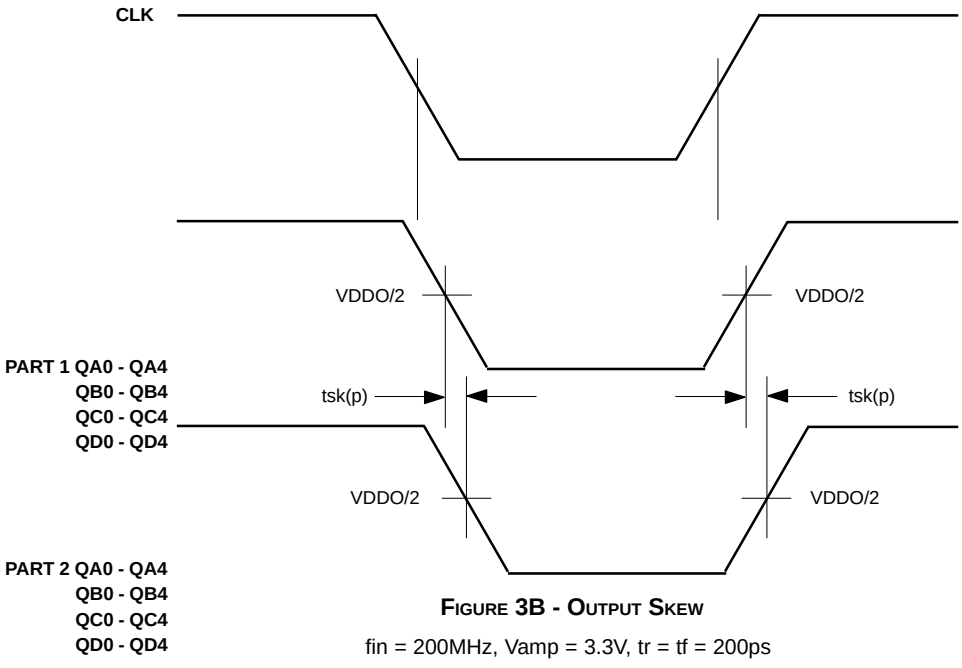


FIGURE 3B - OUTPUT SKEW

fin = 200MHz, Vamp = 3.3V, tr = tf = 200ps

PACKAGE OUTLINE - Y SUFFIX

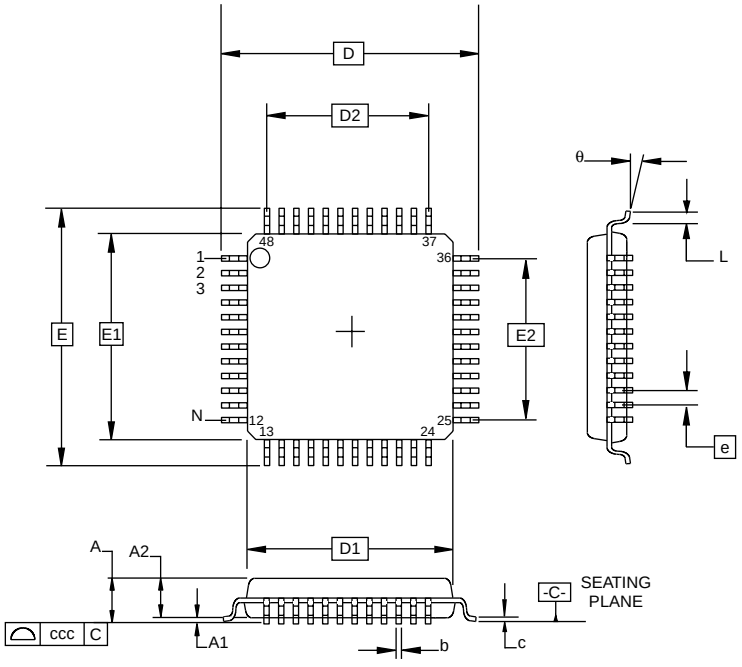


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BCC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		48	
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50	
e		0.5 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8701CYI	ICS8701CYI	48 Lead LQFP	250 per tray	-40°C to 85°C
ICS8701CYIT	ICS8701CYI	48 Lead LQFP on Tape and Reel	2000	-40°C to 85°C