



CYPRESS

CYM9260
CYM9261B
CYM9262A
CYM9263

64K x 72 SRAM Module
128K x 72 SRAM Module
256K x 72 SRAM Module
512K x 72 SRAM Module

Features

- Operates at 66 MHz
- Uses 64K x 18, 128K x 18, or 256K x 18 high performance synchronous SRAMs
- 168-position Angled DIMM from Amp p/n 179508-2
- 3.3V inputs/data outputs

Functional Description

The CYM9260, CYM9261, CYM9262, and the CYM9263 are high-performance synchronous memory modules organized as 64K(9260), 128K(9261), 256K(9262), or 512K(9263) by 72 bits. These modules are constructed from either 128K x 18(9260,9261B,9262A) or 256K x 18 (9263) SRAMs in plastic

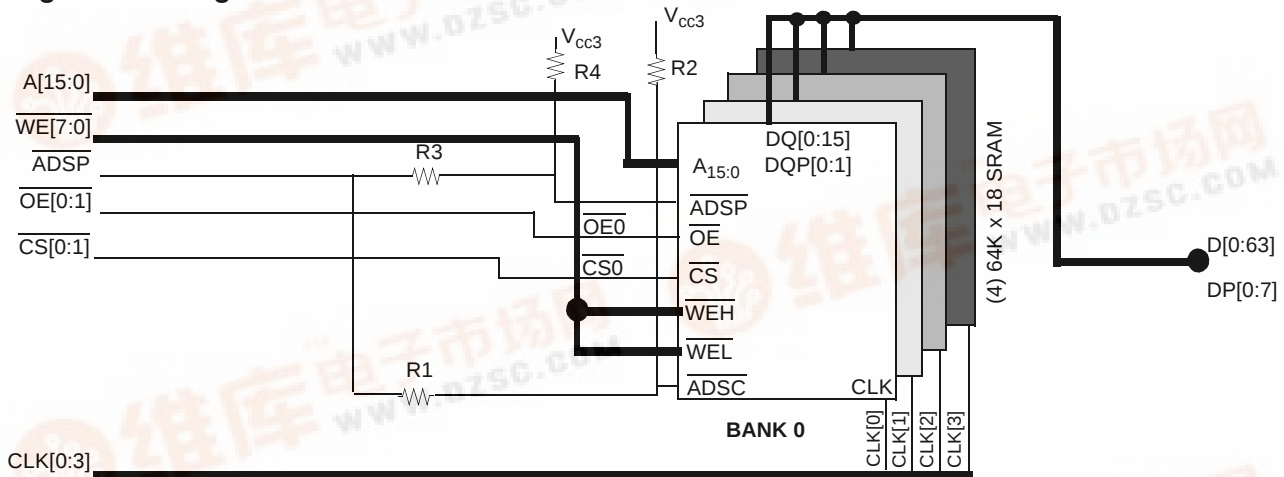
surface mount packages on an epoxy laminate board with pins. The modules are designed to be incorporated into large memory arrays.

The module is configured as either one or two banks, where each bank has separate chip select and output enable controls. Separate clocks are provided for every pair of SRAMs's.

Multiple ground pins and on-board decoupling capacitors ensure high performance with maximum noise immunity.

All components on the cache modules are surface mounted on a multi-layer epoxy laminate (FR-4) substrate. The contact pins are plated with 150 micro-inches of nickel covered by 30 micro-inches of gold flash.

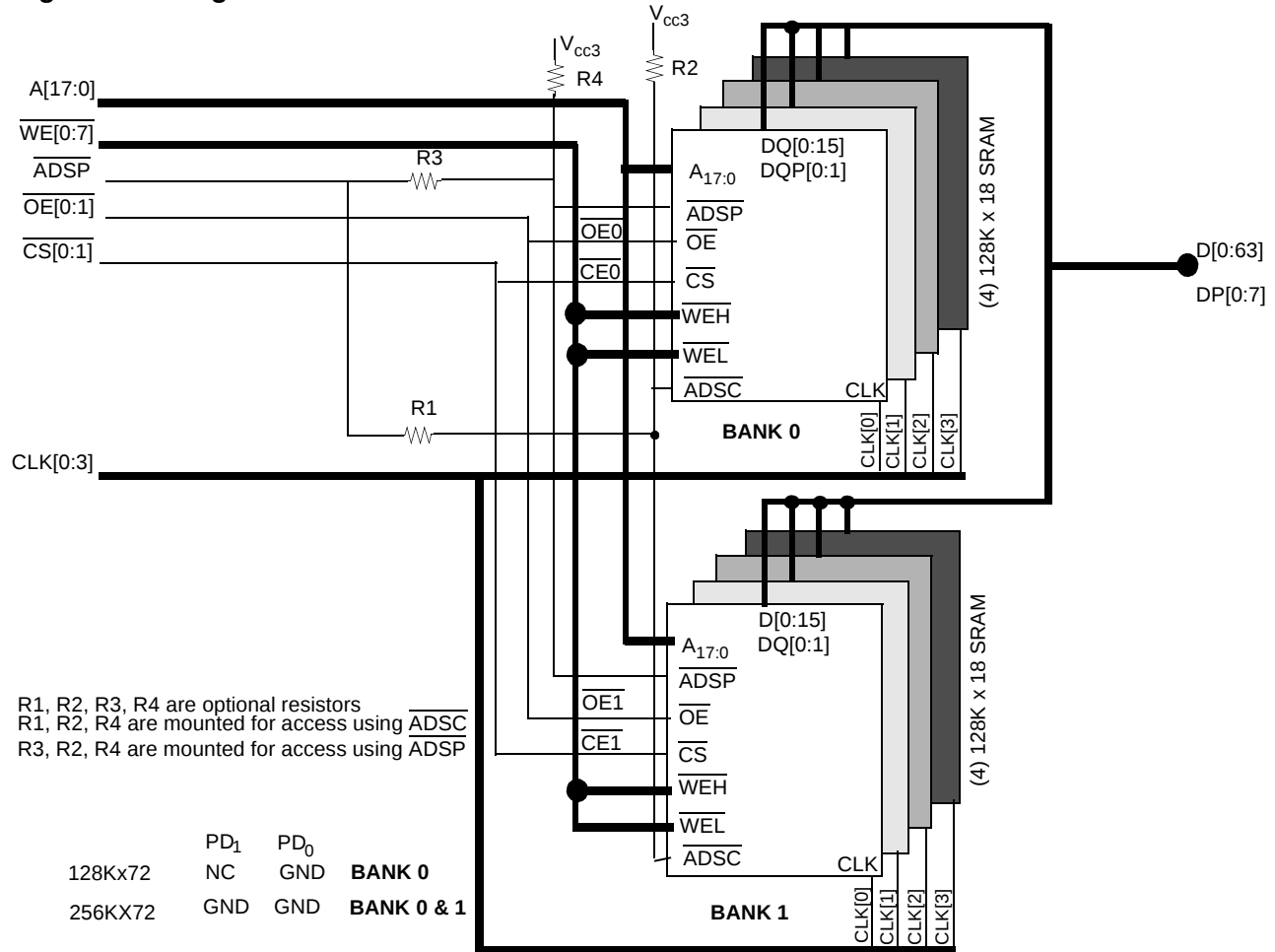
Logic Block Diagram - CYM9260



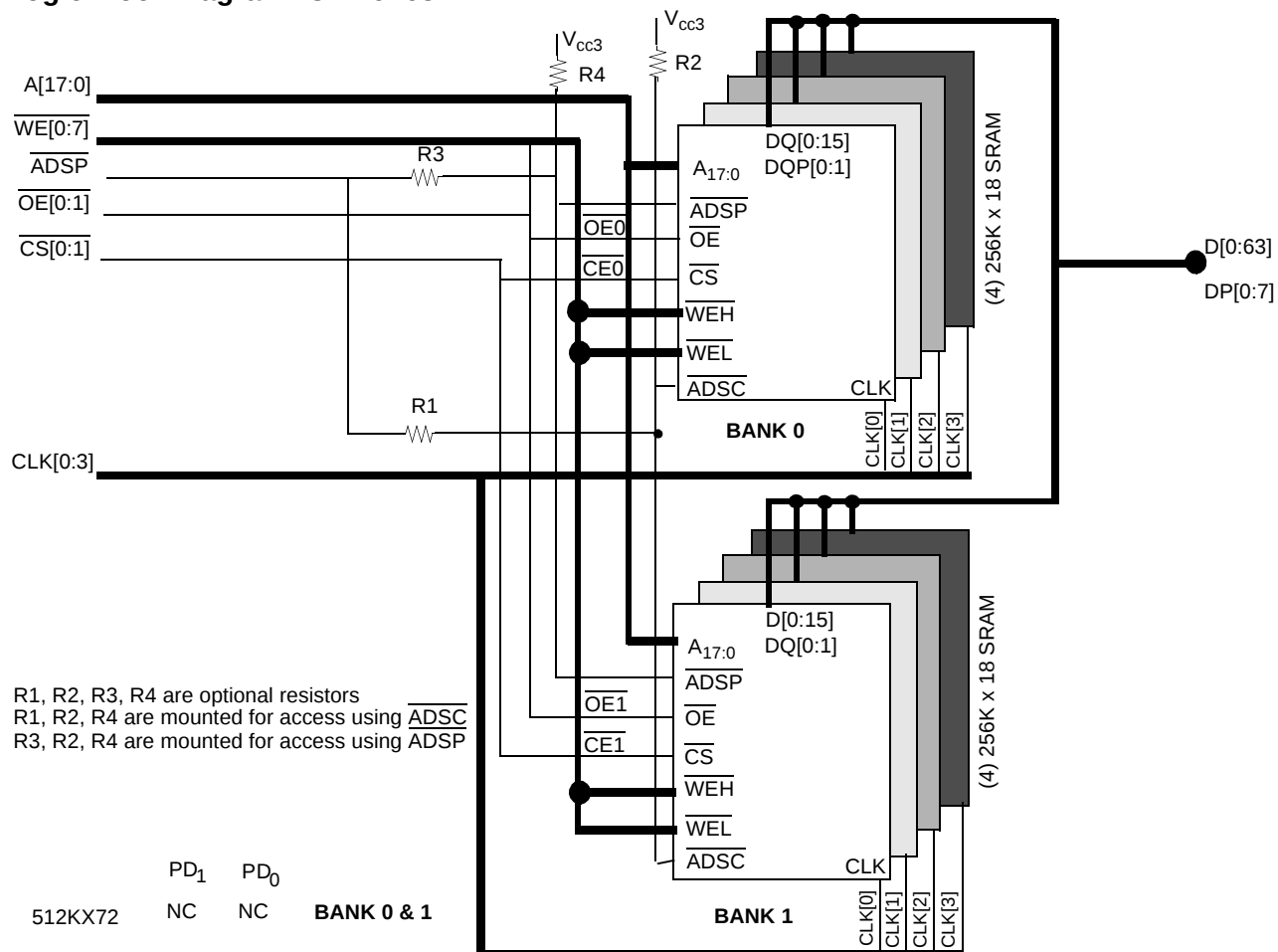
R1, R2, R3, R4 are optional resistors
R1, R2, R4 are mounted for access using ADSC
R3, R2, R4 are mounted for access using ADSP

PD₁ PD₀
64Kx72 GND NC **BANK 0**

Logic Block Diagram - CYM9261B/CYM9262A



Logic Block Diagram - CYM9263



Selection Guide

Part Number	Synchronous Cache Module			
	CYM9260-66	CYM9261B-66	CYM9262A-66	CYM9263-66
Cache Size	64 K x 72	128 K x 72	256 K x 72	512 K x 72
SRAMs Used	4 of 64K x 18	4 of 128K x 18	8 of 128K x 18	8 of 256K x 18
System Clock (MHz)	66	66	66	66
Data t _{CDV}	10.3 ns	10.3 ns	10.3 ns	10.3 ns



Pin Configuration

Dual Read-Out SIMM (DIMM)
Top View

GND	1	85	GND
D ₆₃	2	86	DP ₇
D ₆₂	3	87	D ₆₁
V _{CC3}	4	88	GND
D ₆₀	5	89	D ₅₉
D ₅₈	6	90	D ₅₇
GND	7	91	GND
D ₅₆	8	92	DP ₆
D ₅₅	9	93	D ₅₄
GND	10	94	V _{CC3}
D ₅₃	11	95	D ₅₂
D ₅₁	12	96	D ₅₀
GND	13	97	GND
D ₄₉	14	98	D ₄₈
DP ₅	15	99	D ₄₇
V _{CC3}	16	100	GND
D ₄₆	17	101	D ₄₅
D ₄₄	18	102	D ₄₃
GND	19	103	GND
D ₄₂	20	104	D ₄₁
D ₄₀	21	105	DP ₄
GND	22	106	V _{CC3}
D ₃₉	23	107	D ₃₈
D ₃₇	24	108	D ₃₆
GND	25	109	GND
D ₃₅	26	110	D ₃₄
D ₃₃	27	111	D ₃₂
GND	28	112	GND
CLK ₃	29	113	CLK ₂
GND	30	114	GND
DP ₃	31	115	D ₃₁
D ₃₀	32	116	D ₂₉
V _{CC3}	33	117	GND
D ₂₈	34	118	D ₂₇
D ₂₆	35	119	D ₂₅
GND	36	120	GND
D ₂₄	37	121	DP ₂
D ₂₃	38	122	D ₂₂
GND	39	123	V _{CC3}
D ₂₁	40	124	D ₂₀
D ₁₉	41	125	D ₁₈
GND	42	126	GND
D ₁₇	43	127	D ₁₆
DP ₁	44	128	D ₁₅
V _{CC3}	45	129	GND
D ₁₄	46	130	D ₁₃
D ₁₂	47	131	D ₁₁
GND	48	132	GND
D ₁₀	49	133	D ₉
D ₈	50	134	DP ₀
GND	51	135	V _{CC3}
D ₇	52	136	D ₆
D ₅	53	137	D ₄
GND	54	138	GND
D ₃	55	139	D ₂
D ₁	56	140	D ₀
V _{CC3}	57	141	GND
PD ₀	58	142	PD ₁
NC	59	143	A ₁₇
GND	60	144	GND
A ₁₆	61	145	A ₁₅
A ₁₄	62	146	A ₁₃
GND	63	147	V _{CC3}
A ₁₂	64	148	A ₁₁
A ₁₀	65	149	A ₉
GND	66	150	GND
A ₈	67	151	A ₇
A ₆	68	152	A ₅
V _{CC3}	69	153	GND
A ₄	70	154	A ₃
A ₂	71	155	A ₁
A ₀	72	156	ADSP
GND	73	157	GND
CLK ₁	74	158	CLK ₀
GND	75	159	GND
WE ₇	76	160	WE ₆
WE ₅	77	161	WE ₄
GND	78	162	GND
WE ₃	79	163	WE ₂
WE ₁	80	164	WE ₀
GND	81	165	V _{CC3}
OE ₁	82	166	OE ₀
CS ₁	83	167	CS ₀
GND	84	168	GND



Pin Definitions

Signal	Description
V _{CC3}	3V Supply
GND	Ground
A[17:0]	Addresses From Processor
OE[1:0]	Output Enables For The Two Banks
WE[7:0]	Byte Write Enables
CS[1:0]	Chip Select For The Two Banks
PD ₀ –PD ₁	Presence Detect Output Pins
D[63:0]	Data Lines From Processor
DP[7:0]	Data Parity Lines From Processor
CLK[0:3]	Clock Lines To The Module
ADSP	Address Strobe From The Processor
NC	Signal Not Connected On Module
RSVD	Reserved

Presence Detect Pins

	PD ₁	PD ₀
CYM9260 - 64K x 72	GND	NC
CYM9261 - 128K x 72	NC	GND
CYM9262 - 256K x 72	GND	GND
CYM9263 - 512K x 72	NC	NC



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -55°C to $+125^{\circ}\text{C}$

Ambient Temperature
with Power Applied -0°C to $+70^{\circ}\text{C}$

3.3V Supply Voltage to Ground Potential -0.5V to $+4.5\text{V}$

DC Voltage Applied to Outputs
in High Z State -0.5V to $+4.6\text{V}$

DC Input Voltage -0.5V to $+4.6\text{V}$

Output Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to $+70^{\circ}\text{C}$	$3.3\text{V} \pm 5\%$

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Condition	Min.	Max.	Unit
V _{IH}	Input HIGH Voltage		2.2	V _{CC} + 0.3	V
V _{IL}	Input LOW Voltage		-0.3	0.8	V
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8 mA		0.4	V
I _{CC} (9260)	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		1000	mA
I _{CC} (9261)	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		1000	mA
I _{CC} (9262)	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		1200	mA
I _{CC} (9263)	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}		2400	mA

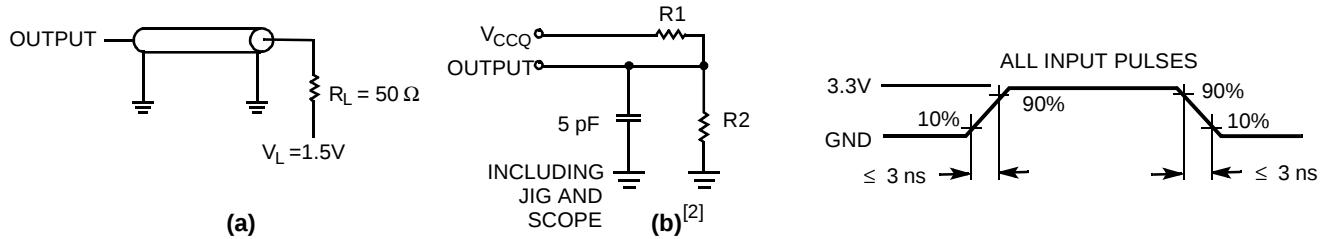
Capacitance^[1]

Parameter	Description	Test Conditions		Max.	Unit
C _A	Address Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9260	24	pF
			9261	14	pF
			9262	20	pF
			9263	40	pF
C _I	Control Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9260	24	pF
			9261	16	pF
			9262	20	pF
			9263	40	pF
C _O	Input/Output Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9260	9	pF
			9261	5	pF
			9262	8	pF
			9263	16	pF
C _{CLK}	Clock Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	9260	6	pF
			9261	3	pF
			9262	5	pF
			9262	10	pF

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[3]



Switching Characteristics Over the Operating Range

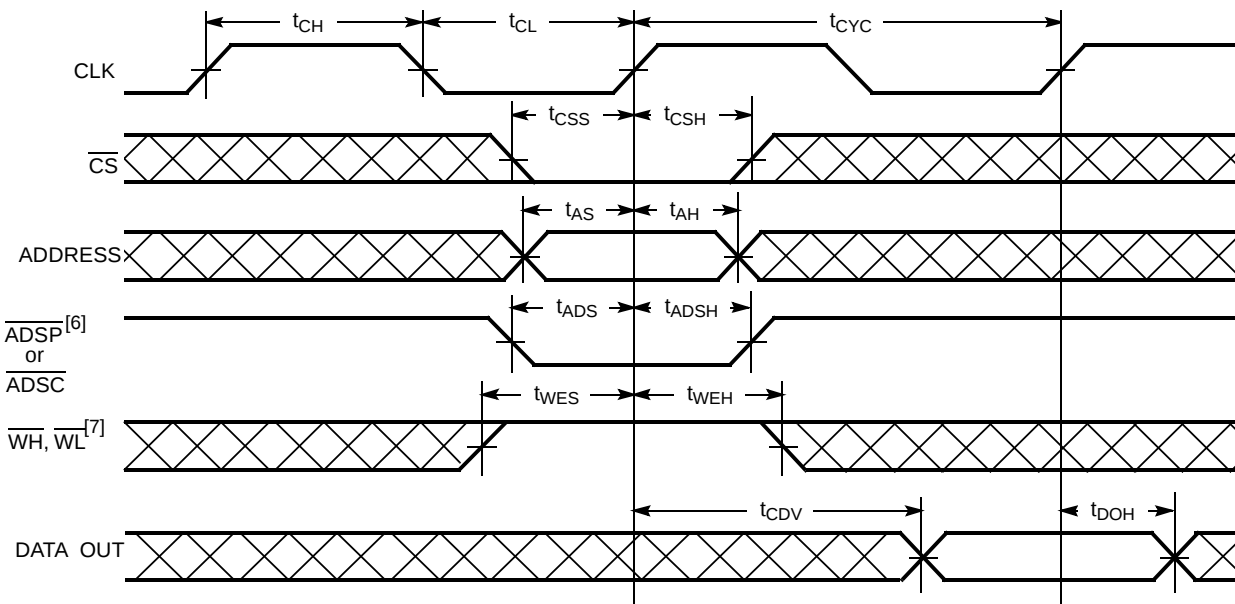
Parameter	Description	CYM9260/61/62/63				Unit
		66 MHz		50 MHz		
		Min.	Max.	Min.	Max.	
t _{CYC}	Clock Cycle Time	15		20		ns
t _{CH}	Clock HIGH	6		8		ns
t _{CL}	Clock LOW	6		8		ns
t _{AS}	Address Set-Up Before CLK Rise	3.1		3.1		ns
t _{AH}	Address Hold After CLK Rise	0.5		0.5		ns
t _{CDV}	Data Output Valid After CLK Rise		10.3		14	ns
t _{DOH}	Data Output Hold After CLK Rise	3		3		ns
t _{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	3.1		3.1		ns
t _{ADSH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		ns
t _{WES}	$\overline{WH}$, $\overline{WL}$ Set-Up Before CLK Rise	3.1		3.1		ns
t _{WEH}	$\overline{WH}$, $\overline{WL}$ Hold After CLK Rise	0.5		0.5		ns
t _{DS}	Data Input Set-Up Before CLK Rise	3.3		3.3		ns
t _{DH}	Data Input Hold After CLK Rise	0.5		0.5		ns
t _{CSS}	Chip Select Set-Up	3.1		3.1		ns
t _{CSH}	Chip Select Hold After CLK Rise	0.5		0.5		ns
t _{EOZ}	$\overline{OE}$ HIGH to Output High Z ^[4]		7		7	ns
t _{EOV}	$\overline{OE}$ LOW to Output Valid	7		7		ns

Notes:

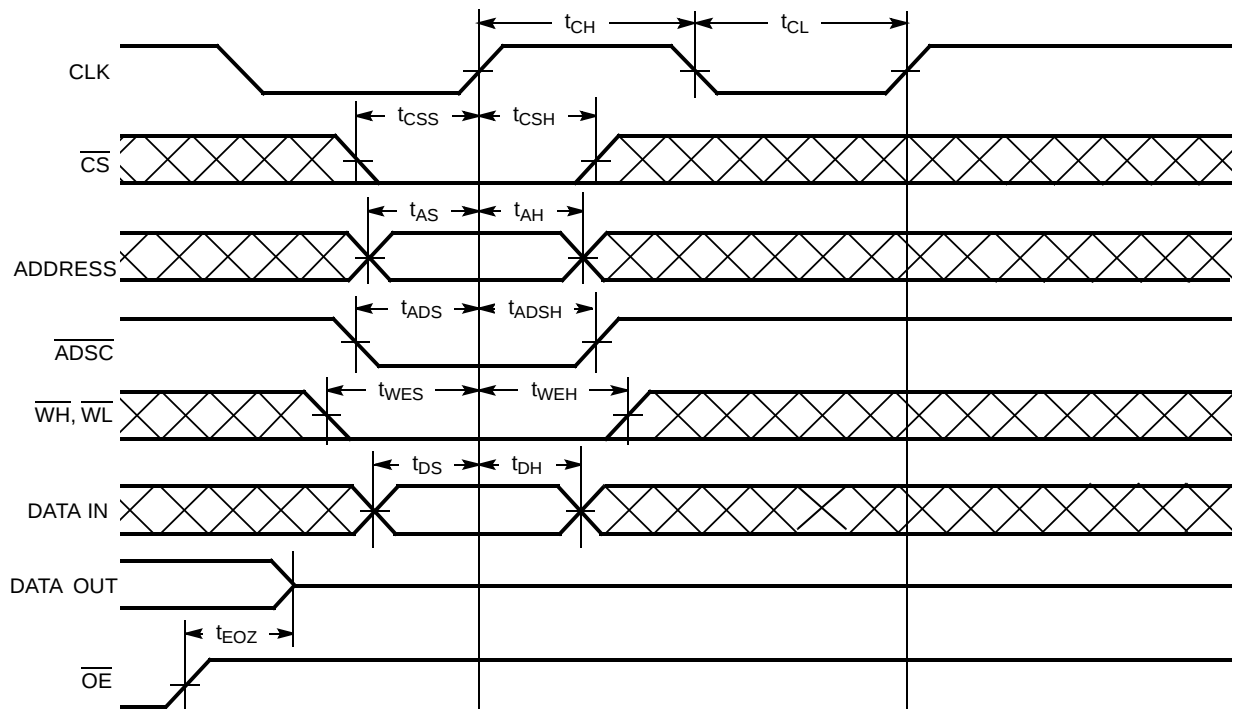
- Resistor values for $V_{CCQ} = 3.3\text{V}$ are $R_1 = 317\ \Omega$ and $R_2 = 351\ \Omega$.
- Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC Test Loads. All measurements are made at room temperature.
- t_{EOZ} is specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured $\pm 500\text{ mV}$ from steady-state voltage.

Switching Waveforms

Single Read^[5]



Single Write Timing (Using ADSC)

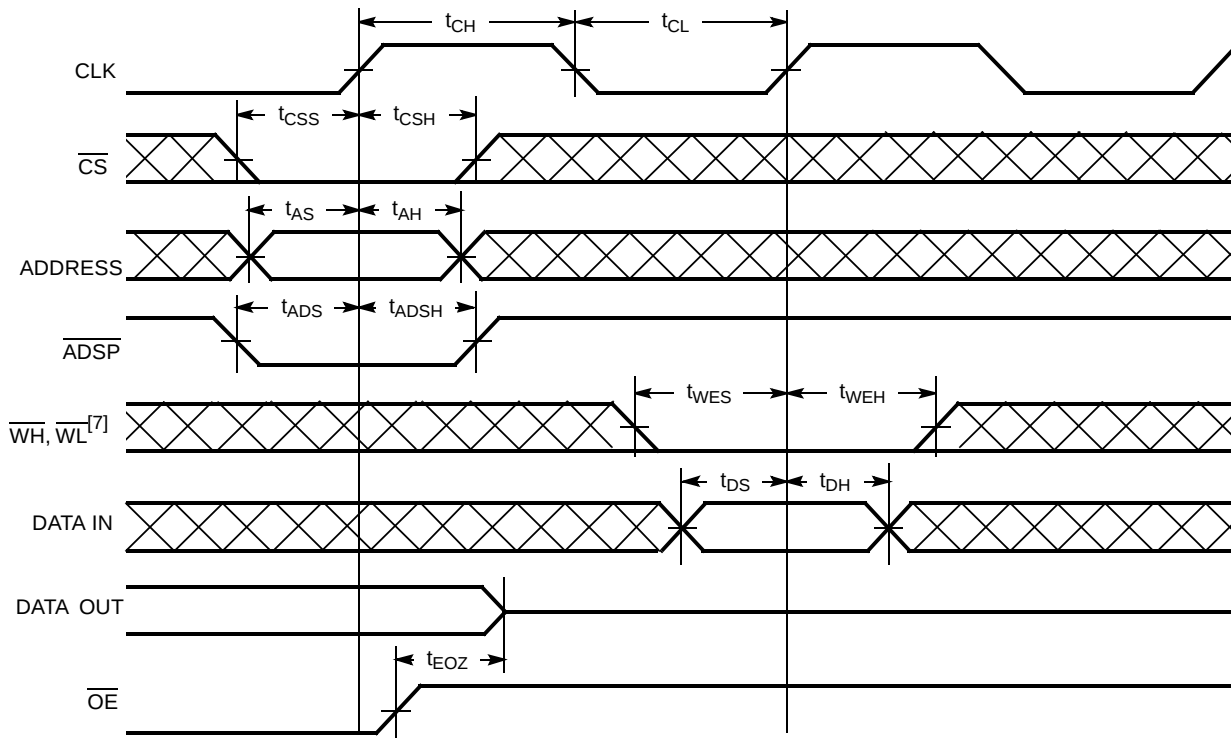


Notes:

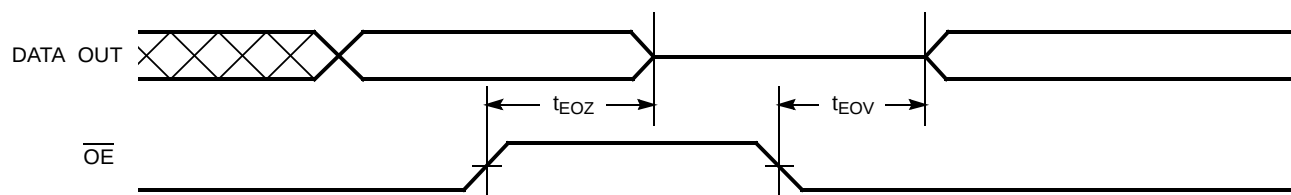
5. $\overline{OE}$ is LOW throughout this operation.
6. If $\overline{ADSP}$ is asserted while $\overline{CS}$ is HIGH, $\overline{ADSP}$ will be ignored.
7. $\overline{ADSP}$ has no effect on $\overline{ADV}$, $\overline{WL}$, and $\overline{WH}$ if $\overline{CS}$ is HIGH.

Switching Waveforms (continued)

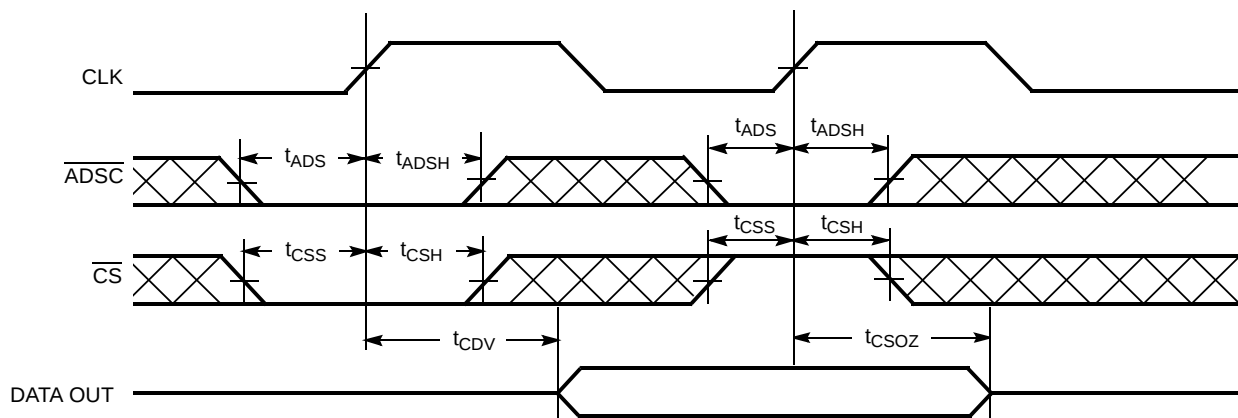
Single Write Cycle Using ADSP



Output (Controlled by OE)

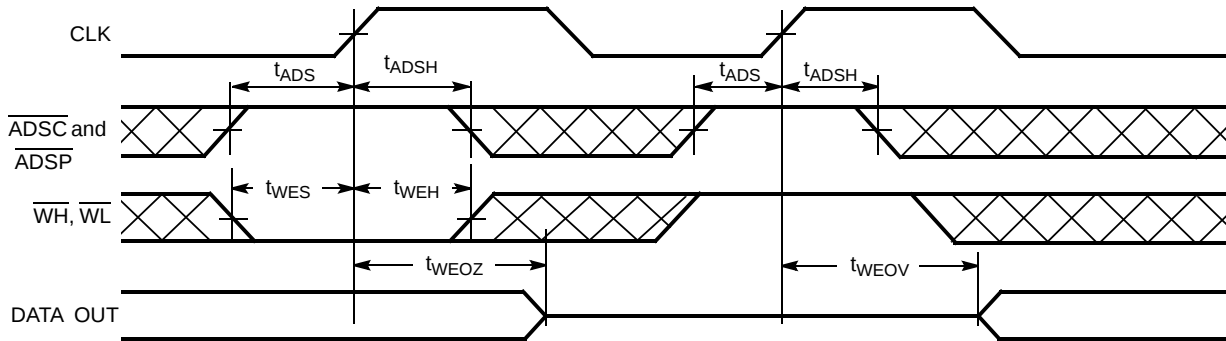


Output Timing (Controlled by CS)



Switching Waveforms (continued)

Output Timing (Controlled by $\overline{WH}$ / $\overline{WL}$)

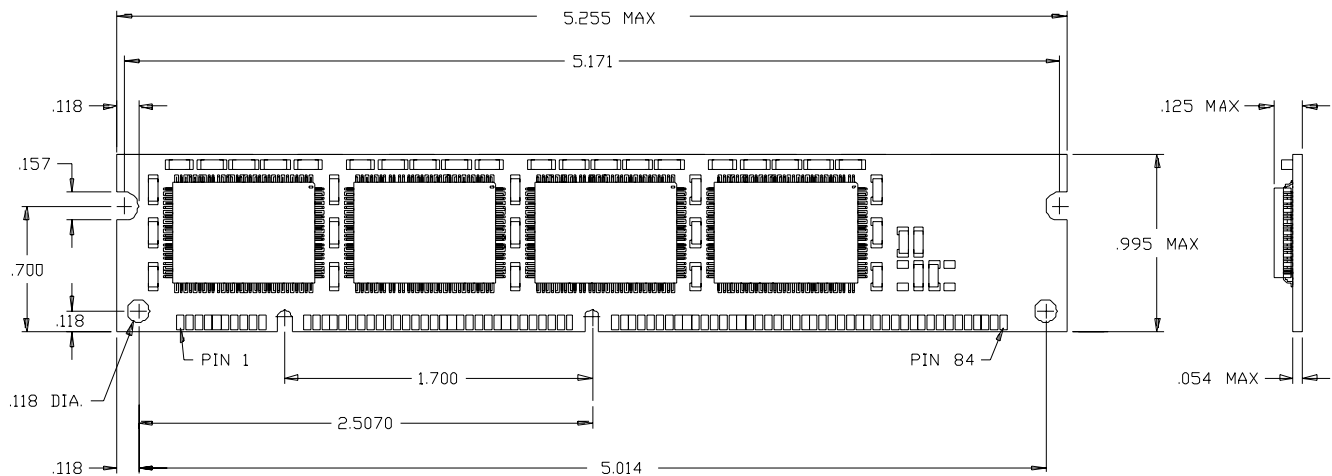


Ordering Information

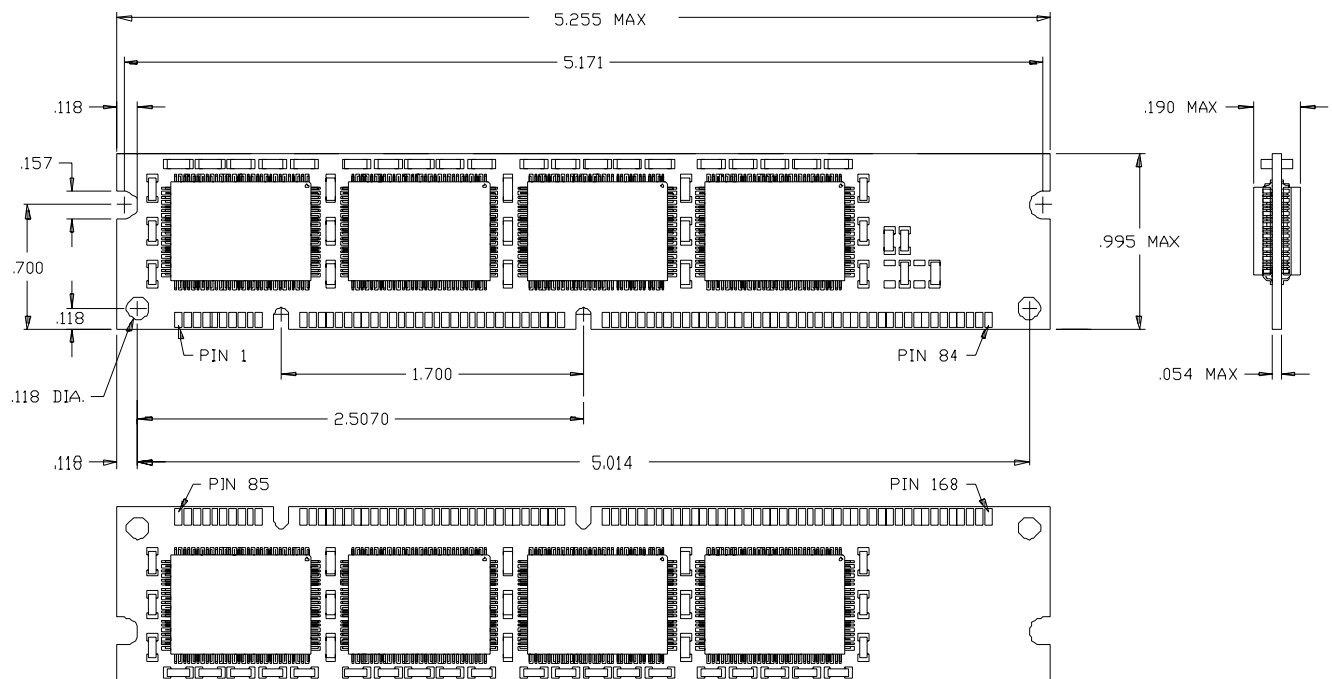
Speed (MHz)	Ordering Code	Package Name	Package Type	Description	Operating Range
50	CYM9260-50C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	Commercial
	CYM9261B-50C	PM43	168-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9262A-50C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9263-50C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	
66	CYM9260-66C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 64K x 72	
	CYM9261B-66C	PM43	168-Pin Dual-Readout SIMM (SIMM)	Sync 128K x 72	
	CYM9262A-66C	PM43	168-Pin Dual-Readout SIMM (DIMM)	Sync 256K x 72	
	CYM9263-66C	PM44	168-Pin Dual-Readout SIMM (DIMM)	Sync 512K x 72	

Package Diagrams

168-Pin Single-Sided DIMM PM43



168-Pin Dual Sided DIMM PM44





CYM9260
CYM9261B
CYM9262A
CYM9263

Document Title: CYM9260, CYM9261B, CYM9262A, CYM9263 64K/128K/256K/512K x 72 SRAM Module Document Number: 38-05002				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	114556	04/02/02	DSG	Change from Spec number: 38-M-00082 to 38-05002