LG Semicon. Co., LTD.

Description

The GM71C4403D/DL is the new generation dynamic RAM organized 1,048,576 words x 4 bit. GM71C4403D/DL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4403D/DL offers Extended Data Out (EDO) Mode as a high speed access Mode. Multiplexed address inputs permit the GM71C4403D/DL to be packaged in a standard 300mil 20pin plastic SOJ. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V±10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

- 1,048,576 Words x 4 Bit Organization
- Extended Data Out Mode Capability
- Single Power Supply (5V ± 10%)
- Fast Access Time & Cycle Time

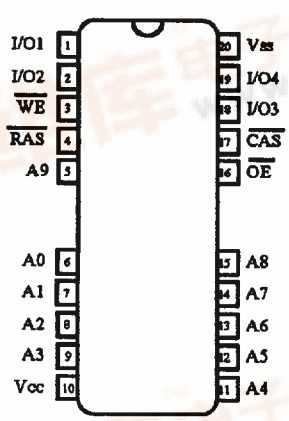
(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
GM71C4403D/DL-60	60	15	104	25
GM71C4403D/DL-70	70	18	124	30
GM71C4403D/DL-80	80	20	144	35

- Low Power
  Active : 440/385/358mW (MAX)
  Standby : 5.5mW (CMOS level : MAX)
  0.55mW (L-version)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-version)
- Battery Back Up Operation (L-version)

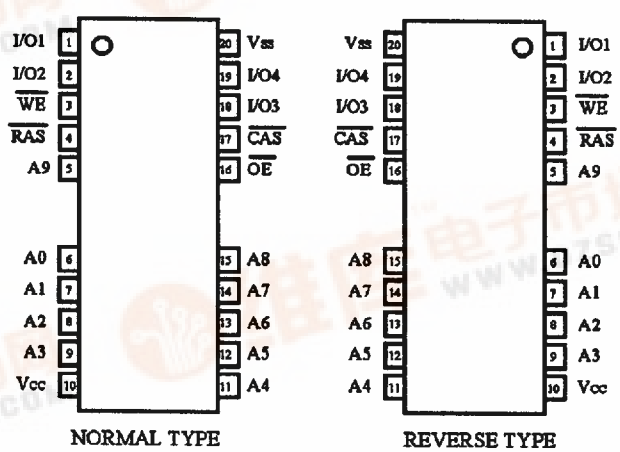
Pin Configuration

20 (26) SOJ



(Top View)

20 (26) TSOP II



(Top View)

Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	$\overline{WE}$	Read/Write Enable
A0-A9	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O1-I/O4	Data Input/Data Output	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe		

Ordering Information

Type No.	Access Time	Package
GM71C4403DJ/DLJ-60 GM71C4403DJ/DLJ-70 GM71C4403DJ/DLJ-80	60ns 70ns 80ns	300 Mil, 20 (26) Pin Plastic SOJ
GM71C4403DT/DLT-60 GM71C4403DT/DLT-70 GM71C4403DT/DLT-80	60ns 70ns 80ns	300 Mil, 20 (26) Pin Plastic TSOP II (Normal Type)
GM71C4403DR/DLR-60 GM71C4403DR/DLR-70 GM71C4403DR/DLR-80	60ns 70ns 80ns	300 Mil, 20 (26) Pin Plastic TSOP II (Reverse Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	℃
T_{STG}	Storage Temperature (Plastic)	-55 ~ 125	℃
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	-1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (All Voitages referenced to Vss, T_A = 0 ~ 70℃)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	-	6.5	V
V_{IL}	Input Low Voltage	-1.0	-	0.8	V

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	-	80	mA	1, 2
		70ns	-	70		
		80ns	-	65		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$= V_{IH}, D_{OUT} = High-Z)		-	2	mA	
I_{CC3}	$\overline{RAS}$-Only Refresh Current Average Power Supply Current $\overline{RAS}$-Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	-	80	mA	2
		70ns	-	70		
		80ns	-	65		
I_{CC4}	Extended Data Out Mode Current Average Power Supply Current Extended Data Out Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{HPC} = t_{HPC} min)	60ns	-	80	mA	1, 3
		70ns	-	70		
		80ns	-	65		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$= V_{IH}, $\overline{WE}$, $\overline{OE}$, Address and D_{IN}=V_{IH} orV_{IL}, D_{OUT}=High-Z)		-	1	mA	5
			-	100	μA	4,5
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	-	80	mA	
		70ns	-	70		
		80ns	-	65		
I_{CC7}	Battery Back Up Current (Standby with CBR Refresh) (t_{RC}=125 μs, t_{RAS} ≤ 1 μs, $\overline{WE}$=V_{IH}, $\overline{CAS}$=V_{IL}, $\overline{OE}$, Address and D_{IN}=V_{IH} orV_{IL}, D_{OUT}=High-Z)		-	300	μA	4, 5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		-	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		-10	10	μA	

Note: 1. I_{CC} depends on output load condition when the device is selected. I_{CC}(max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.
4. L Series.
5. V_{CC}-0.2V ≤ V_{IH} ≤ 6.5V, 0V ≤ V_{IL} ≤ 0.2V.

Capacitance (V_{CC} = 5V ± 10%, T_A = 25℃)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	-	5	pF	1
C_{I2}	Input Capacitance (Clocks)	-	7	pF	1
$C_{I/O}$	Data Input/Output Capacitance (Data-In/Out)	-	7	pF	1, 2

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70℃, Notes 1, 14, 15, 16)

Test Conditions

Input level : V_{IL}=0V, V_{IH}=3.0V
Input rise and fall times: 2ns
Input timing reference levels: V_{IL}=0.8V, V_{IH}=2.4V
Output timing reference levels: V_{OL}=0.8V, V_{OH}=2.0V
Output load : 1 TTL gate + C_L (100pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	104	-	124	-	144	-	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	19
t_{CAS}	$\overline{CAS}$ Pulse Width	12	10,000	15	10,000	15	10,000	ns	20
t_{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
t_{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
t_{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
t_{CAH}	Column Address Hold Time	10	-	13	-	15	-	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	-	18	-	20	-	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	48	-	58	-	68	-	ns	22
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	-	10	-	10	-	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	-	0	-	0	-	ns	
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	-	0	-	0	-	ns	
t_T	TransitionTime (Rise and Fall)	2	50	2	50	2	50	ns	7
t_{REF}	Refresh Period	-	16	-	16	-	16	ms	
	Refresh Period (L-version)	-	128	-	128	-	128	ms	

Read Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	2,3,17
t_{CAC}	Access Time from $\overline{CAS}$	-	15	-	18	-	20	ns	3, 4, 13, 17
t_{AA}	Access Time from Address	-	30	-	35	-	40	ns	3, 5, 13, 17
t_{OAC}	Access Time from $\overline{OE}$	-	15	-	18	-	20	ns	3,17
t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	18
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	18
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	18	-	23	-	28	-	ns	
t_{OFF}	Output Buffer Turn-off Time	-	15	-	20	-	20	ns	6,21
t_{OEZ}	Output Buffer Turn-off Time from $\overline{OE}$	-	15	-	20	-	20	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	
t_{RDD}	$\overline{RAS}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	
t_{WDD}	$\overline{WE}$ to D_{IN} Delay Time	15	-	18	-	20	-	ns	
t_{OEP}	$\overline{OE}$ Pulse width	15	-	18	-	20	-	ns	
t_{OFR}	Output Buffer Turn-off Time to $\overline{RAS}$	-	15	-	15	-	15	ns	6,21
t_{WEZ}	Output Buffer Turn-off Time to $\overline{WE}$	-	15	-	15	-	15	ns	6
t_{OH}	Output Data Hold Time	5	-	5	-	5	-	ns	
t_{OHR}	Output Data Hold Time form $\overline{RAS}$	5	-	5	-	5	-	ns	
t_{RCHR}	Read Command Hold Time from $\overline{RAS}$	60	-	70	-	80	-	ns	
t_{RCHC}	Read Command Hold Time from $\overline{CAS}$	15	-	18	-	20	-	ns	
t_{RCHA}	Read Command Hold Time from Column Address	30	-	35	-	40	-	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	-	0	-	0	-	ns	

Write Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	10
t_{WCH}	Write Command Hold Time	10	-	13	-	15	-	ns	
t_{WP}	Write Command Pulse Width	10	-	10	-	10	-	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	-	13	-	15	-	ns	
t_{DS}	Data-in Setup Time	0	-	0	-	0	-	ns	11
t_{DH}	Data-in Hold Time	10	-	13	-	15	-	ns	11

Read- Modify-Write Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	133	-	159	-	183	-	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	77	-	90	-	102	-	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	32	-	38	-	42	-	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	47	-	55	-	62	-	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	-	18	-	20	-	ns	

Refresh Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	-	10	-	10	-	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	-	10	-	10	-	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	-	10	-	10	-	ns	

Extended Data Out (EDO) Mode Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	23
t_{CP}	EDO Mode $\overline{CAS}$ Precharge Time	8	-	10	-	15	-	ns	
t_{RASP}	EDO Mode $\overline{RAS}$ Pulse Width	60	100,000	70	100,000	80	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	-	35	-	40	-	45	ns	3,13,17
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{CPW}	EDO Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	52	-	60	-	67	-	ns	10
t_{HPRWC}	EDO Mode Read-Modify-Write Cycle Time	66	-	75	-	85	-	ns	
t_{COL}	$\overline{CAS}$ Hold Time Referred $\overline{OE}$	10	-	13	-	20	-	ns	
t_{COP}	$\overline{CAS}$ to $\overline{OE}$ setup Time	5	-	5	-	5	-	ns	
t_{RCHP}	Read Command Hold Time from $\overline{CAS}$ Precharge	35	-	40	-	45	-	ns	
t_{DOH}	Output data hold time from $\overline{CAS}$ low	3	-	3	-	3	-	ns	

Test Mode Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WS}	Test Mode $\overline{WE}$ Setup Time	0	-	0	-	0	-	ns	
t_{WH}	Test Mode $\overline{WE}$ Hold Time	10	-	10	-	10	-	ns	

Counter Test Cycle

Symbol	Parameter	GM71C4403 D/DL-60		GM71C4403 D/DL-70		GM71C4403 D/DL-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	40	-	40	-	40	-	ns	

Notes:

1. AC measurements assume $t_T = 2ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a lode circuit equivalent to 1 TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$, $t_{OEZ}(max)$, $t_{OFR}(max)$ and $t_{WEZ}(max)$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals.Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or a read modify write cycle.
12. t_{RASP} defines $\overline{RAS}$ pulse width in extended data out mode cycles.
13. Access time is determined by the longest among t_{AA}, t_{CAC} and t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eitht $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2bits test function controlled by control address bit CA0. This test mode operaiton can be performed by $\overline{WE}$-and-$\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is low level. In order to end this test mode operation, perform $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

18. Either t_{RCH} or t_{RRH} must be satisfied.
19. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in Read - Modify - Write cycle.
20. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in Read - Modify - Write cycle.
21. t_{OFF} and t_{OFR} are determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
22. $t_{CSH}(min)$ can be achieved when $t_{RCD} \leq t_{CSH}(min) - t_{CAS}(min)$.
23. EDO Hi-Z control by $\overline{OE}$ or $\overline{WE}$. $\overline{OE}$ rising edge disables data outputs. When $\overline{OE}$ goes high during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access. When $\overline{WE}$ goes low during $\overline{CAS}$ high, the data will not come out until next $\overline{CAS}$ access.
24. $t_{HPC}(min)$ can be achieved during a series of EDO mode write cycles or EDO mode read cycles. If both write and read operation are mixed in a EDO mode $\overline{RAS}$ cycle(EDO mode mix cycle (1),(2)) minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2t_T$) becomes greater than the specified $t_{HPC}(min)$ value.The value of $\overline{CAS}$ cycle time of mixed EDO mode is shown in EDO mode mix cycle (1) and (2).

Timing Waveforms

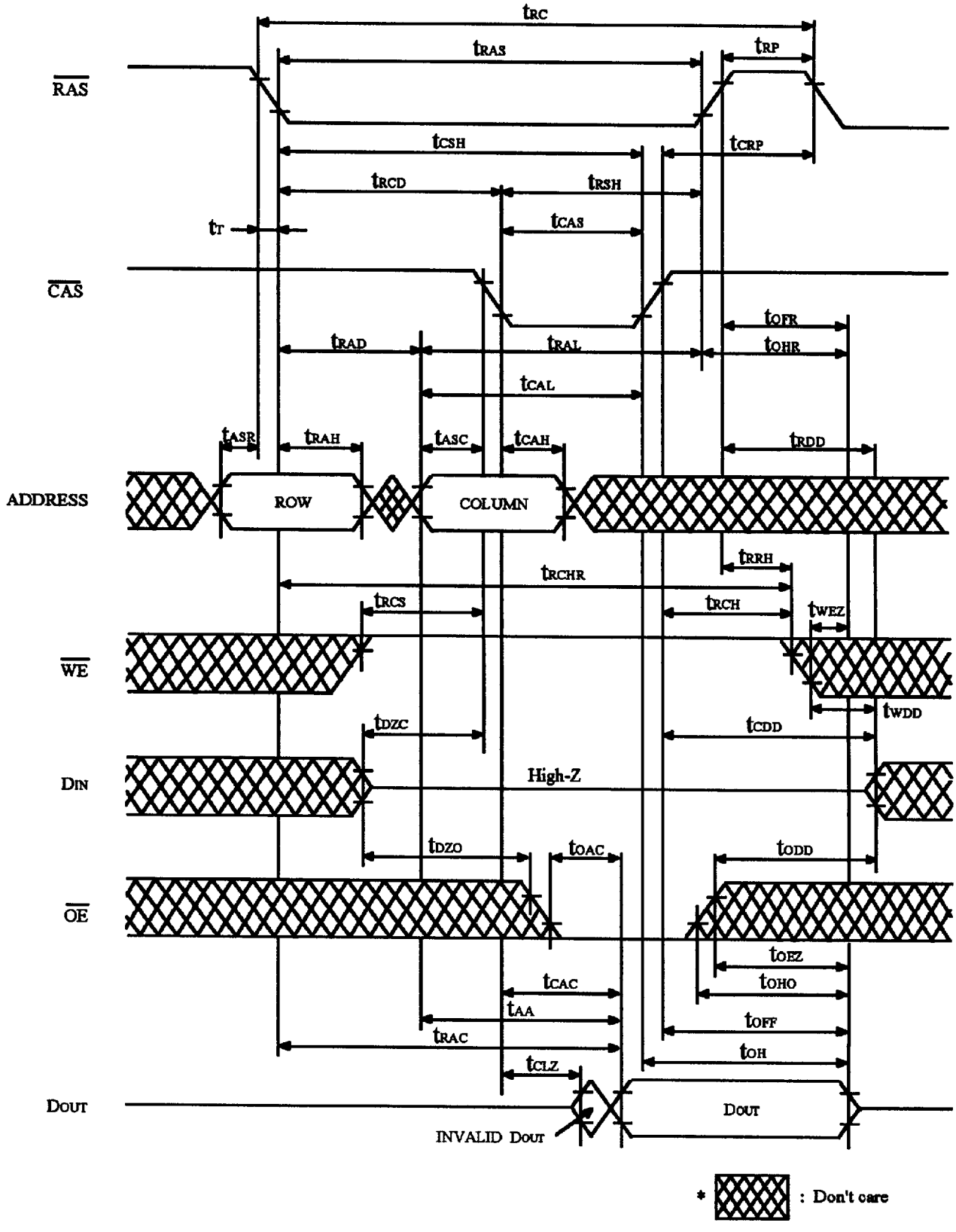


FIGURE 1. READ CYCLE

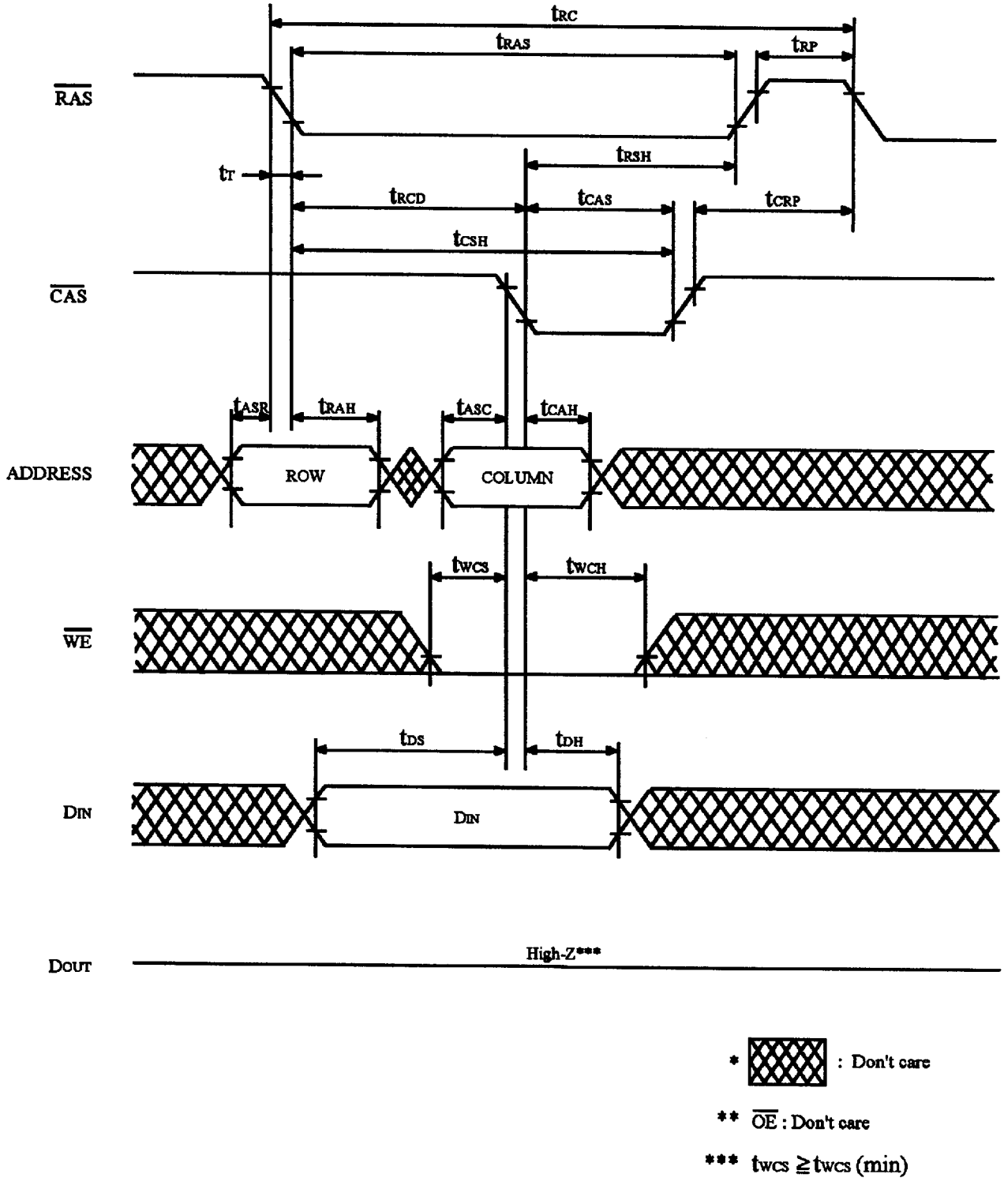


FIGURE 2. EARLY WRITE CYCLE

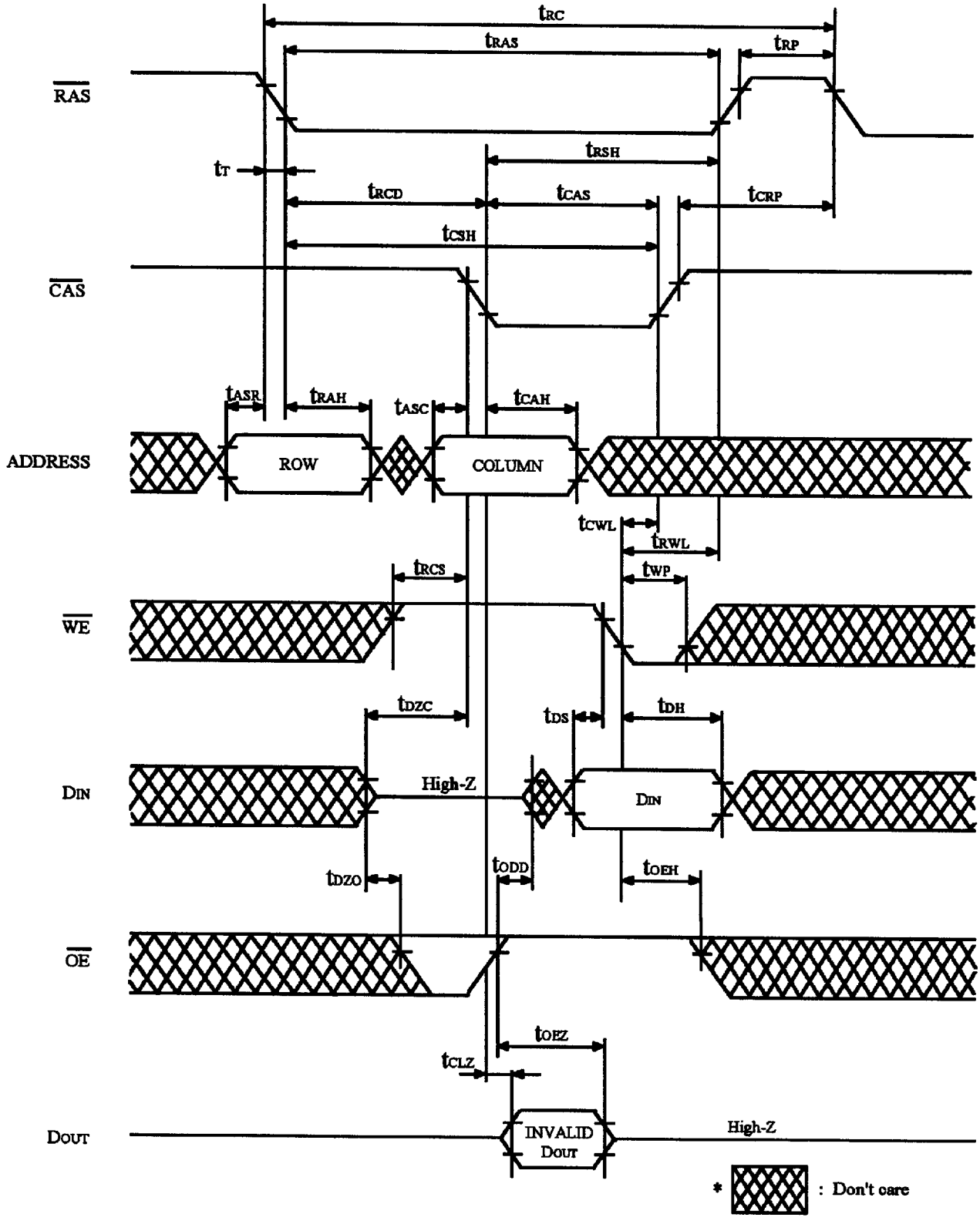


FIGURE 3. DELAYED WRITE CYCLE *18

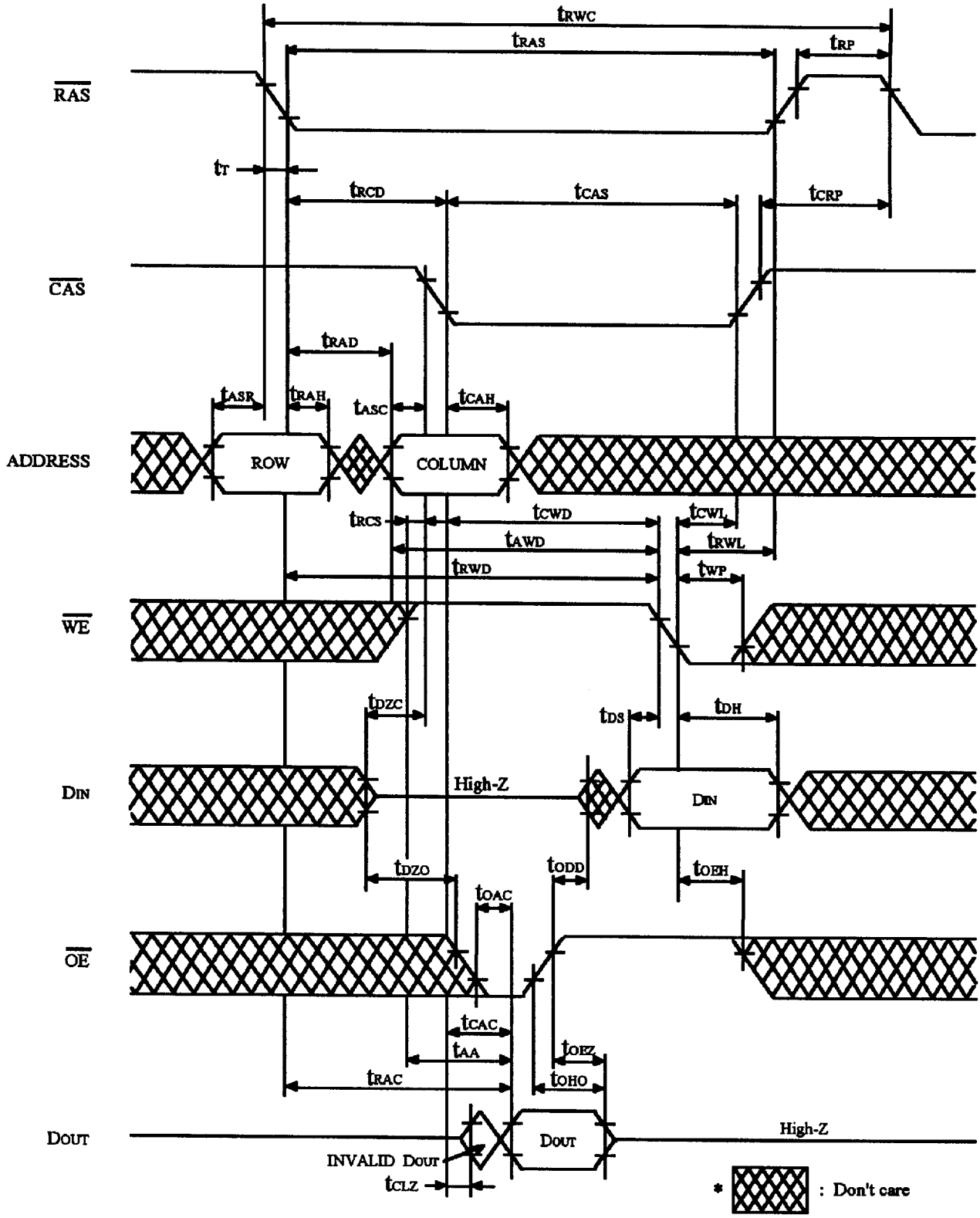
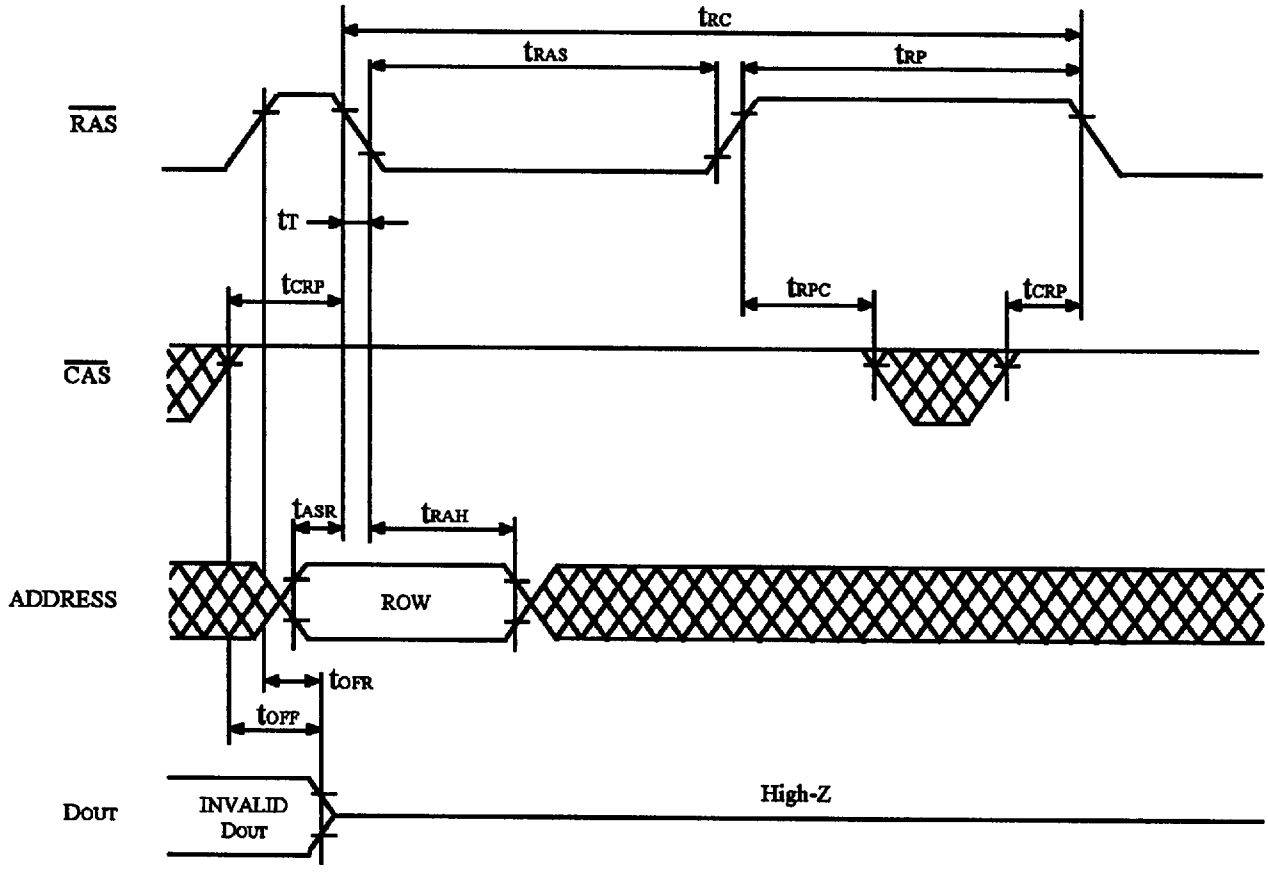


FIGURE 4. READ MODIFY WRITE CYCLE [*18]

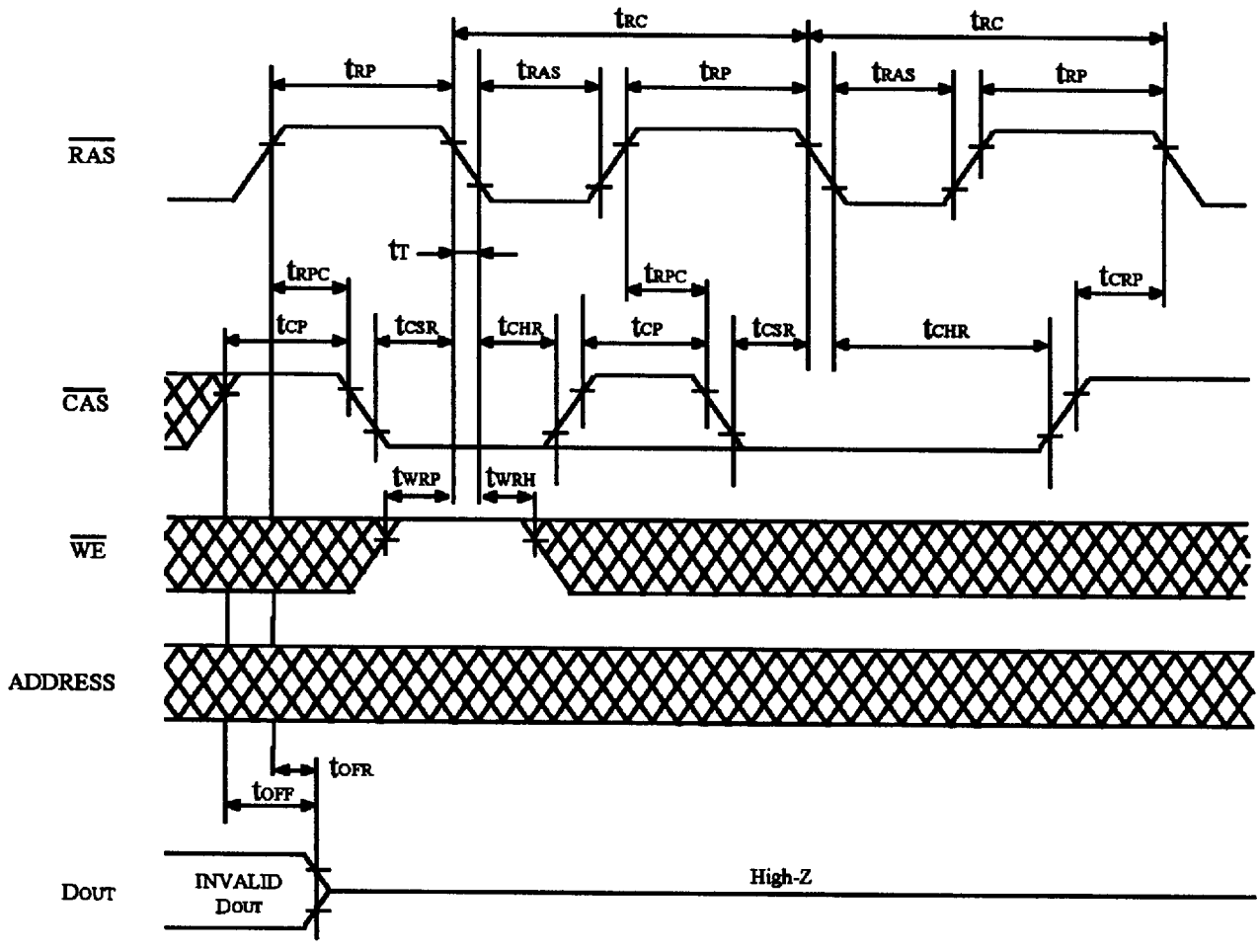


* : Don't care

** $\overline{OE}$, $\overline{WE}$: Don't care

*** Refresh Address: A0-A9 (RA0-RA9)

FIGURE 5. $\overline{RAS}$ ONLY REFRESH CYCLE



* : Don't care

** $\overline{OE}$: Don't care

FIGURE 6. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

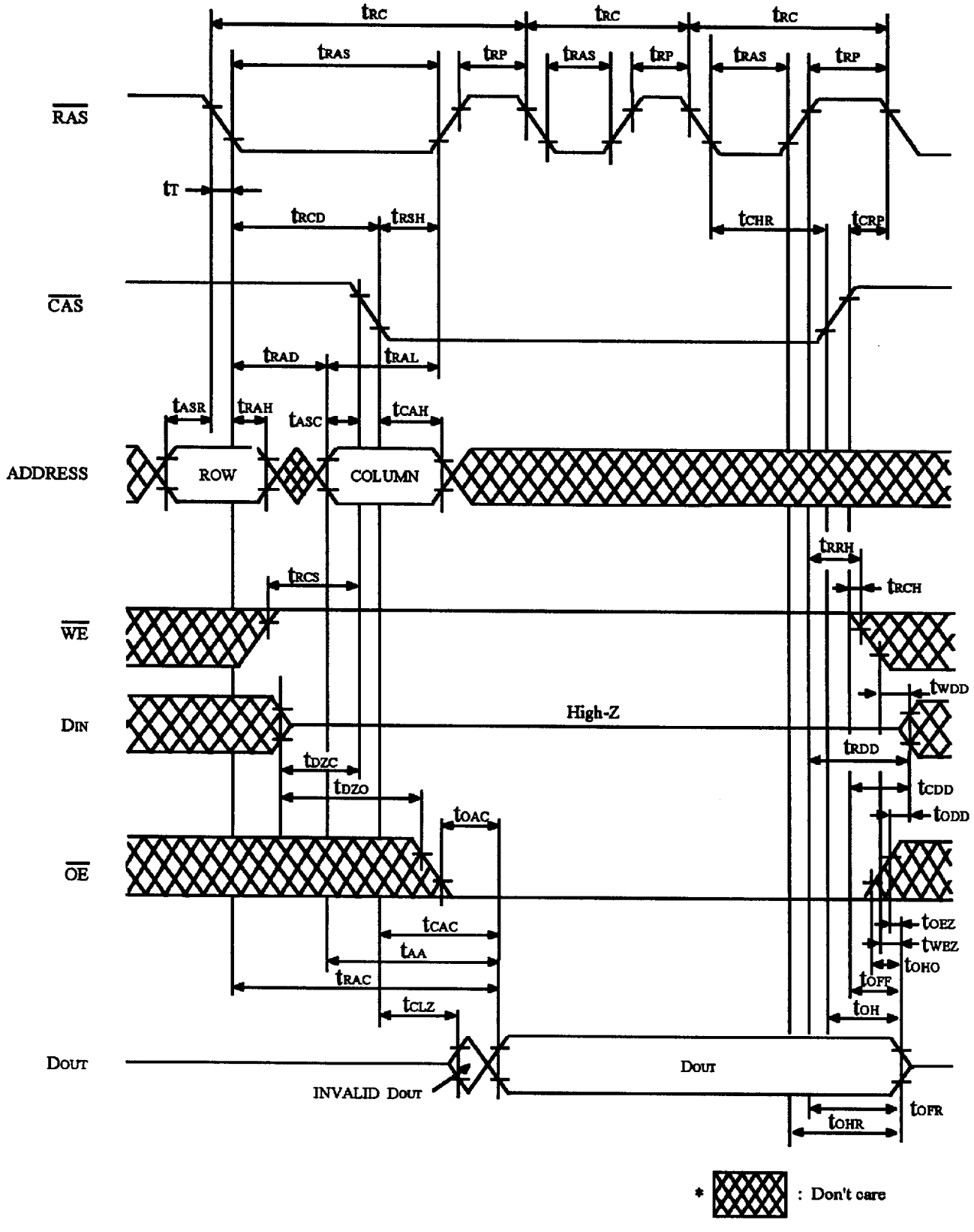


FIGURE 7. HIDDEN REFRESH CYCLE

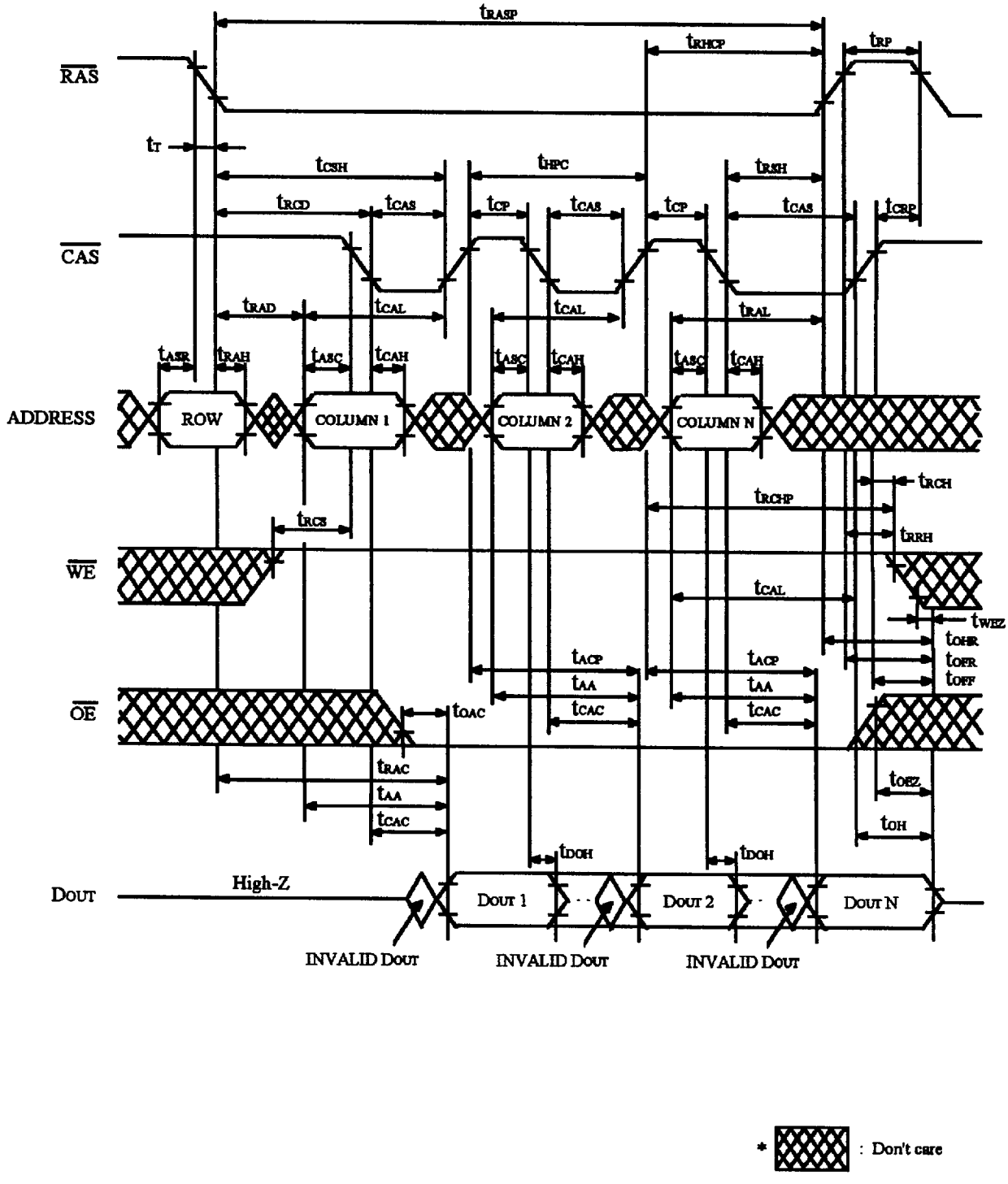


FIGURE 8. EXTENDED DATA OUT MODE READ CYCLE

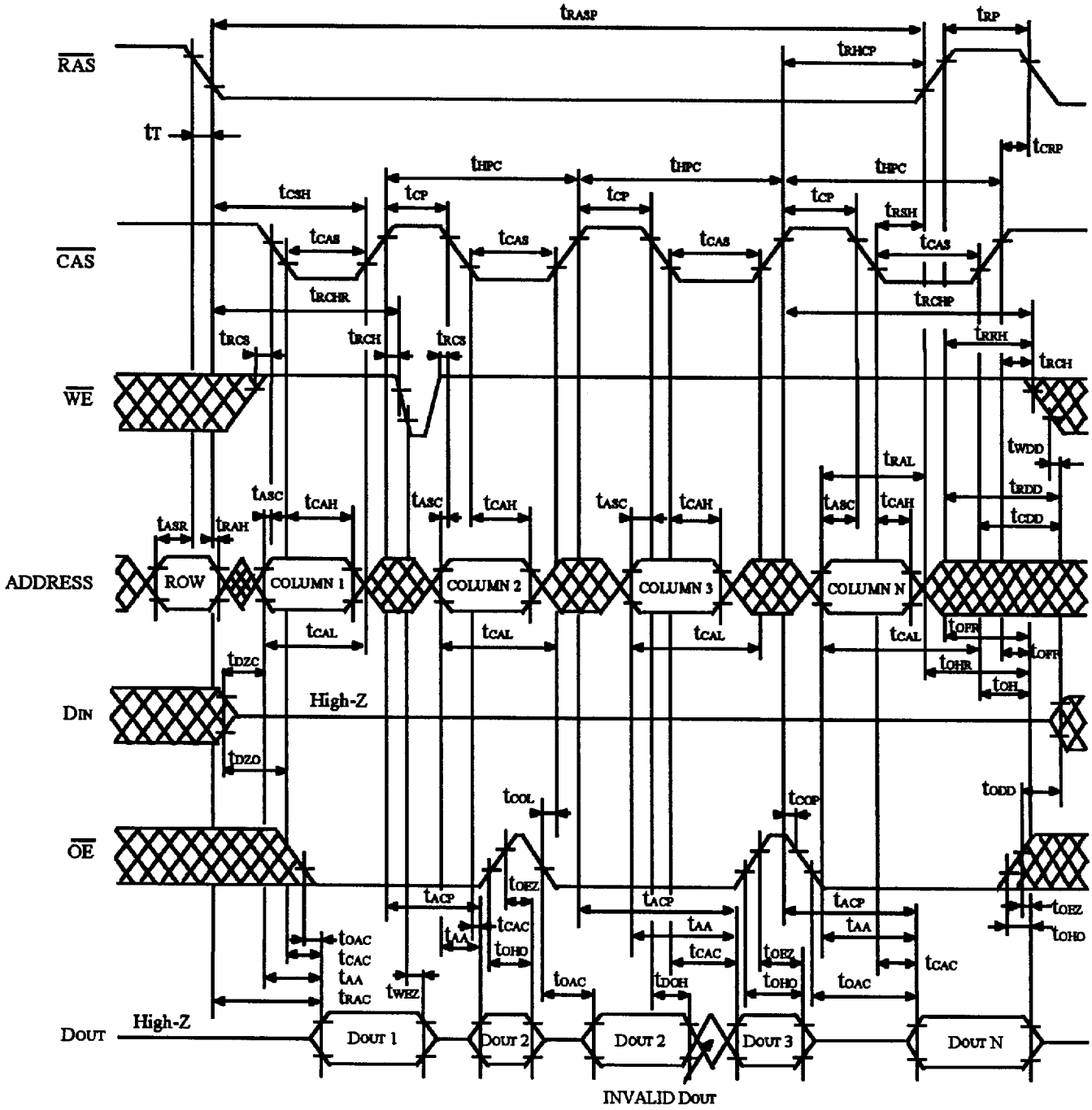


FIGURE 9. EXTENDED DATA OUT MODE READ CYCLE ($\overline{OE}$ CONTROL) [23]

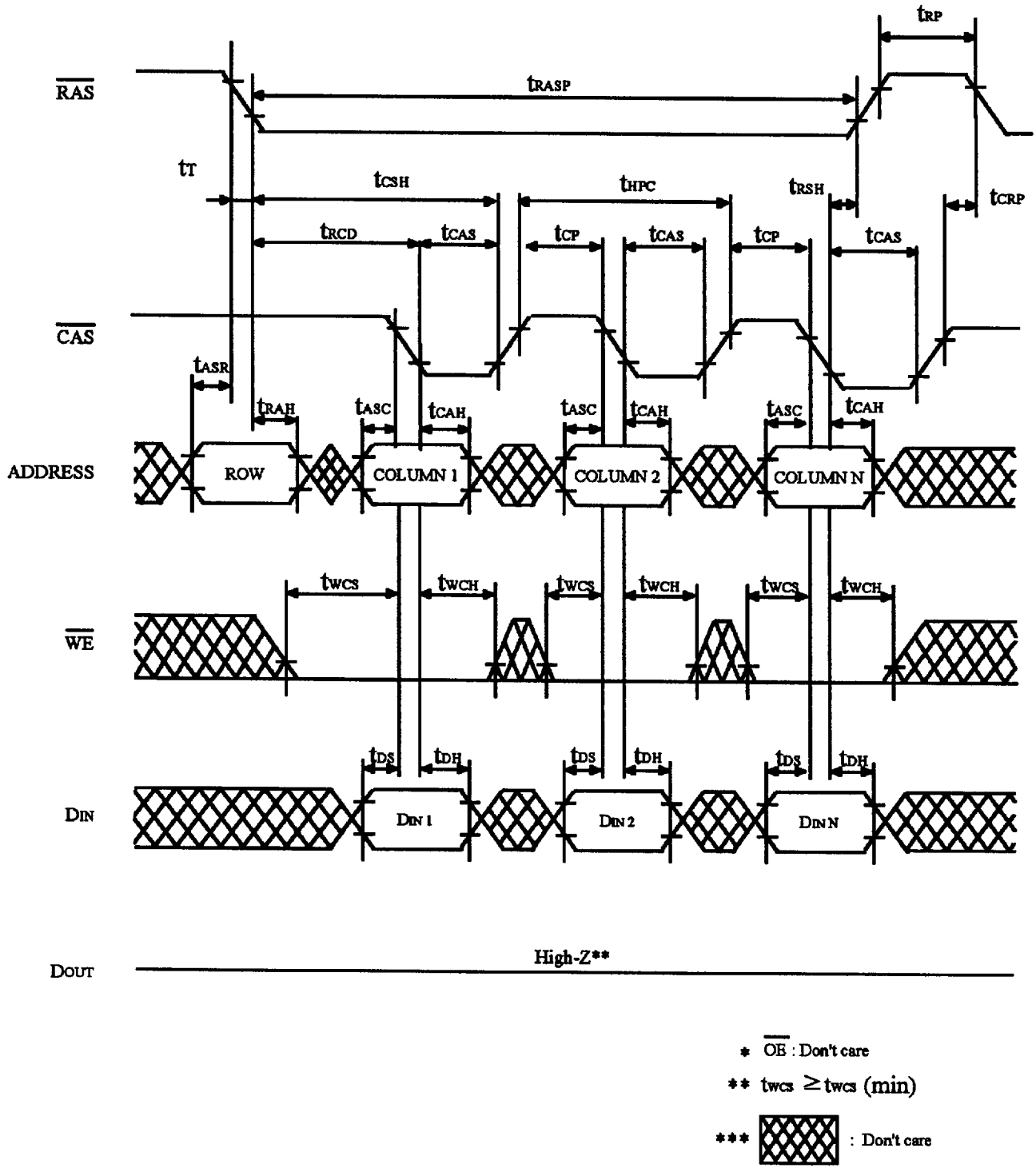


FIGURE 10. EXTENDED DATA OUT MODE EARLY WRITE CYCLE

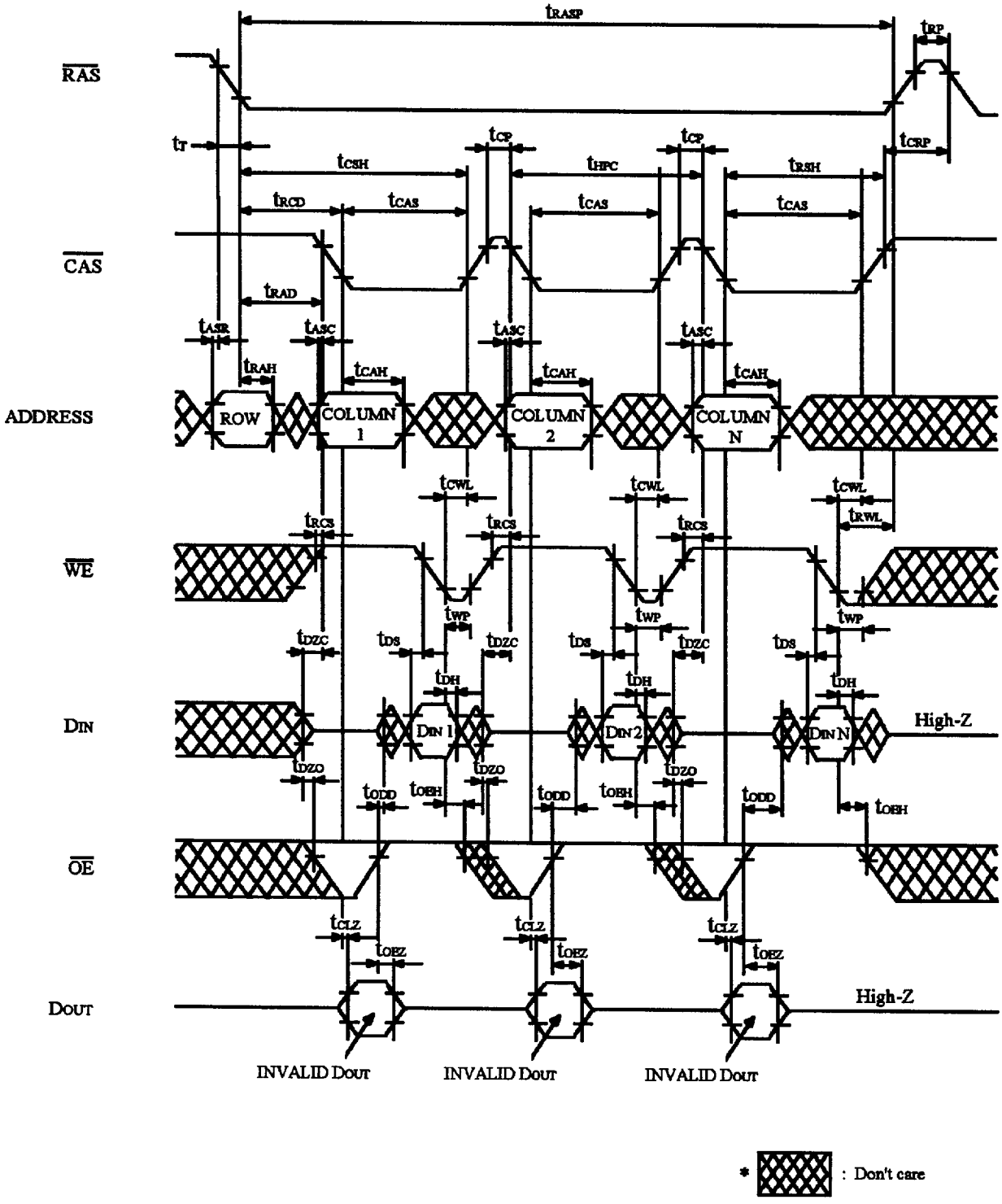


FIGURE 11. EXTENDED DATA OUT MODE DELAYED WRITE CYCLE *18

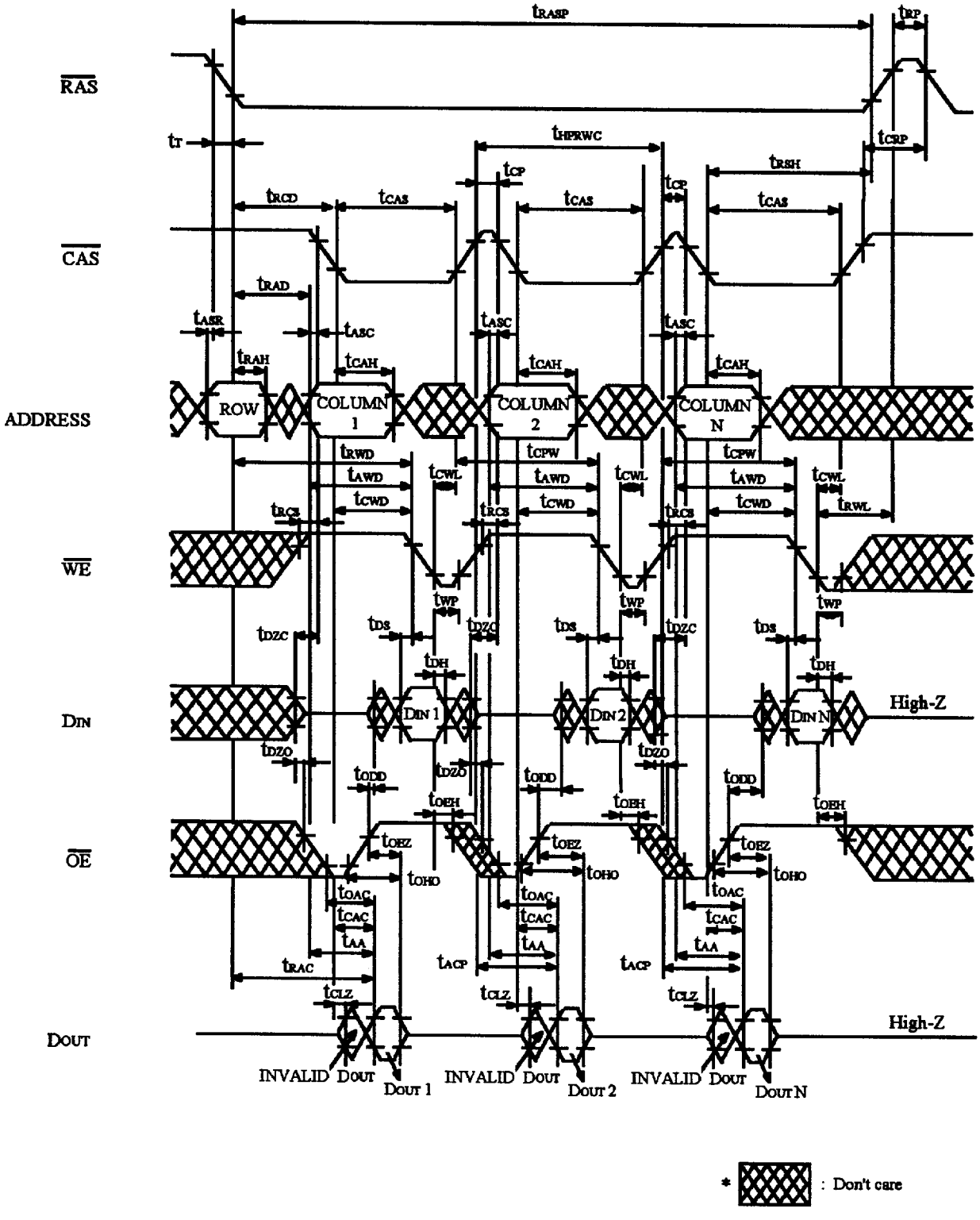


FIGURE 12. EXTENDED DATA OUT MODE READ MODIFY WRITE CYCLE [18]

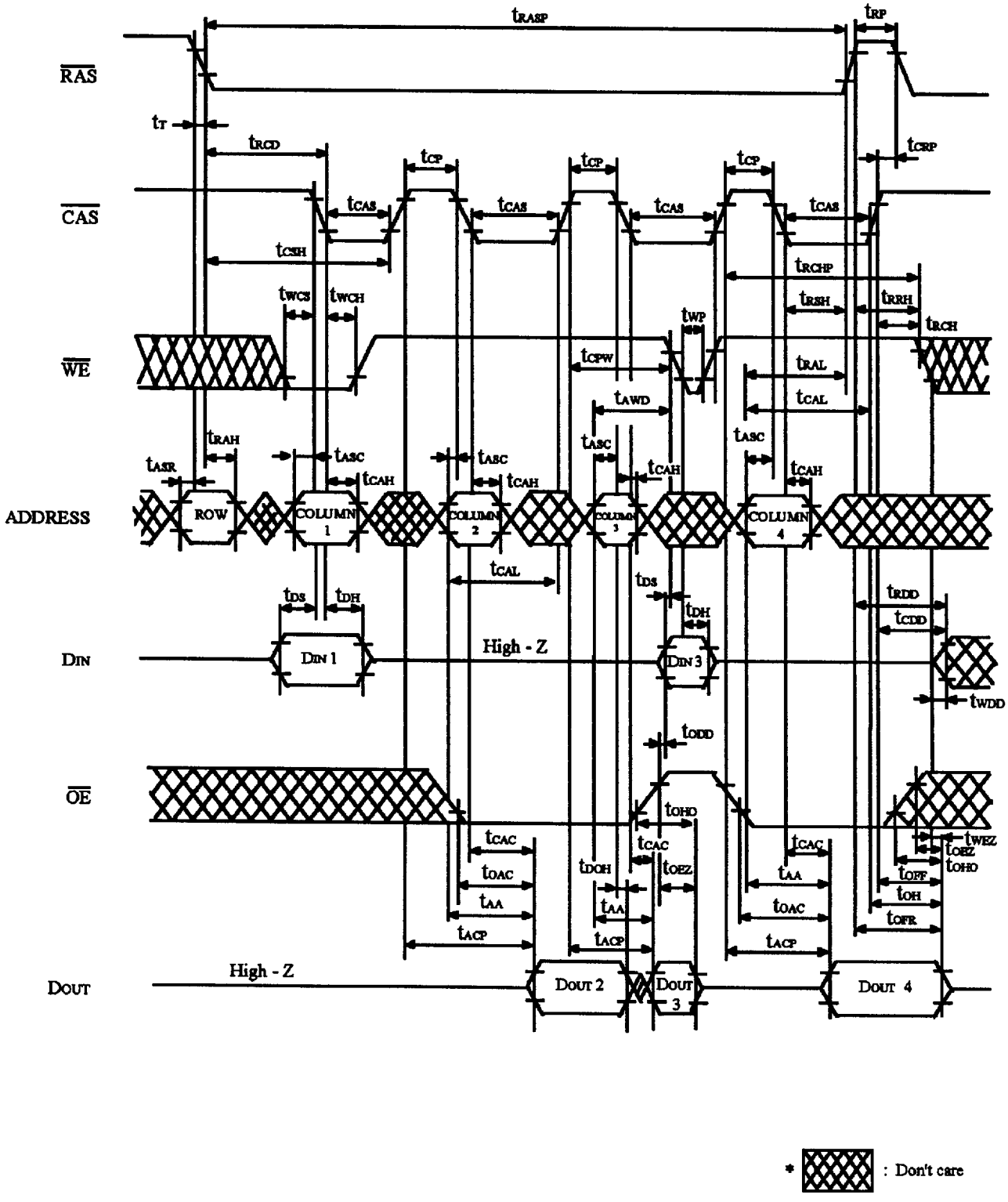


FIGURE 13. EXTENDED DATA OUT MODE MIX CYCLE (1) [24]

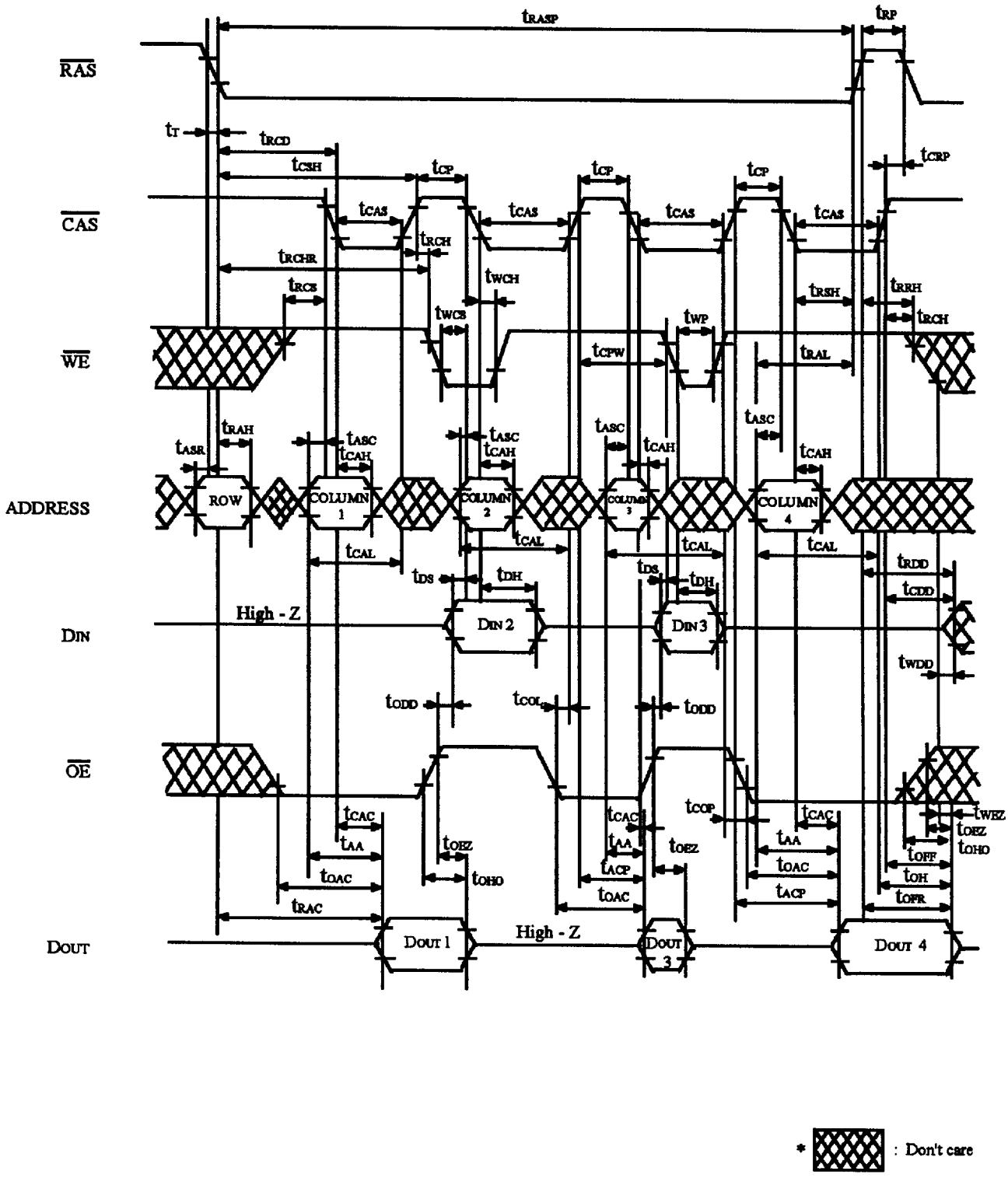


FIGURE 14. EXTENDED DATA OUT MODE MIX CYCLE (2) [24]

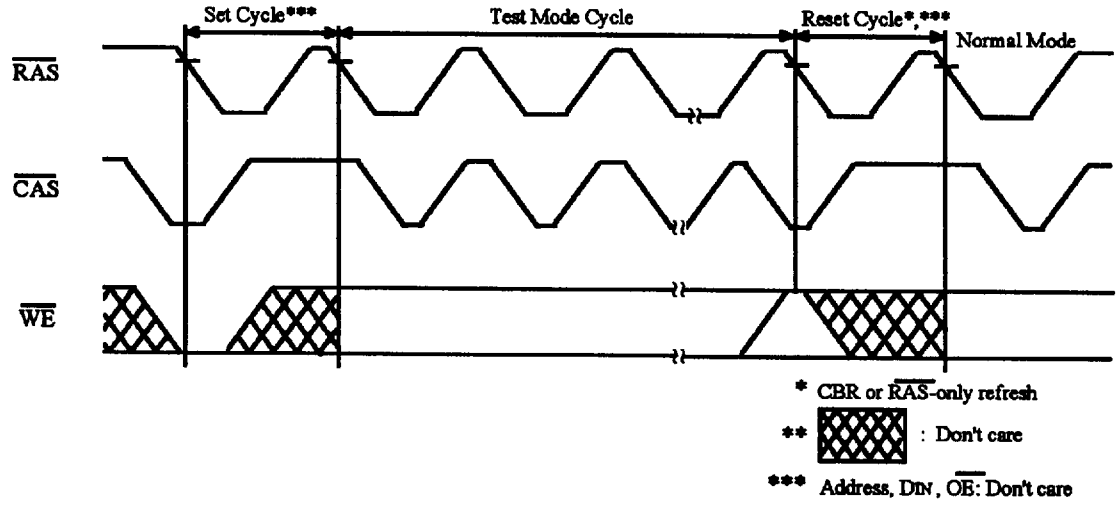


FIGURE 15. TEST MODE CYCLE

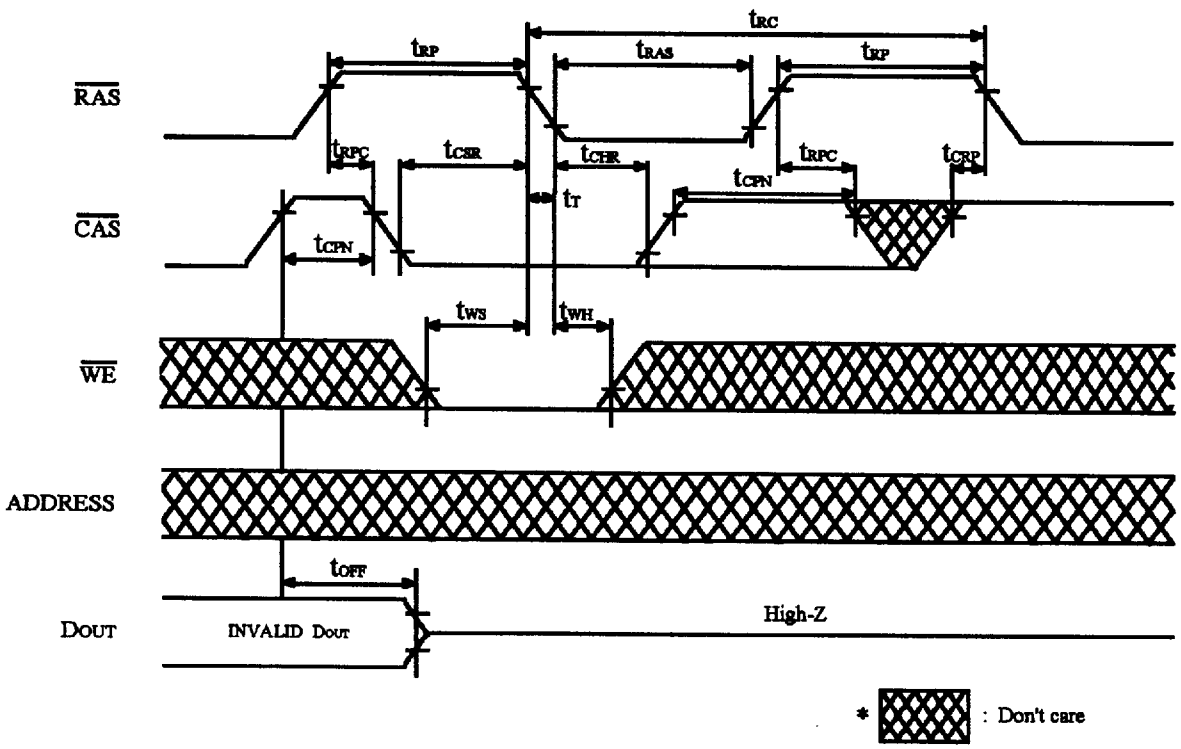


FIGURE 16. TEST MODE SET CYCLE

Test Mode Reset Cycle

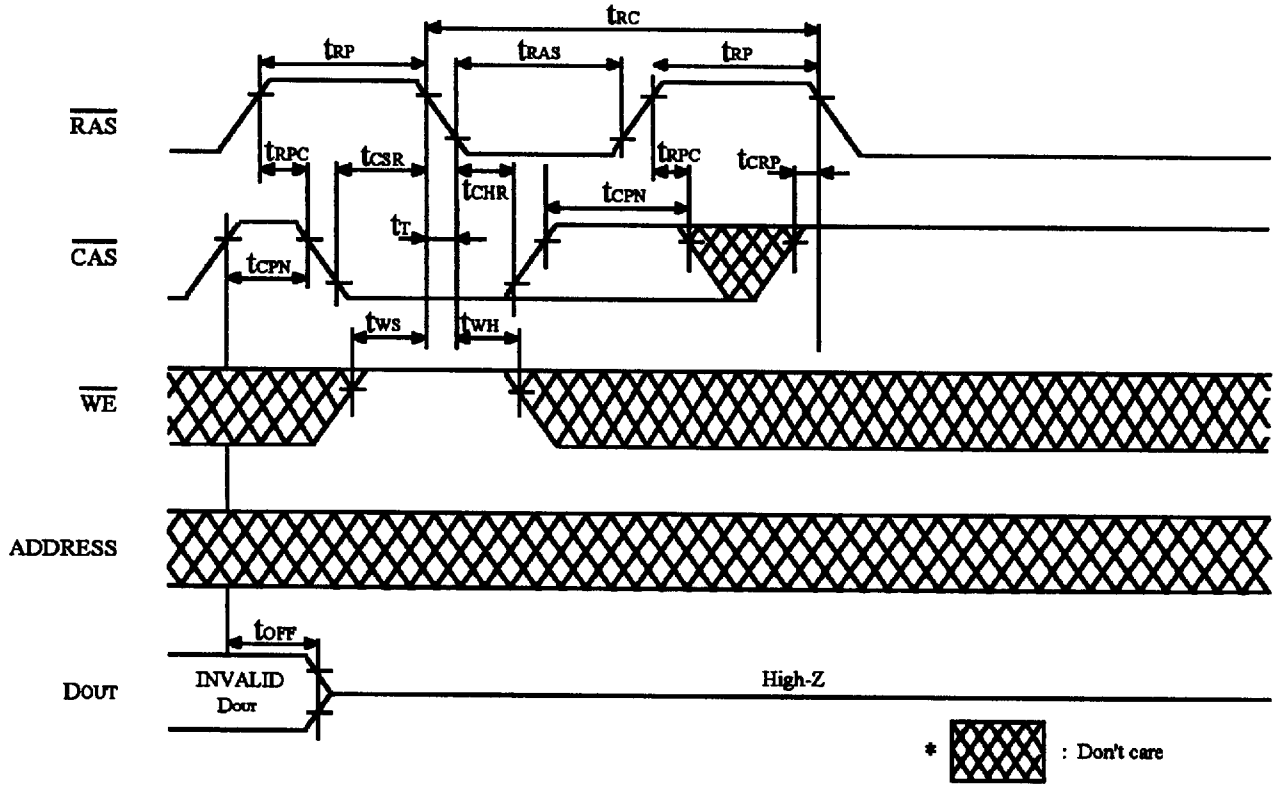


FIGURE 17. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

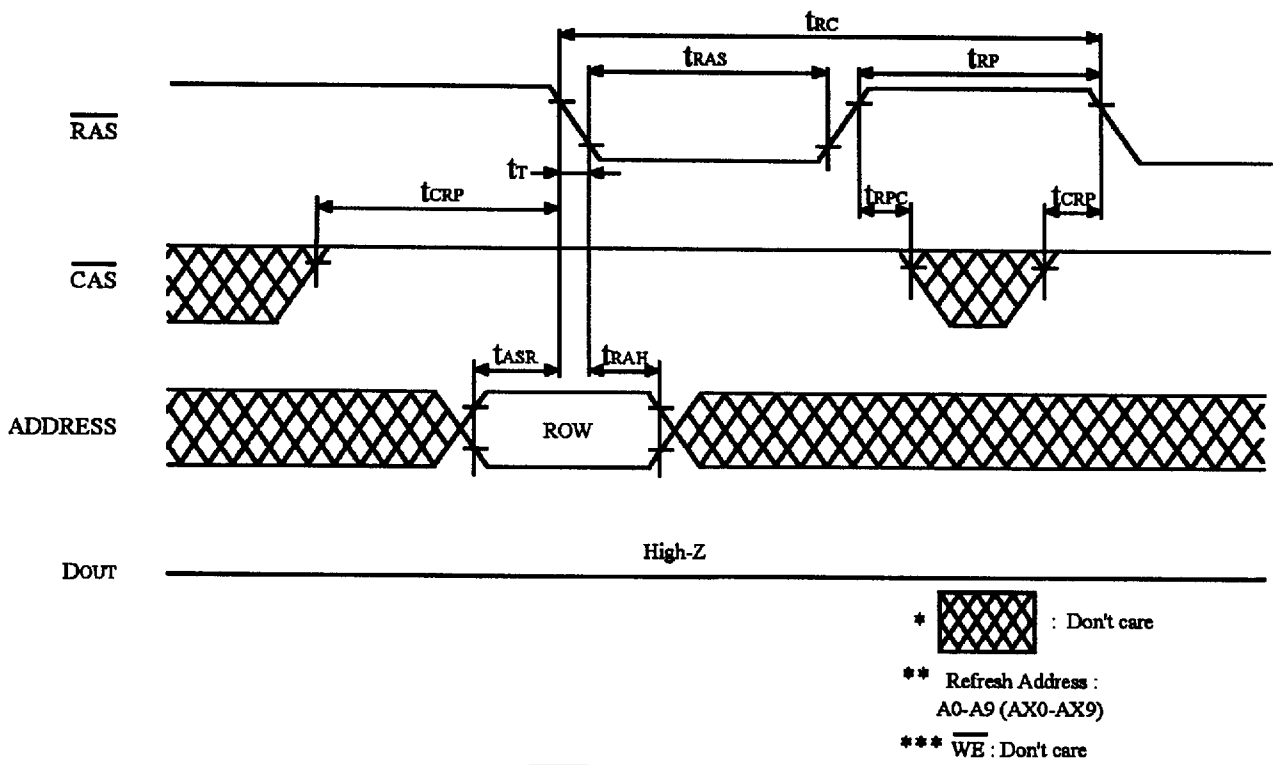


FIGURE 18. $\overline{RAS}$ ONLY REFRESH CYCLE

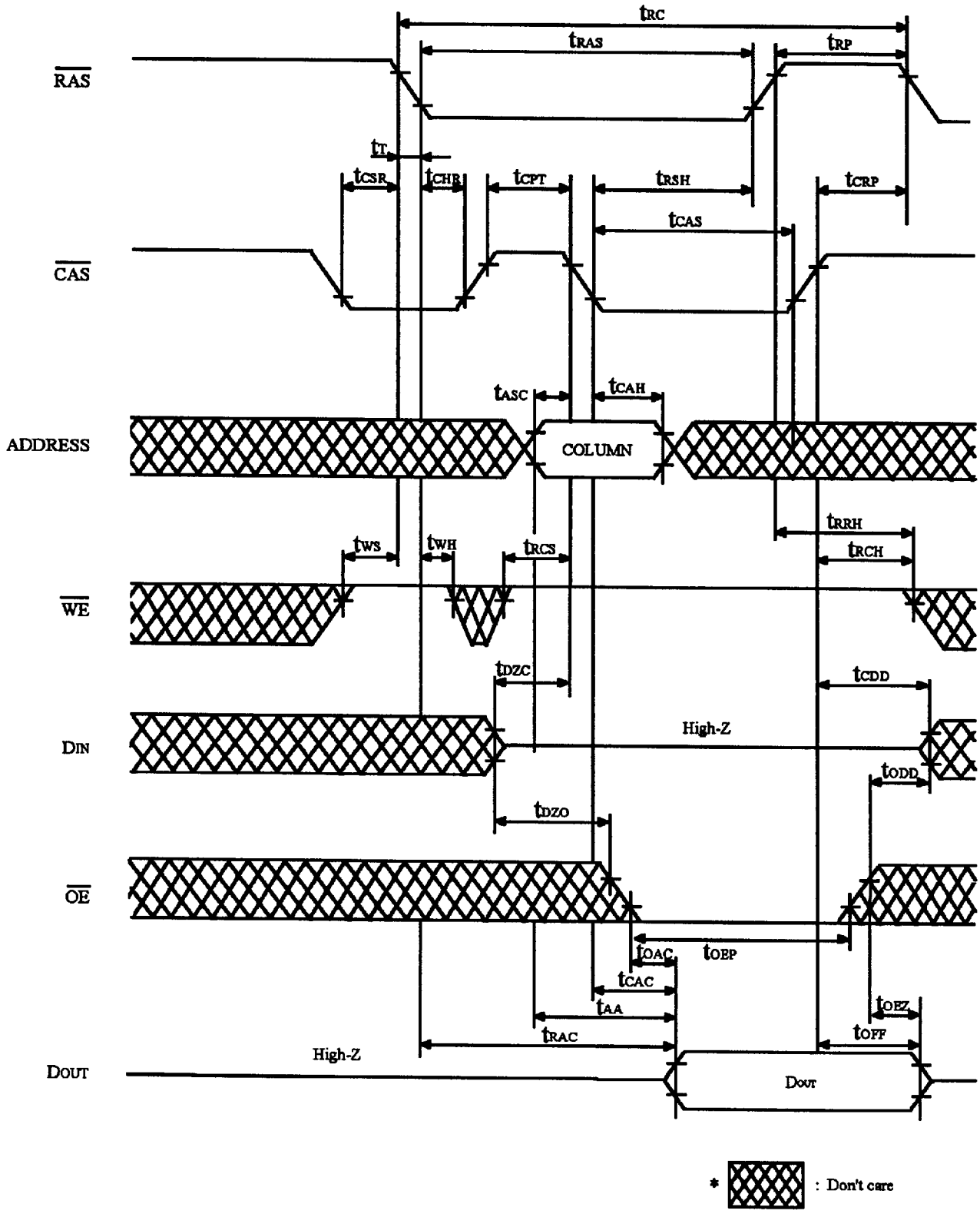


FIGURE 19. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

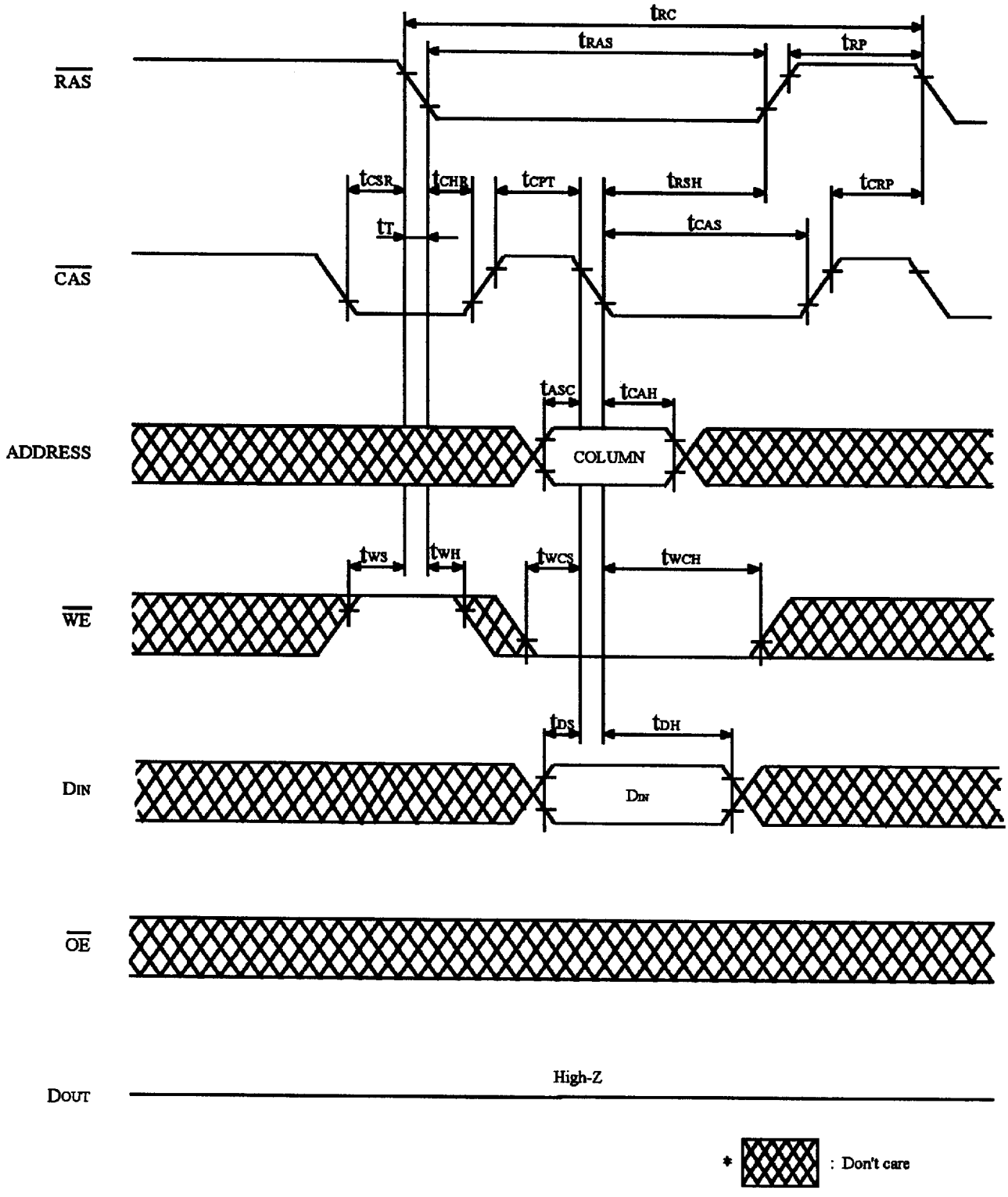
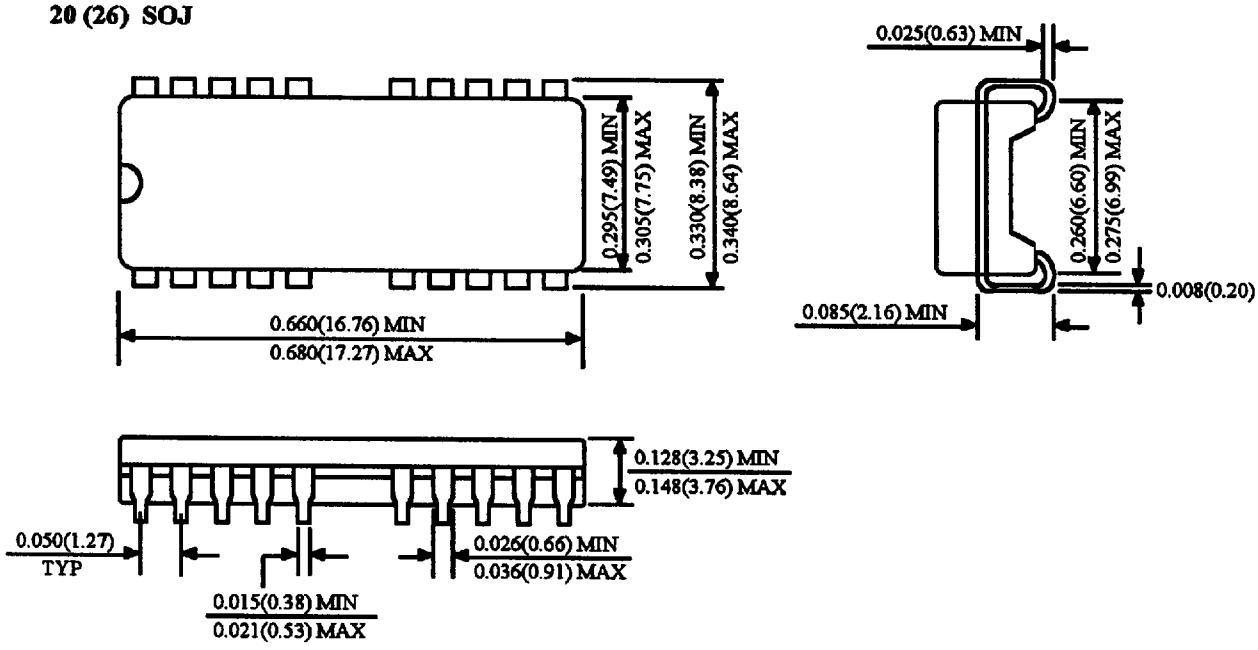


FIGURE 20. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (WRITE)

Package Dimension

Unit: Inches (mm)

20 (26) SOJ



20 (26) TSOP (TYPE. II)