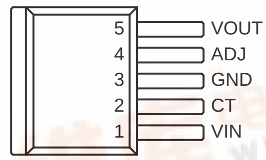
Unitrode Products
from Texas Instruments

UCC283-3, UCC283-5, UCC283-ADJ, UCC383-3, UCC383-5, UCC383-ADJ
LOW-DROPOUT 3-A LINEAR REGULATOR FAMILY

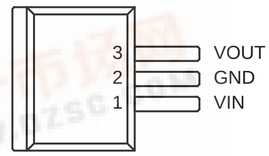
SLUS215B − OCTOBER 1998 − REVISED FEBRUARY 2004

- **Precision Positive Linear Series Pass Voltage Regulation**
- **0.45 V Dropout at 3 A**
- **50 mV Dropout at 10 mA**
- **Quiescent Current Under 650 µA Irrespective of Load**
- **Adjustable (5-Lead) Output Voltage Version**
- **Fixed (3-Lead) Versions for 3.3-V and 5-V Outputs**
- **Logic Shutdown Capability**
- **Short-Circuit Power Limit of ($3\% \times V_{IN} \times I_{SHORT}$)**
- **Low V_{OUT} to V_{IN} Reverse Leakage**
- **Thermal Shutdown**

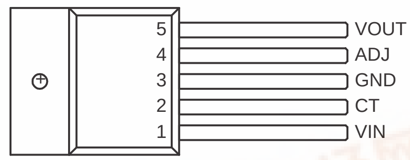
TO−263−5 TD PACKAGE (FRONT VIEW)



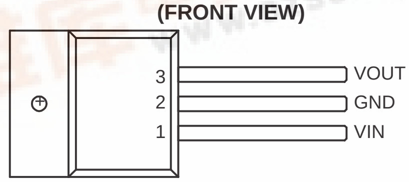
TO−263−3 TD PACKAGE (FRONT VIEW)



TO−220−5 T PACKAGE (FRONT VIEW)



TO−220−3 T PACKAGE (FRONT VIEW)



description

The UCC283−3/−5/−ADJ family of positive linear series pass voltage regulators are tailored for low-drop-out applications where low quiescent power is important. Fabricated with a BiCMOS technology ideally suited for low input-to-output differential applications, the UCC283−5 passes 3 A while requiring only 0.45 V of typical input voltage headroom (ensured 0.6-V dropout).

These regulators include reverse voltage sensing that prevents current in the reverse direction. Quiescent current is always less than 650 µA. These devices have been internally compensated in such a way that the need for a minimum output capacitor has been eliminated.

UCC283−3 and UCC283−5 versions are in 3-lead packages and have preset outputs at 3.3 V and 5.0 V respectively. The output voltage is regulated to 1.5% at room temperature. The UCC283−ADJ version, in a 5-lead package, regulates the output voltage programmed by an external resistor ratio.

Short-circuit current is internally limited. The device responds to a sustained overcurrent condition by turning off after a t_{ON} time delay. The device then stays off for a period, t_{OFF}, that is 32 times the t_{ON} delay. The device then begins pulsing on and off at the $t_{ON}/(t_{ON}+t_{OFF})$ duty cycle of 3%. This drastically reduces the power dissipation during short-circuit and means heat sinks need only accommodate normal operation. On the 3-leaded versions of the device t_{ON} is fixed at 750 µs, on the adjustable 5-leaded versions an external capacitor sets the on time. The off time is always $32 \times t_{ON}$. The external timing control pin, CT, on the 5-leaded versions also serves as a shutdown input when pulled low.

Internal power dissipation is further controlled with thermal overload protection circuitry. Thermal shutdown occurs if the junction temperature exceeds 165°C. The chip remains off until the temperature has dropped 20°C.

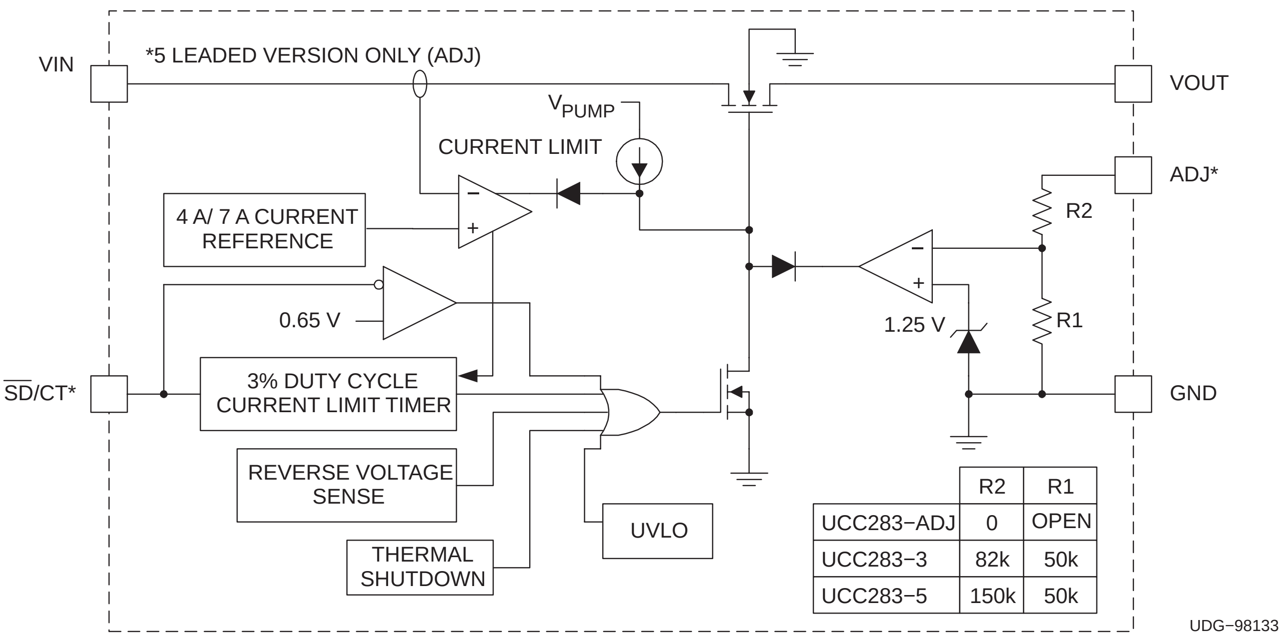
The UCC283 series is specified for operation over the industrial range of −40°C to 85°C, and the UCC383 series is specified from 0°C to 70°C. These devices are available in 3- and 5-pin TO−220 and TO−263 power packages.

AVAILABLE OPTIONS(1)

T_A	OUTPUT VOLTAGE (V)			PACKAGE DEVICES			
				TO−263−3(2)	TO−263−5(2)	TO−220−3	TO−220−5
	MIN	TYP	MAX	TD		T	
−40°C to 85°C	3.22	3.3	3.58	UCC283TD−3	—	UCC283T−3	—
	4.875	5.00	5.125	UCC283TD−5	—	UCC283T−5	—
	ADJ			—	UCC283TD−ADJ	—	UCC283T−ADJ
0°C to 70°C	3.22	3.3	3.58	UCC383TD−3	—	UCC383T−3	—
	4.875	5.00	5.125	UCC383TD−5	—	UCC383T−5	—
	ADJ			—	UCC383TD−ADJ	—	UCC383T−ADJ

1. For more package and ordering information, see the Package Option Addendum located at the end of this data sheet.
2. For 50 piece reel, add KTTT (e.g., UCC283TDKTTT−3); for 500 piece reel, add TR (e.g., UCC283TDTR−3).

functional block diagram



electrical characteristics T_A = 0°C to 70°C for the UCC383−x series, T_A = −40°C to 85°C for the UCC283−x, $V_{VIN} = V_{VOUT}$ + 1.5 V, I_{OUT} = 10 mA, C_{IN} = 10 μF, C_{OUT} = 22 μF. For the UCC283−ADJ, V_{VIN} = 6.5 V, V_{OUT} = 5.0 V, C_T = 750 pF, $T_J = T_A$ unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283−5 Fixed 5 V, 3 A Family					
Output voltage	T_J = 25°C	4.925	5	5.075	V
	Over temperature	4.875		5.125	V
Line regulation	V_{VIN} = 5.15 V to 9 V		2	10	mV
Load regulation	I_{OUT} = 10 mA to 3 A		10	20	mV
Dropout voltage, $V_{DROPOUT} = V_{VIN} - V_{VOUT}$	I_{OUT} = 3 A, V_{OUT} = 4.85 V		0.4	0.6	V
	I_{OUT} = 1.5 A, V_{OUT} = 4.85 V		0.2	0.45	V
	I_{OUT} = 10 mA, V_{OUT} = 4.85 V		50	150	mV
Peak current limit	V_{VOUT} = 0 V	4	7	10	A
Overcurrent threshold		3	4	5.5	A
Current limit duty cycle	V_{VOUT} = 0 V		3%	5%	
Overcurrent time out, t_{ON}	V_{VOUT} = 0 V	400	750	1400	μs
Quiescent current	No load		400	650	μA
Reverse leakage current	1 V < V_{VIN} < V_{VOUT}, V_{VOUT} ≤ 5.1 V, at V_{VOUT}		30	75	μA
Undervoltage lockout	VIN where VOUT passes current	2.5	2.8	3	V
UCC283−3 Fixed 3.3 V, 3 A Family					
Output voltage	T_J = 25°C	3.25	3.3	3.35	V
	Over temperature	3.22		3.38	V
Line regulation voltage	V_{VIN} = 3.45 V to 9 V		2	7	mV
Load regulation voltage	I_{OUT} = 10 mA to 3 A		7	15	mV
Dropout voltage, $V_{DROPOUT} = V_{VIN} - V_{VOUT}$	I_{OUT} = 3A, VOUT = 3.15 V		0.5	1	V
	I_{OUT} = 1.5A, VOUT = 3.15 V		0.25	0.6	V
	I_{OUT} = 10mA, VOUT = 3.15 V		50	150	mV
Peak current limit	V_{VOUT} = 0 V	4	7	10	A
Overcurrent threshold		3	4	5.5	A
Current limit duty cycle	V_{VOUT} = 0 V		3%	5%	
Overcurrent time out, t_{ON}	V_{VOUT} = 0 V	400	750	1400	μs
Quiescent current	No load		400	650	μA
Reverse leakage current	1 V < V_{VIN} < V_{VOUT}, V_{VOUT} ≤ 3.35 V at V_{VOUT}		30	75	μA
Undervoltage lockout	VIN where VOUT passes current	2.5	2.8	3	V

electrical characteristics T_A = 0°C to 70°C for the UCC383−x series, T_A = −40°C to 85°C for the UCC283−x, $V_{VIN} = V_{VOUT}$ + 1.5 V, I_{OUT} = 10 mA, C_{IN} = 10 μF, C_{OUT} = 22 μF. For the UCC283−ADJ, V_{VIN} = 6.5 V, V_{OUT} = 5.0 V, C_T = 750 pF, $T_J = T_A$ unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UCC283−ADJ Adjustable Output, 3 A Family					
Regulating voltage at ADJ pin	TJ = 25°C	1.23	1.25	1.27	V
	Over temperature	1.22		1.28	V
Line regulation voltage, at ADJ input	$V_{VIN} = V_{VOUT}$ + 150 mV to 9 V		1	3	mV
Load regulation voltage, at ADJ input	I_{OUT} = 10 mA to 3 A		2	5	mV
Dropout voltage, $V_{DROPOUT}$ = VIN − VOUT	V_{OUT} = 4.85 V, I_{OUT} = 3 A		0.4	0.6	V
	V_{OUT} = 4.85 V, I_{OUT} = 1.5 A		0.2	0.45	V
	V_{OUT} = 4.85 V, I_{OUT} = 10 mA		50	150	mV
Peak current limit	V_{VOUT} = 0 V	4	7	10	A
Overcurrent threshold		3	4	5.5	A
Current limit duty cycle	V_{VOUT} = 0 V		3	5	%
Overcurrent time out, t_{ON}	V_{VOUT} = 0 V	300	575	1200	μs
Reverse leakage current	1 V < V_{VIN} < V_{VOUT} V_{VOUT} ≤ 9 V, at V_{VOUT}		30	100	μA
Bias current at ADJ input			20	250	nA
Quiescent current	No load		400	650	μA
Shutdown threshold	At CT input	0.25	0.65		V
Quiescent current in shutdown	V_{VIN} = 9 V		40	75	μA
UVLO	VIN where VOUT passes current	2.5	2.8	3	V

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage
- VIN . . . . 9 V
- CT . . . . −0.3 V to 3 V
- ADJ . . . . −0.3 V to 9 V

Storage Temperature, T_{stg} . . . . −65°C to 150°C
Junction Temperature, T_J . . . . −55°C to 150°C
Lead Temperature (soldering, 10 seconds) . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

pin descriptions

ADJ: Adjust pin for the UCC283−ADJ version only. Feedback pin for the linear regulator. Program the output voltage with R1 connected from ADJ to GND and R2 connected from VOUT to ADJ. Output voltage is given by:

$$V_{OUT} = \frac{1.25\ V \times (R1 + R2)}{R1}$$

CT: Short-circuit timing capacitor and shutdown input for the UCC283−ADJ version. Pulling CT below 0.25 V turns off the regulator and places it in a low quiescent-current mode. A timing capacitor, C, from CT to GND programs the duration of the pulsed short-circuit on-time. On-time, t_{ON}, is approximately given by:

$$t_{ON} = 750\ k \times C$$

GND: Reference ground.

VIN: Input voltage, This pin must be bypassed with a low ESL/ESR 1-µF or larger capacitor to GND. VIN can range from (VOUT + $V_{DROPOUT}$) to 9 V. If VIN is reduced to zero while VOUT is held high, the reverse leakage from VOUT to VIN is less than 75µA.

VOUT: Regulated output voltage. A bypass capacitor is not required at VOUT, but may be desired for good transient response. The bypass capacitor must not exceed a maximum value in order to insure the regulator can start.

APPLICATION INFORMATION

overview

The UCC383 family of low dropout linear (LDO) regulators provide a regulated output voltage for applications with up to 3 A of load current. The regulators feature a low dropout voltage and short-circuit protection, making their use ideal for demanding high-current applications requiring fault protection.

short-circuit-protection

The UCC383 provides unique short-circuit protection circuitry that reduces power dissipation during a fault. When an overload situation is detected, the device enters a pulsed mode of operation at 3% duty cycle reducing the heat sink requirements during a fault. The UCC383 has two current thresholds that determine its behavior during a fault as shown in Figure 1. When the regulator current exceeds the **overcurrent threshold** for a period longer than t_{ON}, the UCC383 shuts off for a period (t_{OFF}) which is $32 \times t_{ON}$. During an overload, the regulator actively limits the maximum current to the **peak current limit** value. The peak current limit is nominally 3 A greater than the overcurrent threshold. The regulator continues in pulsed mode until the fault is cleared as illustrated in Figure 1.

APPLICATION INFORMATION

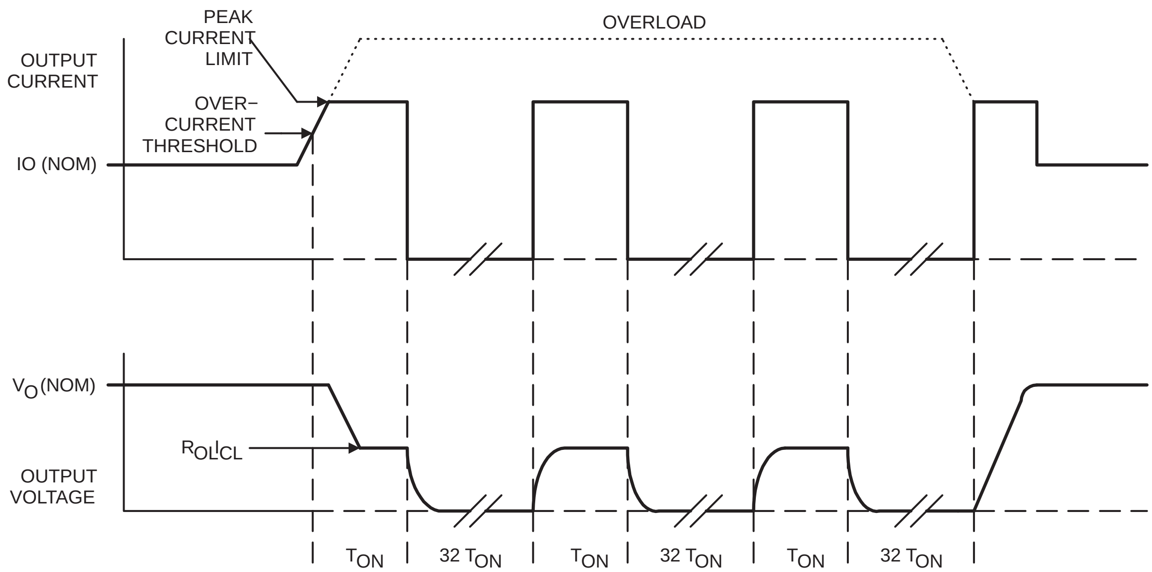


Figure 1. UCC383 Short-Circuit Timing

A capacitive load on the regulator's output appears as a short-circuit during start-up. If the capacitance is too large, the output voltage does not come into regulation during the initial t_{ON} period and the UCC383 enters pulsed mode operation. The peak current limit, t_{ON} period, and load characteristics determine the maximum value of output capacitor that can be charged. For a constant current load the maximum output capacitance is given as follows:

$$C_{OUT(max)} = \left(I_{CL} - I_{LOAD}\right) \times \frac{t_{ON}}{V_{OUT}} \quad \text{Farads} \tag{1}$$

For worst case calculations, the minimum values of on time (t_{ON}) and peak current limit (I_{CL}) should be used. The adjustable version allows the t_{ON} time to be adjusted with a capacitor on the CT pin:

$$t_{ON(adj)} = 750,000 \times C\ (\mu\ \text{Farad})\ \text{microseconds} \tag{2}$$

For a resistive load (R_{LOAD}) the maximum output capacitor can be estimated from:

$$C_{OUT(max)} = \frac{t_{ON(sec)}}{R_{LOAD} \times \ell n \left[\dfrac{1}{1 - \dfrac{VOUT}{I_{CL} \times R_{LOAD}}} \right]} \ \text{Farads} \tag{3}$$

APPLICATION INFORMATION

dropout performance

Referring to the *Block Diagram*, the dropout voltage of the UCC383 is equal to the minimum voltage drop (V_{IN} to V_{OUT}) across the N-channel MOSFET. The dropout voltage is dependent on operating conditions such as load current, input and load voltages, as well as temperature. The UCC383 achieves a low Rds(on) through the use of an internal charge-pump (V_{PUMP}) that drives the MOSFET gate. Figure 2 depicts typical dropout voltages versus load current for the 3.3-V and 5-V versions of the part, as well as the adjustable version programmed to 3.0 V.

Figure 3 depicts the typical dropout performance of the adjustable version with various output voltages and load currents.

Operating temperatures also affect the Rds(on) and dropout voltage of the UCC383. Figure 4 graphs the typical dropout for the 3.3-V and 5-V versions with a 3-A load over temperature.

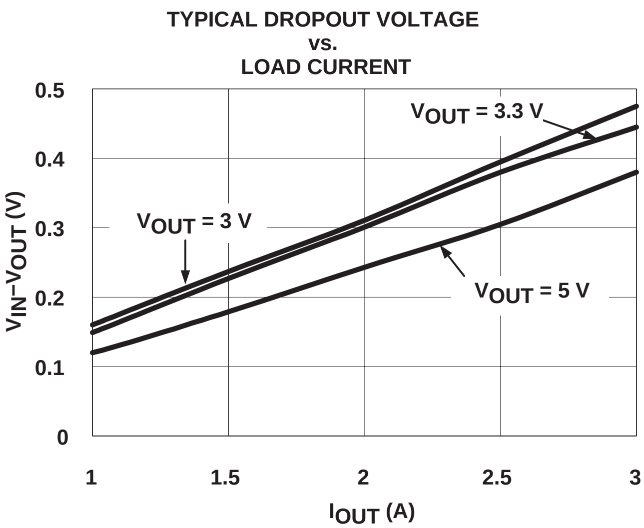


Figure 2

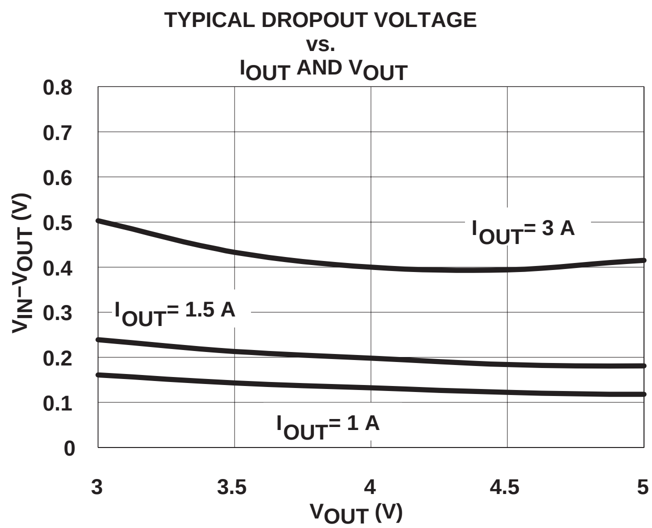


Figure 3

APPLICATION INFORMATION

voltage programming and shutdown feature for adjustable version

A typical application circuit based on the UCC383 adjustable version is shown in Figure 5. The output voltage is externally programmed through a resistive divider at the ADJ pin.

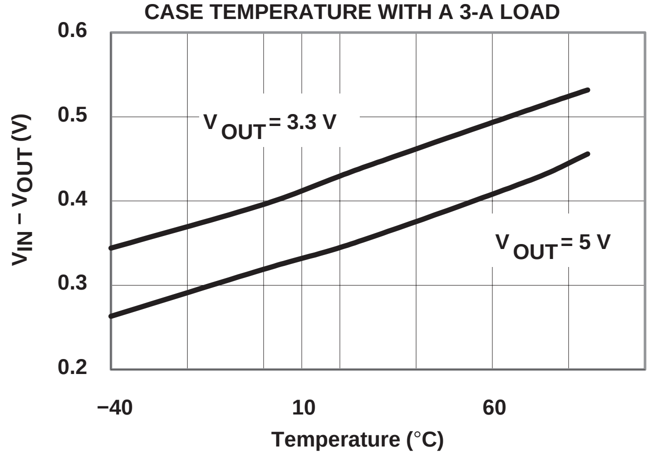


Figure 4

$$V_{OUT} = 1.25 \times \left(1 + \frac{R2}{R1}\right) \text{ Volts} \tag{4}$$

The maximum programmed output voltage is constrained by the 9-V absolute rating of the IC (this includes the charge pump voltage) and its ability to enhance the N-channel MOSFET. Unless the load current is below the 3-A rating of the device, output voltages above 7 V are not recommended. The minimum output voltage can be programmed down to 1.25 V. However, the input voltage must always be greater than the UVLO of the part.

The adjustable version includes a shutdown feature, limiting quiescent current to 40 µA typical. The UCC383 is shut down by pulling the CT pin to below 0.25 V. As shown in Figure 5, a small logic level MOSFET or BJT transistor in parallel with the timing capacitor can be driven with a digital signal, putting the device in shutdown. If the CT pin is not pulled low, the IC internally pulls up the pin enabling the regulator. The CT pin should not be forced high, as this interferes with the short-circuit-protection feature. Selection of the timing capacitor is explained in *Short-Circuit-Protection*.

The adjustable version can be used in applications requiring remote voltage sensing (i.e. monitoring a voltage other than or not directly tied to the VOUT pin). This is possible since the inverting input of the error-voltage amplifier (see *Block Diagram*) is brought out to the ADJ pin.

APPLICATION INFORMATION

thermal design

The *Package Information* section of the *Power Supply Control Products Data Book, Volume 3* (Literature No. SLUD003) contains reference material for the thermal ratings of various packages. The section also includes an excellent article *Thermal Characteristics of Surface Mount Packages*, that is the basis of the following discussion.

Thermal design for the UCC383 family of linear regulators includes two modes of operation, normal and pulsed mode. In normal operation, the linear regulator and heat sink must dissipate power equal to the maximum forward voltage drop multiplied by the maximum load current. Assuming a constant current load, the expected heat rise at the regulator's junction can be calculated as follows:

$$t_{RISE}(\theta) = P_{DISS} \times \left(\theta_{jc} + \theta_{ca}\right) \quad °C \tag{5}$$

Where theta, (θ) is thermal resistance and P_{DISS} is the power dissipated. The thermal resistance of both the TO−220 and TO−263 packages (junction to case) is 3°C per Watt. In order to prevent the regulator from going into thermal shutdown, the case to ambient theta must keep the junction temperature below 150°C. If the LDO is mounted on a 5-square inch pad of 1-ounce copper, for example, the thermal resistance from junction to ambient becomes 60°C per Watt. If a lower thermal resistance is required by the application, the device heat sinking would need to be improved.

When the UCC383 regulator is in pulsed mode due to an overload or short-circuit in the application, the maximum average power dissipation is calculated as follows:

$$P_{PULSE(avg)} = \left(V_{IN} - V_{OUT}\right) \times I_{CL} \times \frac{t_{ON}}{33 \times t_{ON}} \text{ Watts} \tag{6}$$

As seen in Equation 6, the average power during a fault is reduced dramatically by the duty cycle, allowing the heat sink to be sized for normal operation. Although the peak power in the regulator during the t_{ON} period can be significant, the thermal mass of the package generally keeps the junction temperature from rising unless the t_{ON} period is increased to tens of milliseconds.

ripple rejection

Even though the UCC383 family of linear regulators are not optimized for fast transient applications (Refer to the UC182 Fast LDO Linear Regulator), they do offer significant power supply rejection at lower frequencies. Figure 6 depicts ripple rejection performance in a typical application. The performance can be improved with additional filtering.

APPLICATION INFORMATION

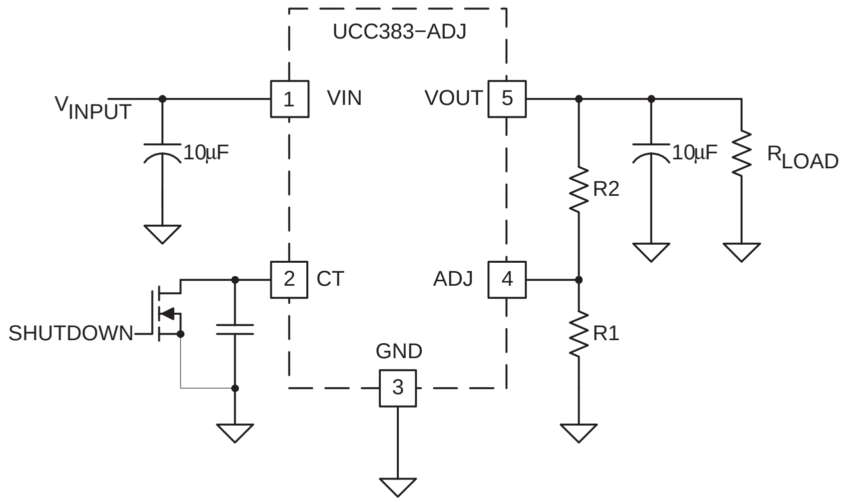


Figure 5. Typical Application for 5-Pin Adjustable Version

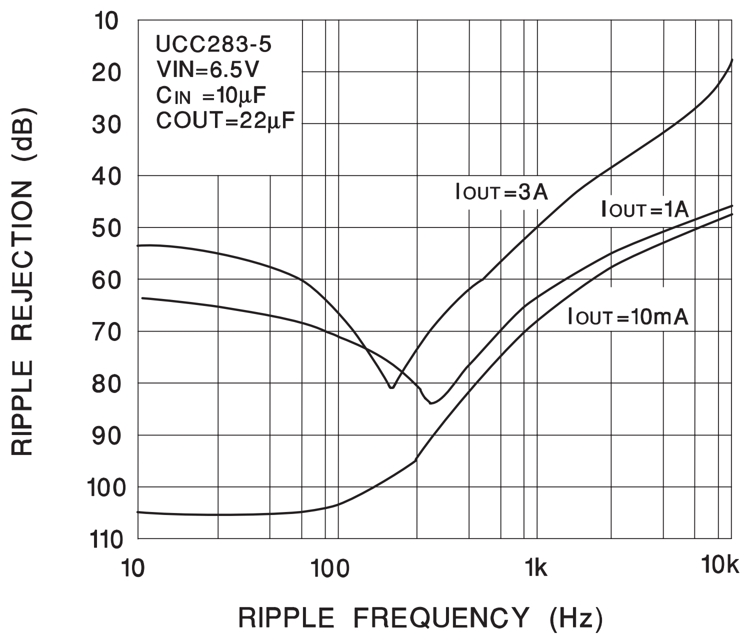


Figure 6. Ripple Rejection vs. Frequency

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC283T-3	ACTIVE	TO-220	KC	3	50	None	CU SN	Level-NA-NA-NA
UCC283T-5	ACTIVE	TO-220	KC	3	50	None	CU SN	Level-NA-NA-NA
UCC283T-ADJ	ACTIVE	TO-220	KC	5	50	None	CU SN	Level-NA-NA-NA
UCC283TD-ADJ	OBSOLETE	DDPAK/ TO-263	KTT	5		None	Call TI	Call TI
UCC283TDKTTT-3	ACTIVE	DDPAK/ TO-263	KTT	3	50	None	CU SN	Level-2-220C-1 YEAR
UCC283TDKTTT-5	ACTIVE	DDPAK/ TO-263	KTT	3	50	None	CU SN	Level-2-220C-1 YEAR
UCC283TDKTTT-ADJ	ACTIVE	DDPAK/ TO-263	KTT	5	50	None	CU SN	Level-2-220C-1 YEAR
UCC283TDTR-3	ACTIVE	DDPAK/ TO-263	KTT	3	500	None	CU SN	Level-2-220C-1 YEAR
UCC283TDTR-5	ACTIVE	DDPAK/ TO-263	KTT	3	500	None	CU SN	Level-2-220C-1 YEAR
UCC283TDTR-ADJ	ACTIVE	DDPAK/ TO-263	KTT	5	500	None	CU SN	Level-2-220C-1 YEAR
UCC383T-3	ACTIVE	TO-220	KC	3	50	None	CU SN	Level-NA-NA-NA
UCC383T-5	ACTIVE	TO-220	KC	3	50	None	CU SN	Level-NA-NA-NA
UCC383T-ADJ	ACTIVE	TO-220	KC	5	50	None	CU SN	Level-NA-NA-NA
UCC383TD-3	OBSOLETE	DDPAK/ TO-263	KTT	3		None	Call TI	Call TI
UCC383TD-5	OBSOLETE	DDPAK/ TO-263	KTT	3		None	Call TI	Call TI
UCC383TD-ADJ	OBSOLETE	DDPAK/ TO-263	KTT	5		None	Call TI	Call TI
UCC383TDKTTT-3	ACTIVE	DDPAK/ TO-263	KTT	3	50	None	CU SN	Level-2-220C-1 YEAR
UCC383TDKTTT-5	ACTIVE	DDPAK/ TO-263	KTT	3	50	None	CU SN	Level-2-220C-1 YEAR
UCC383TDKTTT-ADJ	ACTIVE	DDPAK/ TO-263	KTT	5	50	None	CU SN	Level-2-220C-1 YEAR
UCC383TDTR-3	ACTIVE	DDPAK/ TO-263	KTT	3	500	None	CU SN	Level-2-220C-1 YEAR
UCC383TDTR-5	ACTIVE	DDPAK/ TO-263	KTT	3	500	None	CU SN	Level-2-220C-1 YEAR
UCC383TDTR-ADJ	ACTIVE	DDPAK/ TO-263	KTT	5	500	None	CU SN	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).

PACKAGE OPTION ADDENDUM

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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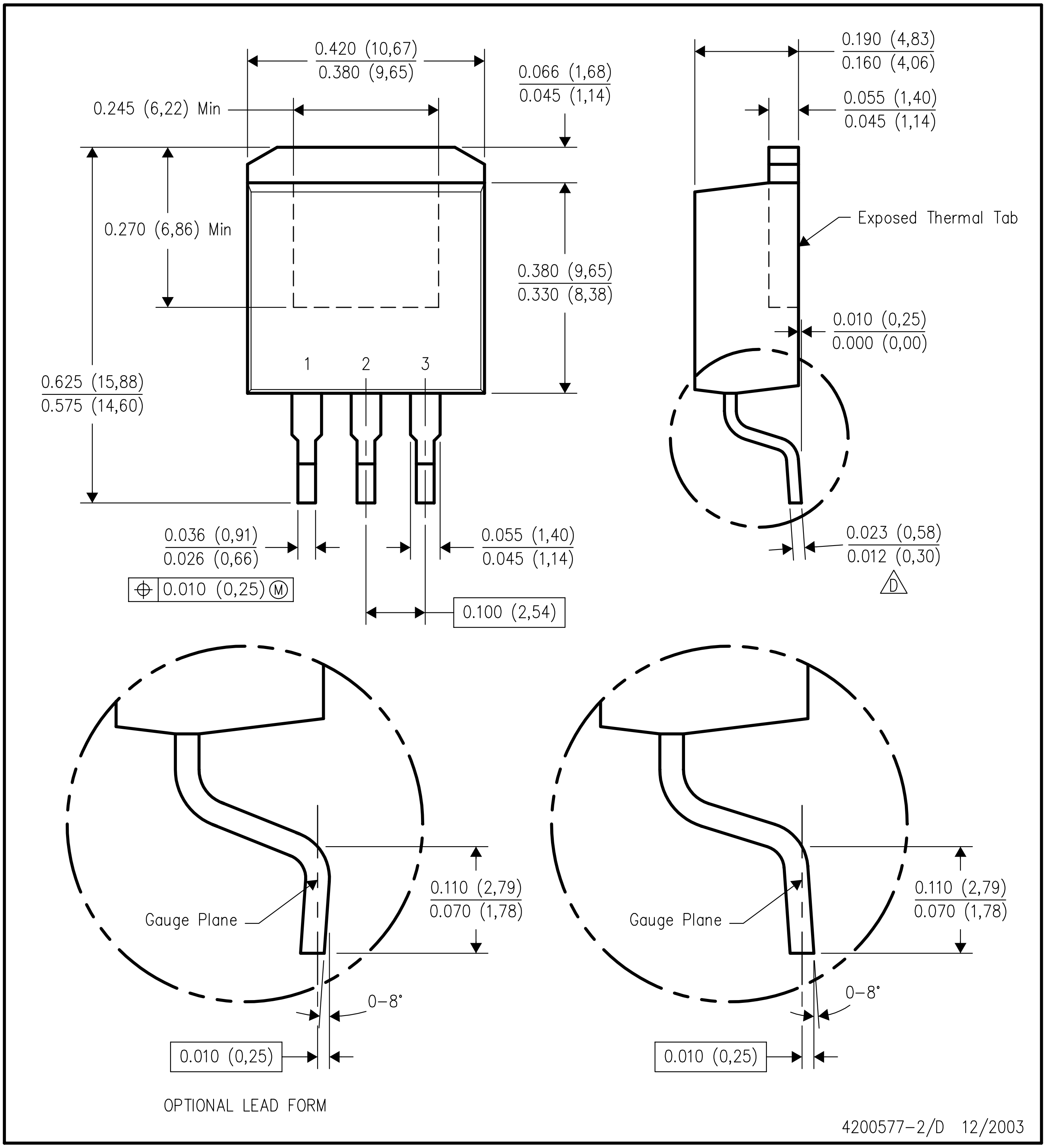
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



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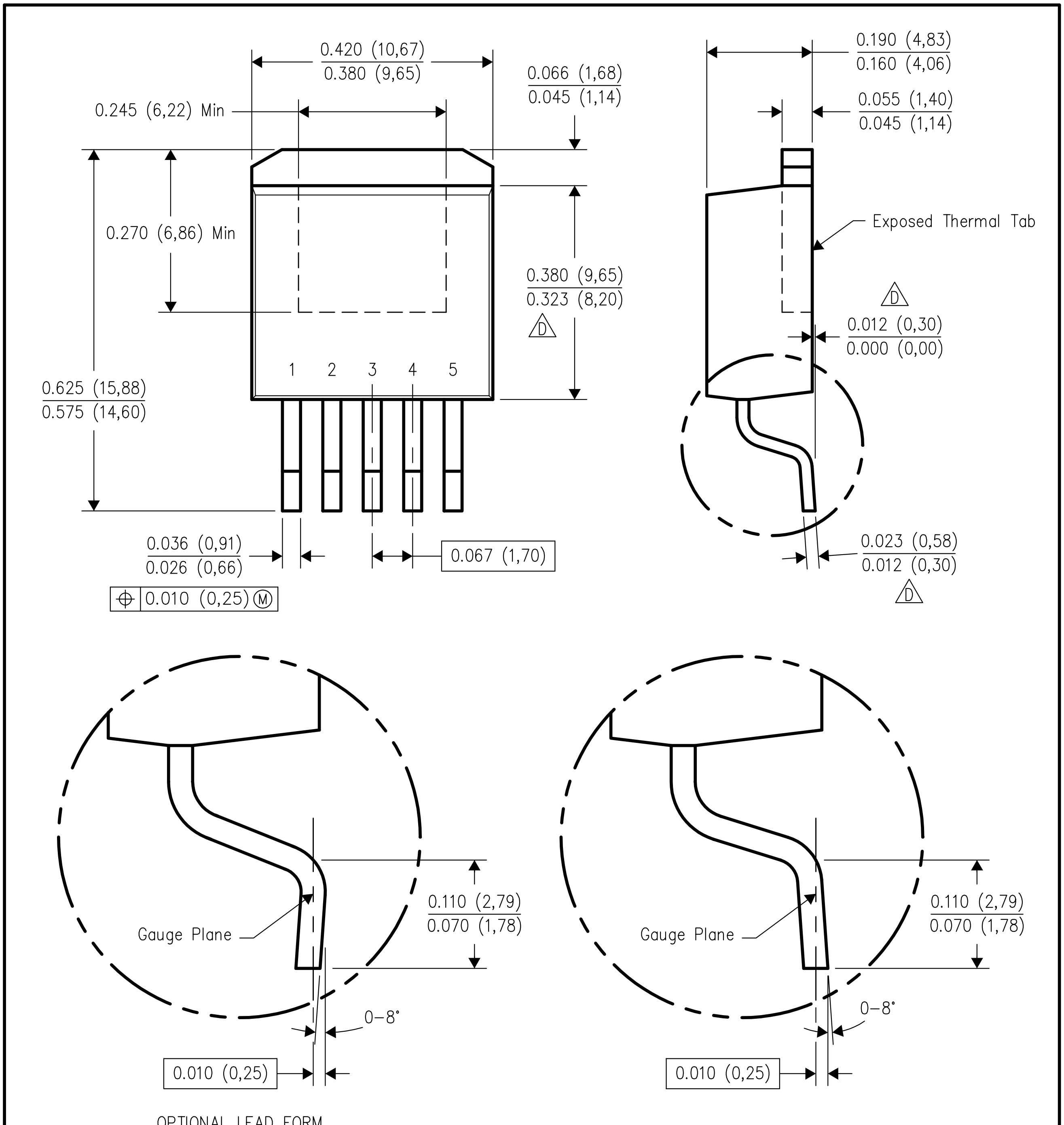
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness.

KTT (R–PSFM–G5) PLASTIC FLANGE–MOUNT PACKAGE



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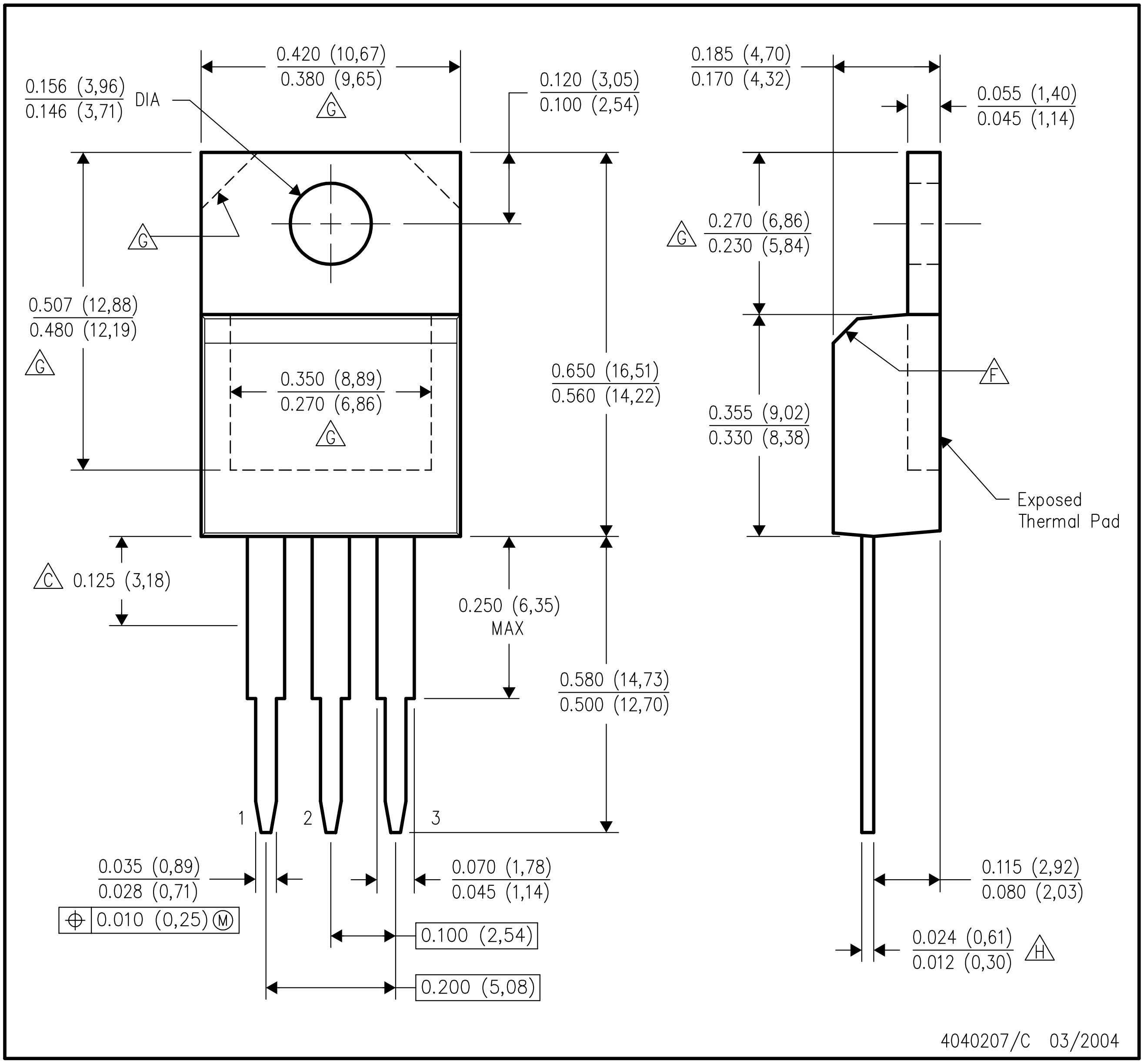
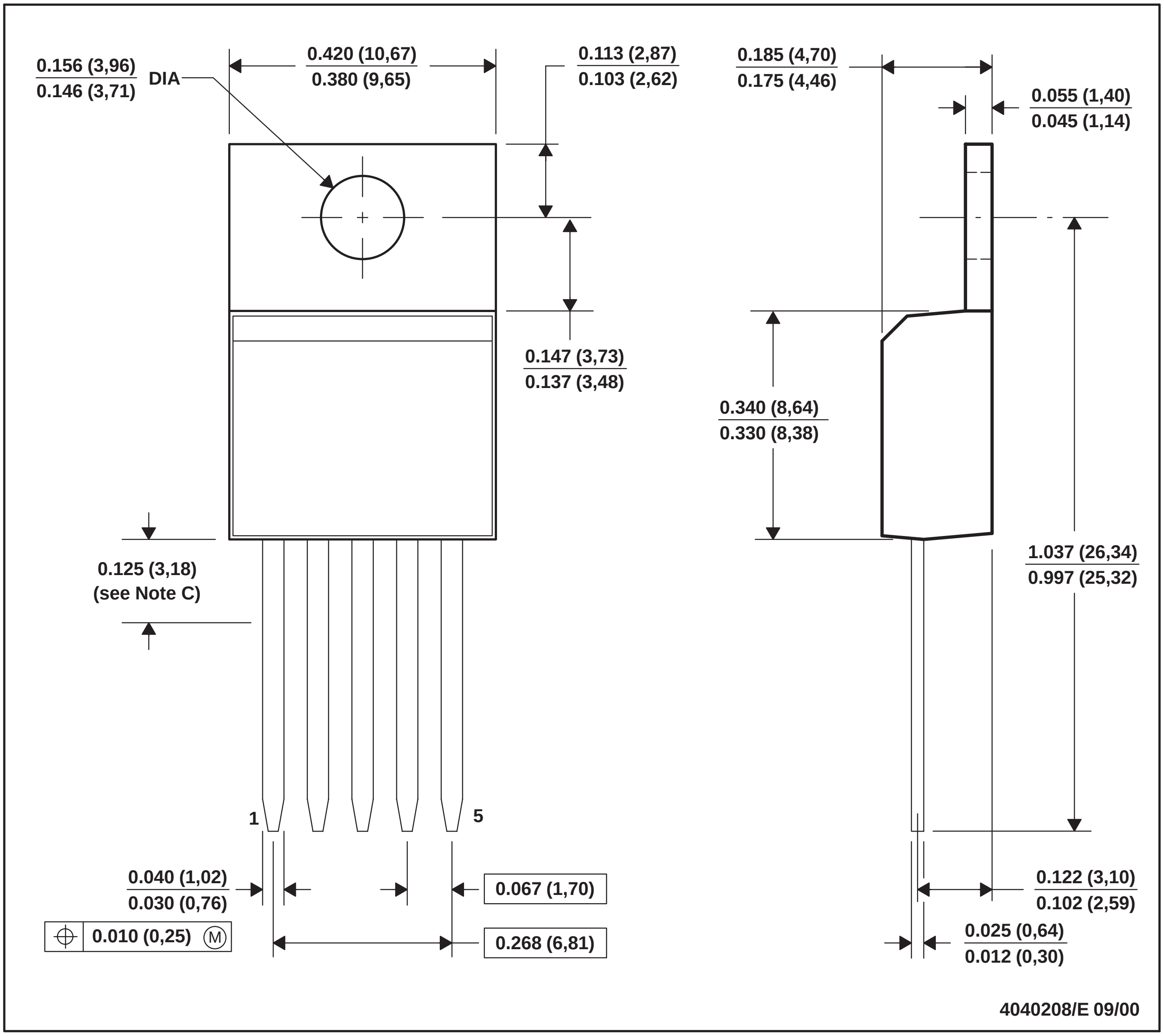
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
D. Falls within JEDEC TO–263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

KC (R-PSFM-T5) **PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

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