# ❑ MN101D06F , MN101D06G , MN101D06H

| Type | MN101D06F | MN101D06G | MN101D06H |
|---|---|---|---|
| ROM (×8-bit) | 96 K | 128 K | 160 K |
| RAM (×8-bit) | 3 K | 4 K | 5 K |
| Package | QFP100-P-1818B *Lead-free | | |
| Minimum Instruction Execution Time | With main clock operated: 0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)<br>71.5 µs (at 3.0 V to 5.5 V fixed to 14.32 MHz internal frequency division)<br>When sub-clock operated: 61 µs (at 2.2 V to 5.5 V, 32.768 kHz) | | |
| Interrupts | • RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4 • key input (P50 to 54)<br>• Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 4 • Timer 6 • Capstan FG • Control • HSW<br>• Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0 • Serial 1 • Serial 2<br>• A/D (common with PWM 4 reference frequency) • OSD V-sync | | |

**Timer Counter**

Timer counter 0: 16-bit × 1
(timer function, clock function [max. 2 s or max. 36 h at cascade-connecting with timer 6])
- Clock source ····· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; overflow of timer counter 6; 1/512 of XI oscillation clock or OSC oscillation clock frequency
- Interrupt source ····· overflow of timer counter 0

Timer counter 1: 16-bit × 1 (timer function, linear timer counter function)
- Clock source ····· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; CTL signal
- Interrupt source ····· overflow of timer counter 1

Timer counter 2: 16-bit × 1 (timer function, input capture, duty judgment of CTL signal(VISS/VASS detection function))
- Clock source ····· 1/2, (1/4,) 1/8, (1/16,) 1/12, (1/24) of system clock frequency
- Interrupt source ····· overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register

Timer counter 3: 16-bit × 1
(timer function, detection of serial indexing, generation of remote control output carrier frequency)
- Clock source ····· 1/2, (1/4,) 1/8, (1/16) of system clock frequency; XI oscillation clock
- Interrupt source ····· overflow of timer counter 3

Timer counter 4: 16-bit × 1 (timer function, event count [P15 input], generation of serial transmission clock)
- Clock source ····· 1/8, (1/16) of system clock frequency; external clock input
- Interrupt source ····· overflow of timer counter 4; coincidence of timer counter 4 with OCR4

Timer counter 5: 19-bit × 1 (watchdog, stable oscillation waiting function)
- Clock source ····· system clock
- Watchdog interrupt source ·· $1/2^{16}$, $1/2^{19}$ of timer counter 5 frequency
- Clear by stable oscillation ·· after 256 counts by timer counter 5 ($2^{18}$ counts of OSC oscillation clock)

Timer counter 6: 16-bit × 1 (clock function [max. 2 s])
- Clock source ····· 1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/4, (1/8,) 1/64, (1/128) of system clock frequency
- Interrupt source ····· $1/2^{13}$, $1/2^{14}$, $1/2^{15}$ overflow of timer counter 6

Timer counter 7: 8-bit × 1 or 4-bit × 2 (timer function, event count)
- Clock source ····· 1/4, (1/8,) 1/16, (1/32) of system clock frequency; external clock input
- Interrupt source ····· overflow of timer counter 7 (although when 4-bit × 2, there is one interrupt vector. )

**Serial Interface**

Serial 0: 8-bit × 1 (synchronous type/start-stop synchronous type) (transfer direction of MSB/LSB selectable)
- Synchronous type clock source 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT0 pin input
- Clock for UART ····· 8-division of above clock; 2-division timer 4 output; NSBT0 pin input

## Serial Interface (Continue)

Serial 1: 8-bit × 1
(synchronous type/remote control transmission/simple remote control receive) (transfer direction of MSB/LSB selectable, start condition function)

Clock source ····· 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 4 output; NSBT1 pin input

Remote control clock ····· 2-division timer 4 output

Serial 2: 8-bit × 1 ($I^2C$) (master transmission/reception, slave transmission/reception)

Clock source ····· 1/144 to 1/252 of system clock; SCK pin input

## OSD

OSD mode: Accommodation with menu(internal synchronous) or super impose(external synchronous) display

Applicable broadcasting system:NTSC, PAL, PAL-M, PAL-N

| | |
|---|---|
| Screen configuration | : 24 characters × 2n rows (n = 1 to 6) |
| Character type | : max. 512 character types (variable, incude special characters) |
| Character size | : 12 × 18 dots (Vertical direction: 1 dot for 2H at not enlargement) |
| Enlarged characters | : each × 2, × 3 or × 4 settings in horizontal and vertical |
| Character interpolation | : none |
| Line background color | : 8-hue settable (settable in the row unit at menu display) |
| Line background intensity | : 8 gradations settable in the row unit (at output of composite video signal) |
| Screen background color | : 8-hue settable (at output of composite video signal) |
| Character color | : white (at output of composite video signal) |
| Character intensity | : 8 gradations settable in the row unit (at output of composite video signal) |
| Frame function | : 1-dot frame in 4 or 8 directions |
| Frame intensity | : 4 gradations settable in the row unit (at output of composite video signal) |
| Box shade function | : settable in the character unit (at output of composite video signal with 129 or more characters (character types)) |
| Blinking | : none (covered by software) |
| Inverted character | : settable in the character unit |
| Halftone | : settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal) |

CCD mode: Supports Closed Caption in the U.S.A.

| | |
|---|---|
| Screen configuration | : 32 characters × 16 rows |
| Character type | : max. 128 character types (variable) |
| Character size | : 12 × 26 dots (Vertical direction: 1 dot for 1H, including 8 dots in the underlined area) |
| Enlarged characters | : none |
| Character interpolation | : none |
| Line background color | : 8-hue settable |
| Line background intensity | : 8 gradations settable in the screen unit (at output of composite video signal) |
| Screen background color | : 8-hue settable (at output of composite video signal) |
| Character color | : 8 colors (at RGB output)<br>: White (at output of composite video signal) |
| Character intensity | : 8 gradations settable in the screen unit (at output of composite video signal) |
| Frame function | : none |
| Box shade function | : none |
| Inverted character | : none |
| Halftone | : settable in the row unit in 2 intensity gradations (at output of external synchronous composite video signal) |
| Others | : Underline, italic, blinking function and scroll |
| Input | : composite video signal input (output level: 1 V[p-p] / 2 V[p-p]) |
| Clamp method | : sync tip clamp, clamp level in 4 levels |
| Output | : composite video output<br>: digital output (6 pins) |
| Measure against image fluctuation | : built-in AFC circuit |
| Dot clock | : 1/2 of OSC oscillation clock (automatic phase adjustment) |

**See the next page for electrical characteristics, pin assignment and support tool.**

| | | | |
|---|---|---|---|
| **XDS** | | Built-in U.S. closed caption data slicer (optional 2 line data can be extracted.) | |
| **ROM Correction** | | Correcting address designation: up to 3 addresses possible<br>Correction method: correction program being saved in internal RAM | |
| **I/O Pins** | **I/O** | 75 | • Common use: 66 |
| | **Input** | 2 | • Common use: 2 |
| **A/D Inputs** | | 8-bit × 13-ch. (without S/H) | |
| **PWM** | | 13-bit × 2-ch. (at repetition cycle 572 µs at 14.32 MHz),<br>10-bit × 2-ch. (at repetition cycle 71.5 µs at 14.32 MHz),<br>8-bit × 1-ch. (at repetition cycle 71.5 µs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz) | |
| **ICR** | | 18-bit × 6-ch. | |
| **OCR** | | 16-bit × 2 (8-bit synchronous output; 4-bit 3-state synchronous output),<br>16-bit × 1 (weak electric field V-sync backup), 16-bit × 1 (Rec CTL) | |
| **Special Ports** | | Buzzer output; 3-state output VLP pin; remote control receive;<br>CTL signal input terminal; Capstan FG inputterminal; Sylinder(Durm) PG/FG input terminals;<br>HSW output terminal; Head Amp/Rortary control output terminals;<br>output of 1/2 OSC oscillation clock (2 V[p-p]); output of 1/4 OSC oscillation clock (1 V[p-p]) | |

## Electrical Characteristics

### Supply current

| Parameter | Symbol | Condition | Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Operating supply current | IDD1 | 14.32 MHz operation without load, VDD = 5 V | | 60 | 100 | mA |
| | IDD2 | 1/1024 of 14.32 MHz operation without load, VDD = 3.0 V | | 2 | 5 | mA |
| | IDD3 | Stop of 14.32 MHz oscillation, VDD = 2.7 V<br>32 kHz oscillation operation without load | | 50 | 100 | µA |
| Supply current at STOP | IDSP | Stop of oscillation without load, VDD = 5 V, Ta = 55 °C | | | 10 | µA |
| Supply current at HALT | IDHT0 | 14.32 MHz oscillation without load, VDD = 5 V | | 5 | 15 | mA |
| | IDHT1 | Stop of 14.32 MHz oscillation, VDD = 2.7 V<br>32 kHz oscillation operation without load | | 5 | 20 | µA |

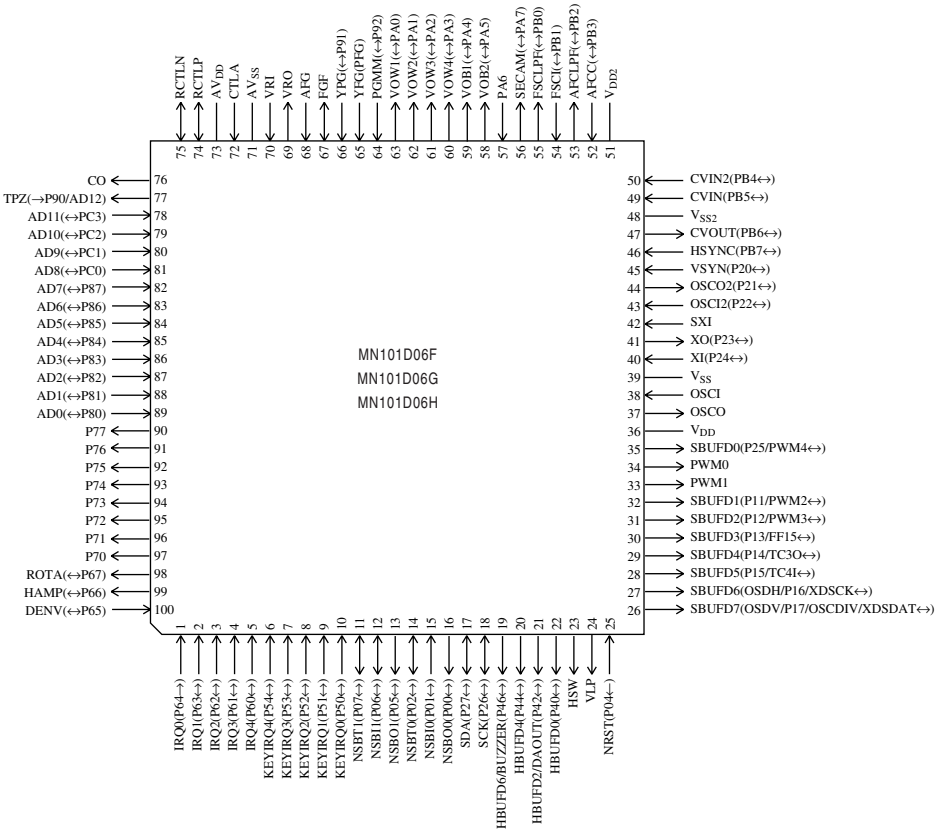
(Ta = 25 °C ± 2 °C , VSS = 0 V)

### A/D Converter Performance

| Parameter | Symbol | Condition | Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Conversion relative error | ΔNLAD | | | | ± 3 | LSB |
| A/D Conversion Time | tAD | fosc = 14.32 MHz | | 8 | | µs |
| Analog Input Voltage | | | | | 5 | V |

(Ta = 25 °C ± 2 °C , VDD = 5.0 V , VSS = 0 V)

## Pin Assignment




QFP100-P-1818B *Lead-free

## Support Tool

| | | |
|---|---|---|
| **In-circuit Emulator** | PX-ICE101C / D + PX-PRB101D06-QFP100-P-1818B-M | |
| **Flash Memory Built-in Type** | Type | MN101DF06ZAF |
| | ROM (× 8-bit) | 224 K |
| | RAM (× 8-bit) | 6 K |
| | Minimum instruction execution time | 0.1397 µs (at 4.0 V to 5.5 V, 14.32 MHz)<br>71.5 µs (at 3.0 V to 5.5 V, fixed to 14.32 MHz internal division)<br>61 µs (at 2.5 V to 5.5 V, 32.768 kHz) |
| | Package | QFP100-P-1818B *Lead-free |

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