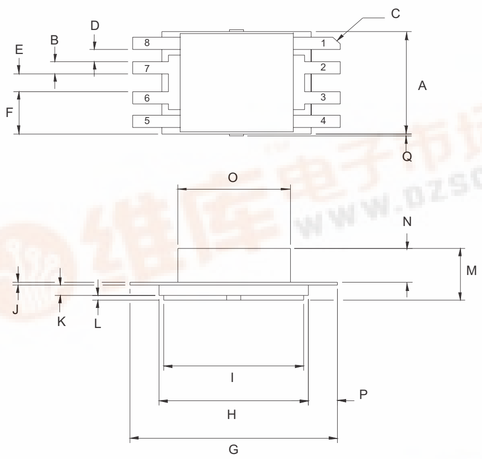
SEME LAB

TetraFET

D1213UK

METAL GATE RF SILICON FET

MECHANICAL DATA



DBC1 Package

PIN 1 Source	PIN 5 Source
PIN 2 Drain	PIN 6 Gate
PIN 3 Drain	PIN 7 Gate
PIN 4 Source	PIN 8 Source

DIM	mm	Tol.	Inches	Tol.
A	6.47	0.08	.255	.003
B	0.76	0.08	.030	.003
C	45°	5°	45°	5°
D	0.76	0.08	.030	.003
E	1.14	0.08	.045	.003
F	2.67	0.08	.105	.003
G	11.73	0.13	.462	.005
H	8.43	0.08	.332	.003
I	7.92	0.08	.312	.003
J	0.20	0.02	.008	.001
K	0.64	0.02	.025	.001
L	0.30	0.02	.012	.001
M	3.25	0.08	.128	.003
N	2.11	0.08	.083	.003
O	6.35SQ	0.08	.250SQ	.003
P	1.65	0.51	.065	.020
Q	0.13	max	.005	max

GOLD METALLISED MULTI-PURPOSE SILICON DMOS RF FET 6W – 7.2V – 500MHz SINGLE ENDED

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- LOW NOISE
- HIGH GAIN – 10 dB MINIMUM

APPLICATIONS

- HF/VHF/UHF COMMUNICATIONS from 1 MHz to 1 GHz

ABSOLUTE MAXIMUM RATINGS (T_{case} = 25°C unless otherwise stated)

P_D	Power Dissipation	58W
BV_{DSS}	Drain – Source Breakdown Voltage	40V
BV_{GSS}	Gate – Source Breakdown Voltage	±20V
$I_{D(sat)}$	Drain Current	20A
T_{stg}	Storage Temperature	–65 to 150°C
T_j	Maximum Operating Junction Temperature	200°C

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ELECTRICAL CHARACTERISTICS (T_{case} = 25°C unless otherwise stated)

Parameter		Test Conditions			Min.	Typ.	Max.	Unit
BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0$	$I_D = 100mA$		40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 12.5V$	$V_{GS} = 0$				1	mA
I_{GSS}	Gate Leakage Current	$V_{GS} = 20V$	$V_{DS} = 0$				1	μA
$V_{GS(th)}$	Gate Threshold Voltage*	$I_D = 10mA$	$V_{DS} = V_{GS}$		0.5		7	V
g_{fs}	Forward Transconductance*	$V_{DS} = 10V$	$I_D = 2A$		1.6			S
G_{PS}	Common Source Power Gain	$P_O = 6W$			10			dB
η	Drain Efficiency	$V_{DS} = 7.2V$	$I_{DQ} = 0.5A$		50			%
VSWR	Load Mismatch Tolerance	f = 500MHz			20:1			—
C_{iss}	Input Capacitance	$V_{DS} = 0$	$V_{GS} = –5V$	f = 1MHz			120	pF
C_{oss}	Output Capacitance	$V_{DS} = 12.5V$	$V_{GS} = 0$	f = 1MHz			80	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 12.5V$	$V_{GS} = 0$	f = 1MHz			8	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle ≤ 2%

THERMAL DATA

$R_{THj–case}$	Thermal Resistance Junction – Case	Max. 3°C / W

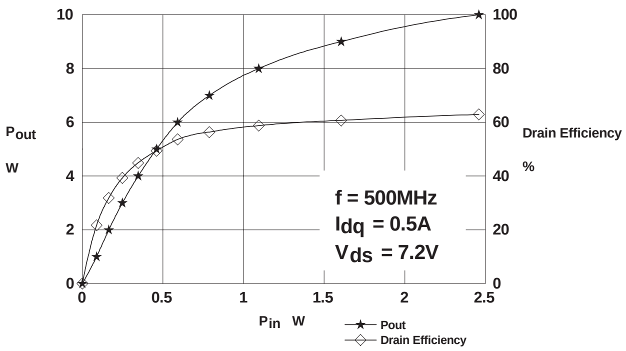

Figure 1 – Power Output and Efficiency vs. Power Input.

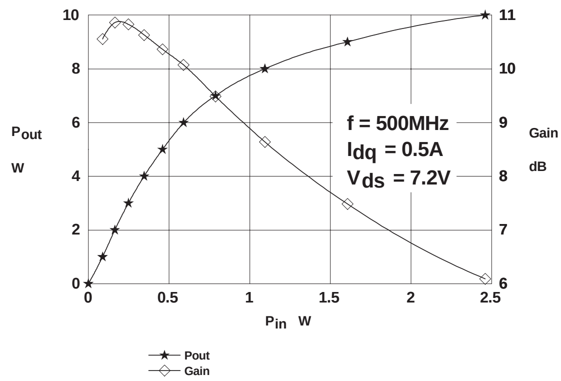

Figure 2 – Power Output & Gain vs. Power Input.

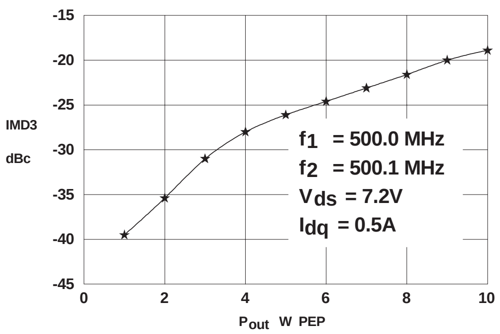

Figure 3 – IMD vs. Output Power.

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OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
500	2.3 - j0.4	2.1 - j1.9

Typical S Parameters

! V_{DS} = 7.2V I_{DQ} = 0.2A

MHZ S MA R 50

!Freq	S11		S21		S12		S22	
MHz	mag	ang	mag	ang	mag	ang	mag	ang
70	0.69	-147	6.8	68	0.021	-1	0.77	-160
100	0.74	-153	4.5	59	0.017	10	0.79	-163
150	0.82	-161	2.5	47	0.015	50	0.84	-167
200	0.86	-167	1.6	42	0.024	78	0.87	-169
250	0.89	-172	1.2	35	0.037	83	0.89	-171
300	0.90	-176	1.0	33	0.052	87	0.90	-173
350	0.91	-179	0.7	27	0.064	82	0.91	-175
400	0.92	178	0.6	26	0.082	82	0.92	-177
450	0.93	174	0.5	23	0.095	80	0.93	-178
500	0.93	171	0.5	21	0.116	77	0.93	-179
550	0.93	168	0.4	20	0.130	73	0.94	180
600	0.93	164	0.4	15	0.148	66	0.94	178
650	0.93	162	0.3	18	0.159	66	0.95	177
700	0.92	158	0.3	16	0.173	60	0.94	177
750	0.92	155	0.3	21	0.182	58	0.95	176
800	0.91	153	0.3	23	0.189	56	0.96	175
850	0.92	151	0.3	29	0.207	59	0.96	173
900	0.94	148	0.3	29	0.235	59	0.95	171
950	0.95	144	0.3	31	0.275	56	0.93	170
1000	0.93	140	0.4	29	0.308	52	0.92	168