Low Cost, Low Power CMOS General-Purpose Dual Analog Front End

AD73322L

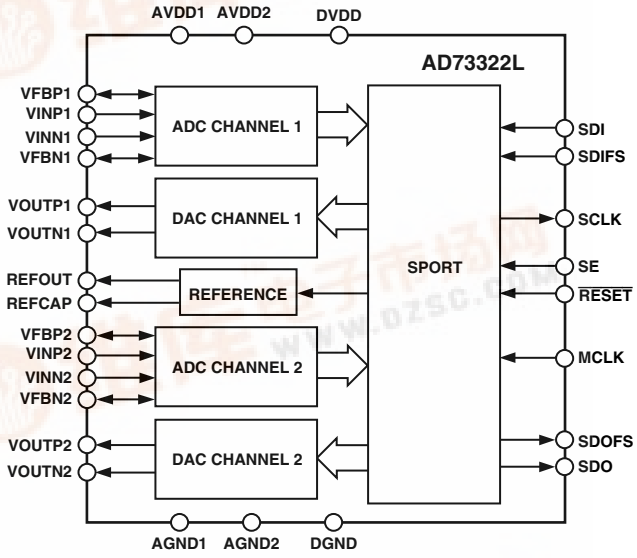
FEATURES

Two 16-Bit A/D Converters
Two 16-Bit D/A Converters
Programmable Input/Output Sample Rates
78 dB ADC SNR
78 dB DAC SNR
64 kS/s Maximum Sample Rate
–90 dB Crosstalk
Low Group Delay (25 μs Typ per ADC Channel, 50 μs Typ per DAC Channel)
Programmable Input/Output Gain
Flexible Serial Port which Allows Up to Four Dual Codecs to be Connected in Cascade Giving Eight I/O Channels
Single (2.7 V to 3.3 V) Supply Operation
50 mW Typ Power Consumption at 3.0 V
Temperature Range: –40°C to +105°C
On-Chip Reference
28-Lead SOIC, TSSOP, and 44-Lead LQFP Packages

APPLICATIONS

General-Purpose Analog I/O
Speech Processing
Cordless and Personal Communications
Telephony
Active Control of Sound and Vibration
Data Communications
Wireless Local Loop

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD73322L is a dual front-end processor for general purpose applications including speech and telephony. It features two 16-bit A/D conversion channels and two 16-bit D/A conversion channels. Each channel provides 78 dB signal-to-noise ratio over a voiceband signal bandwidth. It also features an input-to-output gain network in both the analog and digital domains. This is featured on both codecs and can be used for impedance matching or scaling when interfacing to Subscriber Line Interface Circuits (SLICs).

The AD73322L is particularly suitable for a variety of applications in the speech and telephony area, including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multichannel active control applications.

The A/D and D/A conversion channels feature programmable input/output gains with ranges 38 dB and 21 dB respectively. An on-chip reference voltage is included to allow single-supply operation.

The sampling rate of the codecs is programmable with four separate settings offering 64 kHz, 32 kHz, 16 kHz, and 8 kHz sampling rates (from a master clock of 16.384 MHz).

A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines. The SPORT transfer rate is programmable to allow interfacing to both fast and slow DSP engines.

The AD73322L is available in 28-lead SOIC, 28-lead TSSOP, and 44-lead LQFP packages.

REV. 0

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AD73322L–SPECIFICATIONS[1] (AVDD = 3 V ± 10%; DVDD = 3 V ± 10%; DGND = AGND = 0 V, f_{DMCLK} = 16.384 MHz, f_{SAMP} = 8 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	A, Y Versions Min	Typ	Max	Unit	Test Conditions/Comments
REFERENCE					
REFCAP					
Absolute Voltage, VREFCAP	1.08	1.2	1.32	V	
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from
REFOUT					REFCAP to AGND2
Typical Output Impedance		130		Ω	
Absolute Voltage, V_{REFOUT}	1.08	1.2	1.32	V	Unloaded
Minimum Load Resistance		1		kΩ	
Maximum Load Capacitance		100		pF	
INPUT AMPLIFIER					
Offset		±1.0		mV	
Maximum Output Swing		1.578		V	Max Output Swing = (1.578/1.2) × VREFCAP
Feedback Resistance		50		kΩ	f_C = 32 kHz
Feedback Capacitance		100		pF	
ANALOG GAIN TAP					
Gain at Maximum Setting		+1			
Gain at Minimum Setting		–1			
Gain Resolution		5		Bits	Gain Step Size = 0.0625
Gain Accuracy		±1.0		%	Output Unloaded
Settling Time		1.0		µs	Tap Gain Change of –FS to +FS
Delay		0.5		µs	
ADC SPECIFICATIONS					DAC Unloaded
Maximum Input Range at VIN[2, 3]		1.578		V p-p	Measured Differentially
		–2.85		dBm	Max Input = (1.578/1.2) × VREFCAP
Nominal Reference Level at VIN		1.0954		V p-p	Measured Differentially
(0 dBm0)		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–2.0	–0.7	+0.5	dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					Refer to TPC 1.
PGA = 0 dB	70	78		dB	300 Hz to 3400 Hz; f_{SAMP} = 8 kHz, PUIA = 0
		79		dB	300 Hz to 3400 Hz; f_{SAMP} = 8 kHz, PUIA = 1
		77.5		dB	0 Hz to f_{SAMP}/2; f_{SAMP} = 8 kHz
Total Harmonic Distortion					
PGA = 0 dB		–86	–75	dB	300 Hz to 3400 Hz; f_{SAMP} = 8 kHz
Intermodulation Distortion		–61		dB	PGA = 0 dB
Idle Channel Noise Crosstalk		–72		dBm0	PGA = 0 dB
ADC-to-DAC		–107		dB	ADC Input Signal Level: 1.0 kHz, 0 dBm0
					DAC Input at Idle
ADC-to-ADC		–92		dB	ADC1 Input Signal Level: 1.0 kHz, 0 dBm0
					ADC2 Input at Idle. Input Amplifiers Bypassed
		–93		dB	Input Amplifiers Included in Input Channel
DC Offset	–20	0	+20	mV	PGA = 0 dB
Power Supply Rejection		–65		dB	Input Signal Level at AVDD and DVDD
					Pins: 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	
Input Resistance at PGA[2, 4, 6]		20		kΩ	Input Amplifiers Bypassed
DIGITAL GAIN TAP					
Gain at Maximum Setting		+1			
Gain at Minimum Setting		–1			
Gain Resolution		16		Bits	Tested to 5 MSBs of Settings
Delay		25		µs	Includes DAC Delay
Settling Time		100		µs	Tap Gain Change from –FS to +FS; Includes
					DAC Settling Time

Parameter	A, Y Versions Min	Typ	Max	Unit	Test Conditions/Comments
DAC SPECIFICATIONS					DAC Unloaded
Maximum Voltage Output Swing[2]					
Single-Ended		1.578		V p-p	PGA = 6 dB
		–2.85		dBm	Max Output = (1.578/1.2) × VREFCAP
Differential		3.156		V p-p	PGA = 6 dB
		3.17		dBm	Max Output = 2 × ([1.578/1.2] × VREFCAP)
Nominal Voltage Output Swing (0 dBm0)					
Single-Ended		1.0954		V p-p	PGA = 6 dB
		–6.02		dBm	
Differential		2.1909		V p-p	PGA = 6 dB
		0		dBm	
Output Bias Voltage		1.2		V	REFOUT Unloaded
Absolute Gain	–1.75	–0.6	+0.75	dB	1.0 kHz, 0 dBm0; Unloaded
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion) at 0 dBm0					Refer to TPC 2.
PGA = 0 dB	72	78.5		dB	300 Hz to 3400 Hz; f_{SAMP} = 8 kHz
Total Harmonic Distortion at 0 dBm0					
PGA = 0 dB		–89	–75	dB	300 Hz to 3400 Hz; f_{SAMP} = 8 kHz
Intermodulation Distortion		–77		dB	PGA = 0 dB
Idle Channel Noise Crosstalk		–81		dBm0	PGA = 0 dB
DAC-to-ADC		–73		dB	ADC Input Signal Level: AGND; DAC Output Signal Level: 1.0 kHz, 0 dBm0 Input Amplifiers Bypassed
		–74		dB	Input Amplifiers Included in Input Channel
DAC-to-DAC		–102		dB	DAC1 Output Signal Level: AGND; DAC2 Output Signal Level: 1.0 kHz, 0 dBm0
Power Supply Rejection		–65		dB	Input Signal Level at AVDD and DVDD Pins: 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	Interpolator Bypassed
		50		µs	
Output DC Offset[2, 7]	–50	+5	+60	mV	
Minimum Load Resistance, R_L[2, 8]					
Single-Ended[4]		150		Ω	
Differential		150		Ω	
Maximum Load Capacitance, C_L[2, 8]					
Single-Ended		500		pF	
Differential		100		pF	
FREQUENCY RESPONSE					
(ADC and DAC)[9] Typical Output					
Frequency (Normalized to FS)					
0		0		dB	
0.03125		–0.1		dB	
0.0625		–0.25		dB	
0.125		–0.6		dB	
0.1875		–1.4		dB	
0.25		–2.8		dB	
0.3125		–4.5		dB	
0.375		–7.0		dB	
0.4375		–9.5		dB	
> 0.5		< –12.5		dB	

Parameter	A, Y Versions Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
V_{INH}, Input High Voltage	DVDD – 0.8		DVDD	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current	–10		+10	μA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	DVDD – 0.4		DVDD	V	|IOUT| ≤ 100 μA
V_{OL}, Output Low Voltage	0		0.4	V	|IOUT| ≤ 100 μA
Three-State Leakage Current	–10		+10	μA	
POWER SUPPLIES					
AVDD1, AVDD2	2.7		3.3	V	
DVDD	2.7		3.3	V	
I_{DD}[10]					See Table I

NOTES
[1] Operating temperature range as follows: A Grade, T_{MIN} = –40°C, T_{MAX} = +85°C; Y Grade, T_{MIN} = –40°C, T_{MAX} = +105°C.
[2] Test conditions: Input PGA set for 0 dB gain, Output PGA set for 6 dB gain, no load on analog outputs (unless otherwise noted).
[3] At input to sigma-delta modulator of ADC.
[4] Guaranteed by design.
[5] Overall group delay will be affected by the sample rate and the external digital filtering.
[6] The ADC's input impedance is inversely proportional to DMCLK and is approximated by: (3.3×10^{11})/DMCLK.
[7] Between VOUTP1 and VOUTN1 or between VOUTP2 and VOUTN2.
[8] At VOUT output.
[9] Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.
[10] Test Conditions: no load on digital inputs, analog inputs ac-coupled to ground, no load on analog outputs.

Specifications subject to change without notice.

Table I. Current Summary (AVDD = DVDD = 3.3 V)

Conditions	Analog Current	Digital Current	Total Current (Typ)	Total Current (Max)	SE	MCLK ON	Comments
ADCs On Only	3.4	6.3	9.7	12	1	YES	REFOUT Disabled
DACs On Only	8.8	6.5	15.3	20	1	YES	REFOUT Disabled
ADCs and DACs On	11.6	7.0	18.6	23	1	YES	REFOUT Disabled
ADCs and DACs and Input Amps On	13.8	7.0	20.8	26	1	YES	REFOUT Disabled
ADCs and DACs and AGT On	13.2	7.0	20.2	26	1	YES	REFOUT Disabled
All Sections On	17.2	7.0	24.2	31	1	YES	
REFCAP On Only	0.65	0	0.67	1.25	0	NO	REFOUT Disabled
REFCAP and REFOUT On Only	2.56	0	2.57	4.5	0	NO	
All Sections Off	0	1.25	1.25	1.8	0	YES	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0 μA	12.5 μA	12.7 μA	40 μA	0	NO	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA and are typical values unless otherwise noted.

Table II. Signal Ranges

		3 V Power Supply 5VEN = 0
VREFCAP		1.2 V ± 10%
VREFOUT		1.2 V ± 10%
ADC	Maximum Input Range at V_{IN}	1.578 V p-p
	Nominal Reference Level	1.0954 V p-p
DAC	Maximum Voltage Output Swing	
	Single-Ended	1.578 V p-p
	Differential	3.156 V p-p
	Nominal Voltage Output Swing	
	Single-Ended	1.0954 V p-p
	Differential	2.1909 V p-p
	Output Bias Voltage	VREFOUT

TIMING CHARACTERISTICS

(AVDD = 3 V ± 10%; DVDD = 3 V ± 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

Parameter	Limit at T_A = −40°C to +105°C	Unit	Description
Clock Signals			See Figure 1
t_1	61	ns min	MCLK Period
t_2	24.4	ns min	MCLK Width High
t_3	24.4	ns min	MCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period
t_5	$0.4 \times t_1$	ns min	SCLK Width High
t_6	$0.4 \times t_1$	ns min	SCLK Width Low
t_7	20	ns min	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns min	SDI/SDIFS Hold After SCLK Low
t_9	10	ns max	SDOFS Delay from SCLK High
t_{10}	10	ns min	SDOFS Hold After SCLK High
t_{11}	10	ns min	SDO Hold After SCLK High
t_{12}	10	ns max	SDO Delay from SCLK High
t_{13}	30	ns max	SCLK Delay from MCLK

Specifications subject to change without notice.

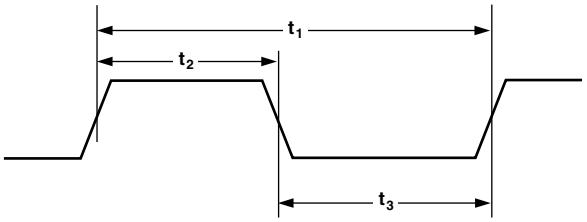


Figure 1. MCLK Timing

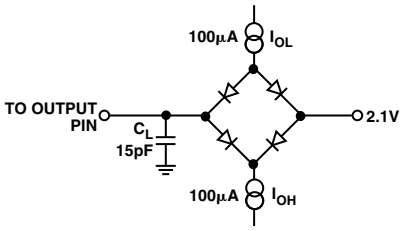


Figure 2. Load Circuit for Timing Specifications

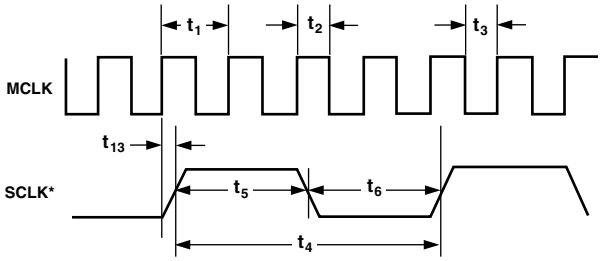


Figure 3. SCLK Timing

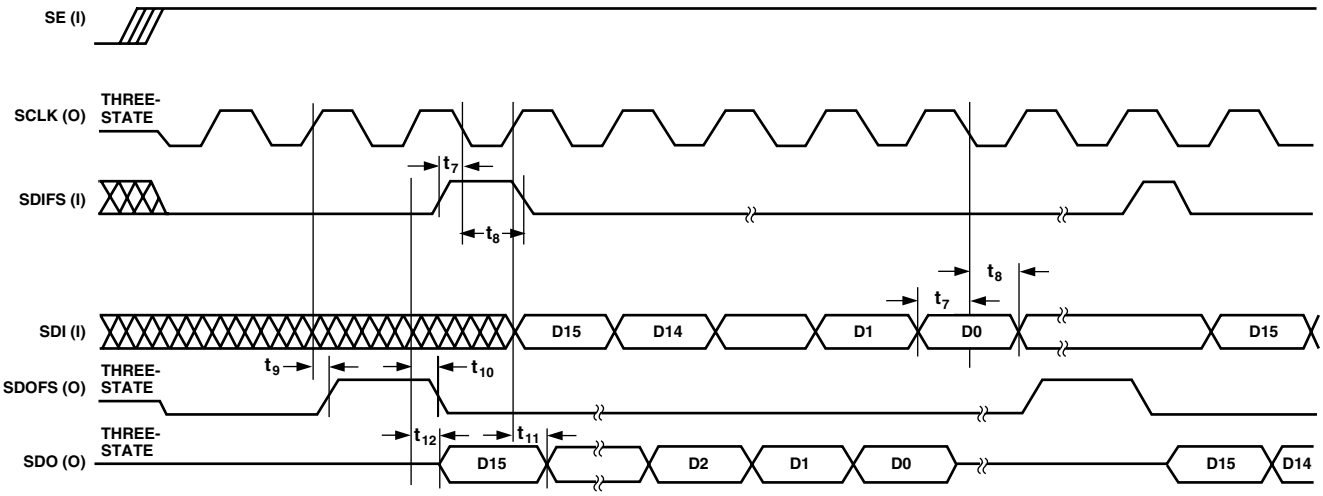


Figure 4. Serial Port (SPORT)

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted)

AVDD, DVDD to GND . . . . . –0.3 V to +4.6 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . –0.3 V to (DVDD + 0.3 V)
Analog I/O Voltage to AGND . . . –0.3 V to (AVDD + 0.3 V)
Operating Temperature Range
  Industrial (A Version) . . . . . –40°C to +85°C
  Extended (Y Version) . . . . . –40°C to +105°C
Storage Temperature Range . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
SOIC, θ_{JA} Thermal Impedance . . . . . 71.4°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C
LQFP, θ_{JA} Thermal Impedance . . . . . 53.2°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C
TSSOP, θ_{JA} Thermal Impedance . . . . . 97.9°C/W
Lead Temperature, Soldering
  Vapor Phase (60 sec) . . . . . 215°C
  Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

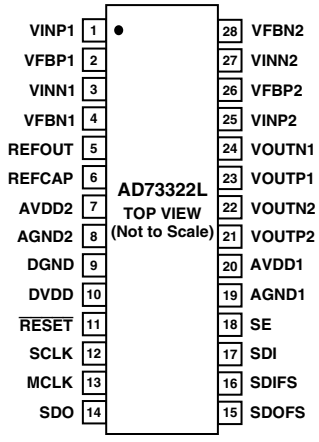
Model	Temperature Range	Package Descriptions	Package Option
AD73322LAR	–40°C to +85°C	Wide Body SOIC	R-28
AD73322LARU	–40°C to +85°C	Thin Shrink TSSOP	RU-28
AD73322LAST	–40°C to +85°C	Plastic Thin Quad Flatpack (LQFP)	ST-44A
AD73322LYR	–40°C to +105°C	Wide Body SOIC	R-28
AD73322LYRU	–40°C to +105°C	Thin Shrink TSSOP	RU-28
AD73322LYST	–40°C to +105°C	Plastic Thin Quad Flatpack (LQFP)	ST-44A
EVAL-AD73322LEB		Evaluation Board	

CAUTION

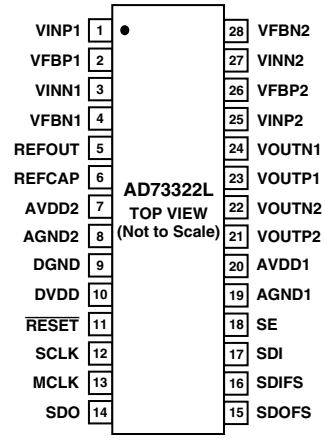
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73322L features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

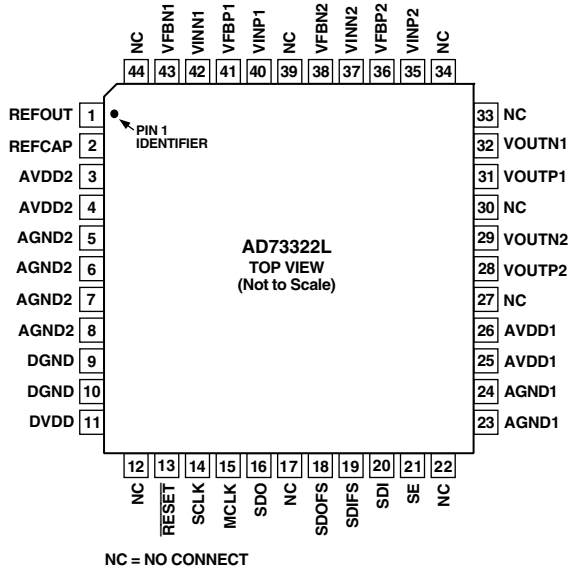
28-Lead Wide Body SOIC (R-28)



28-Lead Thin Shrink TSSOP (RU-28)



44-Lead Plastic Thin Quad Flatpack (LQFP) (ST-44A)



NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Mnemonic	Function
VINP1	Analog Input to the inverting input amplifier on Channel 1's positive input.
VFBP1	Feedback Connection from the output of the inverting amplifier on Channel 1's positive input. When the input amplifiers are bypassed, this pin allows direct access to the positive input of Channel 1's sigma-delta modulator.
VINN1	Analog Input to the inverting input amplifier on Channel 1's negative input.
VFBN1	Feedback connection from the output of the inverting amplifier on Channel 1's negative input. When the input amplifiers are bypassed, this pin allows direct access to the negative input of Channel 1's sigma-delta modulator.
REFOUT	Buffered Reference Output, which has a nominal value of 1.2 V or 2.4 V, the value being dependent on the status of Bit 5VEN (CRC:7). As the reference is common to the two codec units, the reference value is set by the wired OR of the CRC:7 bits in Control Register C of each channel.
REFCAP	A bypass capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin.
AVDD2	Analog Power Supply Connection.
AGND2	Analog Ground/Substrate Connection2.
DGND	Digital Ground/Substrate Connection.
DVDD	Digital Power Supply Connection.
$\overline{\text{RESET}}$	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
SCLK	Serial Clock Output whose rate determines the serial transfer rate to/from the codec. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider.
MCLK	Master Clock Input. MCLK is driven from an external clock signal.
SDO	Serial Data Output. Both data and control information may be output on this pin and are clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one bit wide and is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one bit wide and is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low.
SDI	Serial Data Input. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.
SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low); however, the timing counters and other internal registers are at their reset values.
AGND1	Analog Ground/Substrate Connection.
AVDD1	Analog Power Supply Connection.
VOUTP2	Analog Output from the Positive Terminal of Output Channel 2.
VOUTN2	Analog Output from the Negative Terminal of Output Channel 2.
VOUTP1	Analog Output from the Positive Terminal of Output Channel 1.
VOUTN1	Analog Output from the Negative Terminal of Output Channel 1.
VINP2	Analog Input to the inverting input amplifier on Channel 2's positive input.
VFBP2	Feedback connection from the output of the inverting amplifier on Channel 2's positive input. When the input amplifiers are bypassed, this pin allows direct access to the positive input of Channel 2's sigma-delta modulator.
VINN2	Analog Input to the inverting input amplifier on Channel 2's negative input.
VFBN2	Feedback connection from the output of the inverting amplifier on Channel 2's negative input. When the input amplifiers are bypassed, this pin allows direct access to the negative input of Channel 2's sigma-delta modulator.

TERMINOLOGY

Absolute Gain
Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured (differentially) with a 1 kHz sine wave at 0 dBm0 for the DAC and with a 1 kHz sine wave at 0 dBm0 for the ADC. The absolute gain specification is used for gain tracking error specification.

Crosstalk
Crosstalk is due to coupling of signals from a given channel to an adjacent channel. It is defined as the ratio of the amplitude of the coupled signal to the amplitude of the input signal. Crosstalk is expressed in dB.

Gain Tracking Error
Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 0 dBm0 (equal to absolute gain) at 1 kHz for the DAC and 0 dBm0 (equal to absolute gain) at 1 kHz for the ADC. Gain tracking error at 0 dBm0 (ADC) and 0 dBm0 (DAC) is 0 dB by definition.

Group Delay
Group Delay is defined as the derivative of radian phase with respect to radian frequency, dø(f)/df. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay from a constant indicates the degree of nonlinear phase response of the system.

Idle Channel Noise
Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300 Hz–3400 Hz).

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n is equal to zero. For final testing, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Power Supply Rejection
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

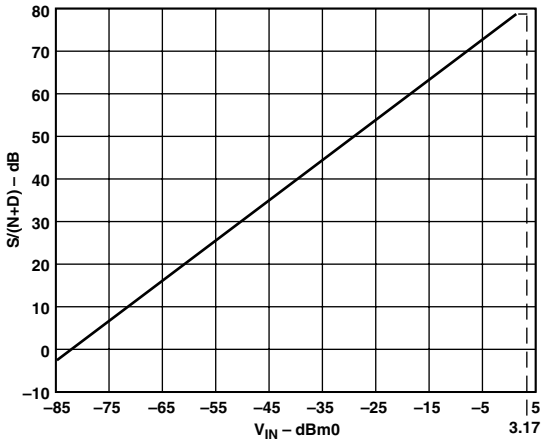
Sample Rate
The sample rate is the rate at which the ADC updates its output register and the DAC updates its output from its input register. The sample rate can be chosen from a list of four that are fixed relative to the DMCLK. Sample rate is set by programming bits DIR0-1 in Control Register B of each channel.

SNR+THD
Signal-to-noise ratio plus harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300 Hz–3400 Hz, including harmonics but excluding dc.

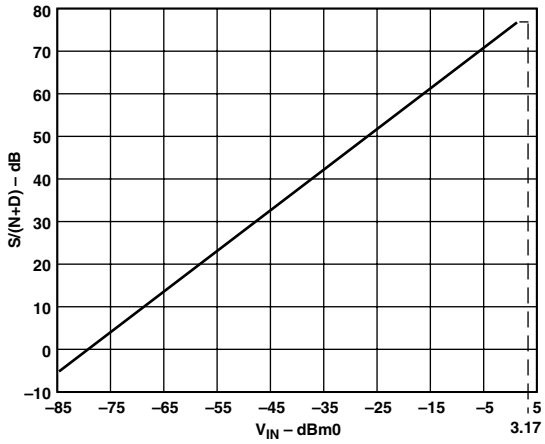
ABBREVIATIONS

ADC	Analog-to-Digital Converter.
AFE	Analog Front End.
AGT	Analog Gain Tap.
ALB	Analog Loop-Back.
BW	Bandwidth.
CRx	A Control Register where *x* is a placeholder for an alphabetic character (A–E). There are five read/write control registers on the AD73322L—designated CRA through CRE.
CRx:n	A bit position, where *n* is a placeholder for a numeric character (0–7), within a control register, where *x* is a placeholder for an alphabetic character (A–E). Position 7 represents the MSB and Position 0 represents the LSB.
DAC	Digital-to-Analog Converter.
DGT	Digital Gain Tap.
DLB	Digital Loop-Back.
DMCLK	Device (Internal) Master Clock. This is the internal master clock resulting from the external master clock (MCLK) being divided by the on-chip master clock divider.
FS	Full Scale.
FSLB	Frame Sync Loop-Back—where the SDOFS of the final device in a cascade is connected to the RFS and TFS of the DSP and the SDIFS of first device in the cascade. Data input and output occur simultaneously. In the case of NonFSLB, SDOFS and SDO are connected to the Rx Port of the DSP while SDIFS and SDI are connected to the Tx Port.
PGA	Programmable Gain Amplifier.
SC	Switched Capacitor.
SLB	Sport Loop-Back.
SNR	Signal-to-Noise Ratio.
SPORT	Serial Port.
THD	Total Harmonic Distortion.
VBW	Voice Bandwidth.

AD73322L–Typical Performance Characteristics



TPC 1. S/(N+D) vs. V_{IN} (ADC @ 3 V) over Voiceband Bandwidth (300 Hz–3.4 kHz)



TPC 2. S/(N+D) vs. V_{IN} (DAC @ 3 V) over Voiceband Bandwidth (300 Hz–3.4 kHz)

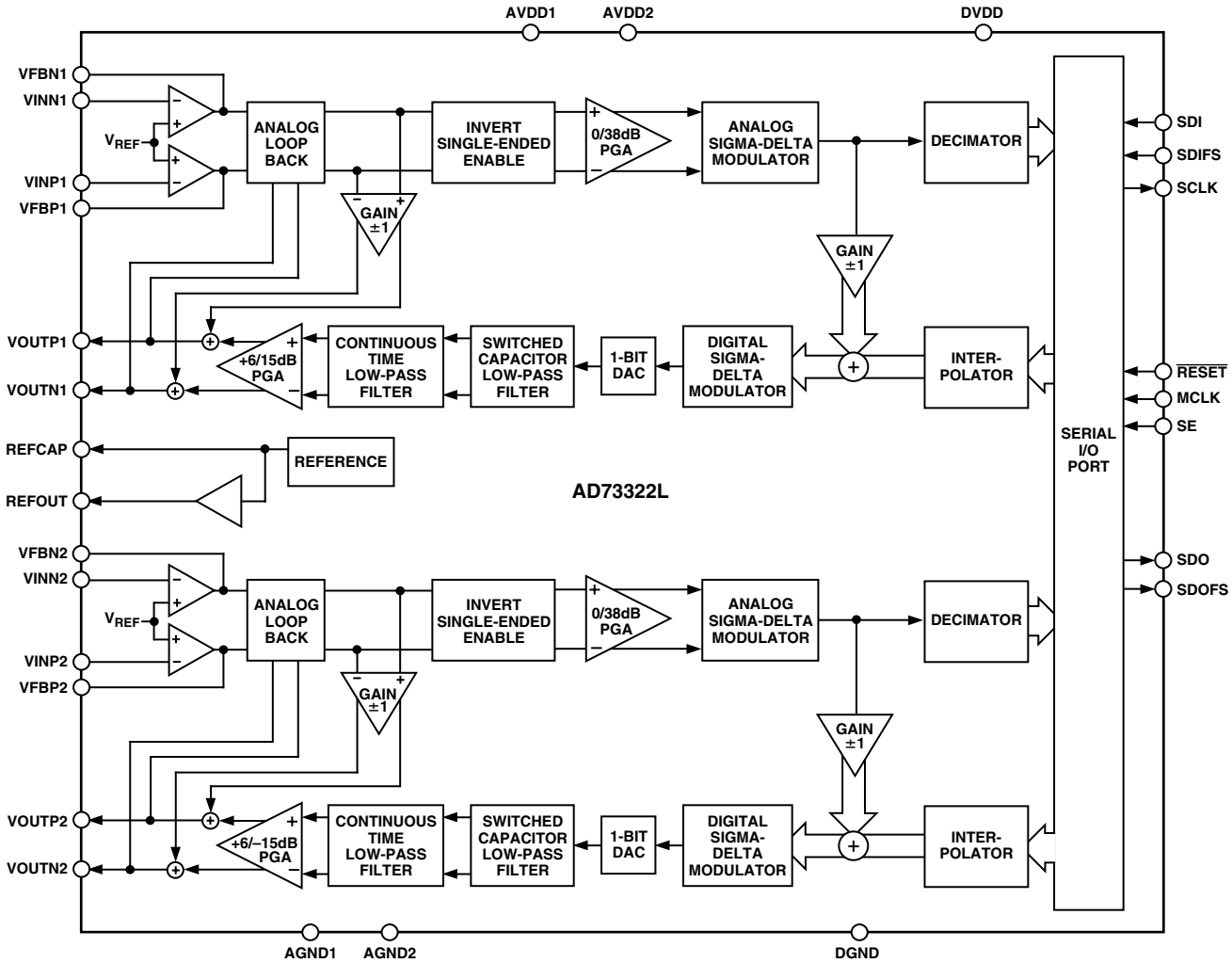


Figure 5. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Encoder Channels

Both encoder channels consist of a pair of inverting op amps with feedback connections that can be bypassed if required, a switched capacitor PGA and a sigma-delta analog-to-digital converter (ADC). An on-board digital filter, which forms part of the sigma-delta ADC, also performs critical system-level filtering. Due to the high level of oversampling, the input antialias requirements are reduced such that a simple single pole RC stage is sufficient to give adequate attenuation in the band of interest.

Programmable Gain Amplifier

Each encoder section's analog front end comprises a switched capacitor PGA, which also forms part of the sigma-delta modulator. The SC sampling frequency is DMCLK/8. The PGA, whose programmable gain settings are shown in Table III, may be used to increase the signal level applied to the ADC from low output sources such as microphones, and can be used to avoid placing external amplifiers in the circuit. The input signal level to the sigma-delta modulator should not exceed the maximum input voltage permitted.

The PGA gain is set by bits IGS0, IGS1 and IGS2 (CRD:0–2) in control register D.

Table III. PGA Settings for the Encoder Channel

IGS2	IGS1	IGS0	Gain (dB)
0	0	0	0
0	0	1	6
0	1	0	12
0	1	1	18
1	0	0	20
1	0	1	26
1	1	0	32
1	1	1	38

ADC

Both ADCs consist of an analog sigma-delta modulator and a digital antialiasing decimation filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a DMCLK/8 rate. This bitstream, representing the analog input signal, is input to the antialiasing decimation filter. The decimation filter reduces the sample rate and increases the resolution.

Analog Sigma-Delta Modulator

The AD73322L's input channels employ a sigma-delta conversion technique, which provides a high resolution 16-bit output with system filtering being implemented on-chip.

Sigma-delta converters employ a technique known as oversampling, where the sampling rate is many times the highest frequency of interest. In the case of the AD73322L, the initial sampling rate of the sigma-delta modulator is DMCLK/8. The main effect of oversampling is that the quantization noise is spread over a very wide bandwidth, up to $F_S/2$ = DMCLK/16 (Figure 7a). This means that the noise in the band of interest is much reduced. Another complementary feature of sigma-delta converters is the use of a technique called noise-shaping. This technique has the effect of pushing the noise from the band of interest to an out-of-band position (Figure 7b). The combination of these techniques, followed by the application of a digital filter, sufficiently reduces the noise in band to ensure good dynamic performance from the part (Figure 7c).

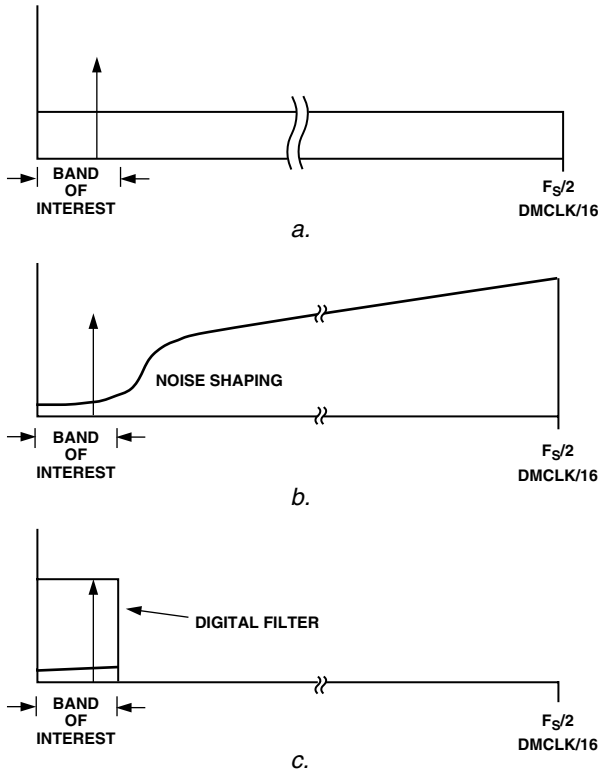
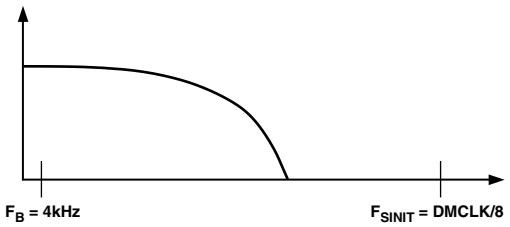
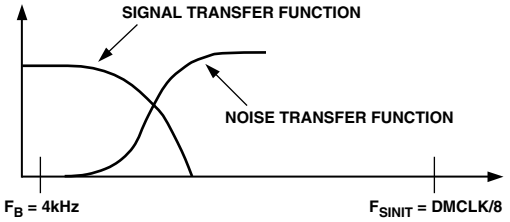


Figure 6. Sigma-Delta Noise Reduction

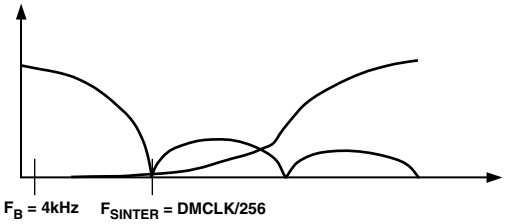
Figure 7 shows the various stages of filtering that are employed in a typical AD73322L application. In Figure 7a we see the transfer function of the external analog antialias filter. Even though it is a single RC pole, its cutoff frequency is sufficiently far away from the initial sampling frequency (DMCLK/8) that it takes care of any signals that could be aliased by the sampling frequency. This also shows the major difference between the initial oversampling rate and the bandwidth of interest. In Figure 7b, the signal and noise-shaping responses of the sigma-delta modulator are shown. The signal response provides further rejection of any high frequency signals while the noise-shaping will push the inherent quantization noise to an out-of-band position. The detail of Figure 7c shows the response of the digital decimation filter (Sinc-cubed response) with nulls every multiple of DMCLK/256, which corresponds to the decimation filter update rate for a 64 kHz sampling. The nulls of the Sinc3 response correspond with multiples of the chosen sampling frequency. The final detail in Figure 7d shows the application of a final antialias filter in the DSP engine. This has the advantage of being implemented according to the user's requirements and available MIPS. The filtering in Figures 7a through 7c is implemented in the AD73322L.



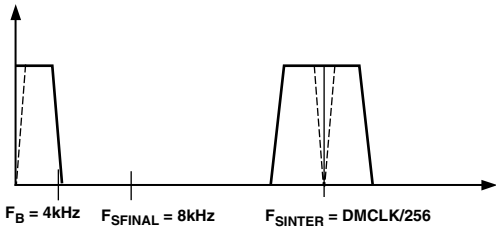
a. Analog Antialias Filter Transfer Function



b. Analog Sigma-Delta Modulator Transfer Function



c. Digital Decimator Transfer Function



d. Final Filter LPF (HPF) Transfer Function

Figure 7. ADC Frequency Responses

Decimation Filter

The digital filter used in the AD73322L carries out two important functions. Firstly, it removes the out-of-band quantization noise, which is shaped by the analog modulator and secondly, it decimates the high frequency bit stream to a lower rate 16-bit word.

The antialiasing decimation filter is a sinc-cubed digital filter that reduces the sampling rate from DMCLK/8 to DMCLK/256, and increases the resolution from a single bit to 15 bits or greater (depending on chosen sampling rate). Its Z transform is given as:

$$[(1 - Z^{-N})/(1 - Z^{-1})]^3$$

where N is set by the sampling rate (N = 32 @ 64 kHz sampling. . . N = 256 @ 8 kHz sampling). Thus when the sampling rate is 64 kHz, a minimal group delay of 25 µs can be achieved.

Word growth in the decimator is determined by the sampling rate. At 64 kHz sampling, where the oversampling ratio between sigma-delta modulator and decimator output equals 32, there are five bits per stage of the three-stage Sinc3 filter. Due to symmetry within the sigma-delta modulator, the LSB will always be a zero; therefore, the 16-bit ADC output word will have 2 LSBs equal to zero, one due to the sigma-delta symmetry and the other being a padding zero to make up the 16-bit word. At lower sampling rates, decimator word growth will be greater than the 16-bit sample word, therefore truncation occurs in transferring the decimator output as the ADC word. For example, at 8 kHz sampling, word growth reaches 24 bits due to the OSR of 256 between sigma-delta modulator and decimator output. This yields eight bits per stage of the three-stage Sinc3 filter.

ADC Coding

The ADC coding scheme is in twos complement format (see Figure 8). The output words are formed by the decimation filter, which grows the word length from the single-bit output of the sigma-delta modulator to a word length of up to 24 bits (depending on decimation rate chosen), which is the final output of the ADC block. In Data Mode this value is truncated to 16 bits for output on the Serial Data Output (SDO) pin.

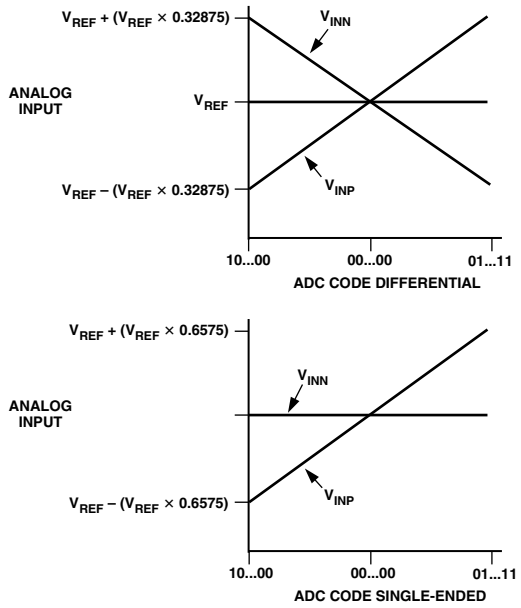


Figure 8. ADC Transfer Function

In mixed Control/Data Mode, the resolution is fixed at 15 bits, with the MSB of the 16-bit transfer being used as a flag bit to indicate either control or data in the frame.

Decoder Channel

The decoder channels consist of digital interpolators, digital sigma-delta modulators, single-bit digital-to-analog converters (DAC), analog smoothing filters and programmable gain amplifiers with differential outputs.

DAC Coding

The DAC coding scheme is in twos complement format with 0x7FFF being full-scale positive and 0x8000 being full-scale negative.

Interpolation Filter

The anti-imaging interpolation filter is a sinc-cubed digital filter that up-samples the 16-bit input words from the input sample rate to a rate of DMCLK/8, while filtering to attenuate images produced by the interpolation process. Its Z transform is given as:

$$[(1 - Z^{-N})/(1 - Z^{-1})]^3$$

where N is determined by the sampling rate (N = 32 @ 64 kHz . . . N = 256 @ 8 kHz). The DAC receives 16-bit samples from the host DSP processor at the programmed sample rate of DMCLK/N. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered by the anti-imaging interpolation filter, but there is an option to bypass the interpolator for the minimum group delay configuration by setting the IBYP bit (CRE:5) of Control register E. The interpolation filter has the same characteristics as the ADC's antialiasing decimation filter.

The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples at a rate of DMCLK/8. The modulator noise-shapes the signal so that errors inherent to the process are minimized in the passband of the converter. The bit-stream output of the sigma-delta modulator is fed to the single-bit DAC where it is converted to an analog voltage.

Analog Smoothing Filter and PGA

The output of the single-bit DAC is sampled at DMCLK/8, therefore it is necessary to filter the output to reconstruct the low frequency signal. The decoder's analog smoothing filter consists of a continuous-time filter preceded by a third-order switched-capacitor filter. The continuous-time filter forms part of the output programmable gain amplifier (PGA). The PGA can be used to adjust the output signal level from –15 dB to +6 dB in 3 dB steps, as shown in Table IV. The PGA gain is set by bits OGS0, OGS1 and OGS2 (CRD:4-6) in Control Register D.

Table IV. PGA Settings for the Decoder Channel

OGS2	OGS1	OGS0	Gain (dB)
0	0	0	+6
0	0	1	+3
0	1	0	0
0	1	1	–3
1	0	0	–6
1	0	1	–9
1	1	0	–12
1	1	1	–15

Differential Output Amplifiers

The decoder has a differential analog output pair (VOUTP and VOUTN). The output channel can be muted by setting the MUTE bit (CRD:7) in Control Register D. The output signal is dc-biased to the codec's on-chip voltage reference.

Voltage Reference

The AD73322L reference, REFCAP, is a bandgap reference that provides a low noise, temperature-compensated reference to the DAC and ADC. A buffered version of the reference is also made available on the REFOUT pin and can be used to bias other external analog circuitry. The reference has a default nominal value of 1.2 V.

The reference output (REFOUT) can be enabled for biasing external circuitry by setting the RU bit (CRC:6) of CRC.

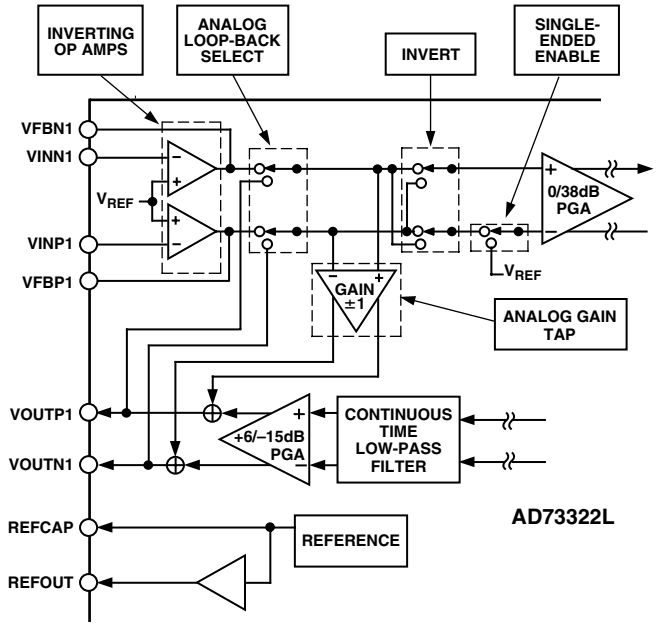


Figure 9. Analog Input/Output Section

Analog and Digital Gain Taps

The AD73322L features analog and digital feedback paths between input and output. The amount of feedback is determined by the gain setting which is programmed in the control registers. This feature can typically be used for balancing the effective impedance between input and output when used in Subscriber Line Interface Circuit (SLIC) interfacing.

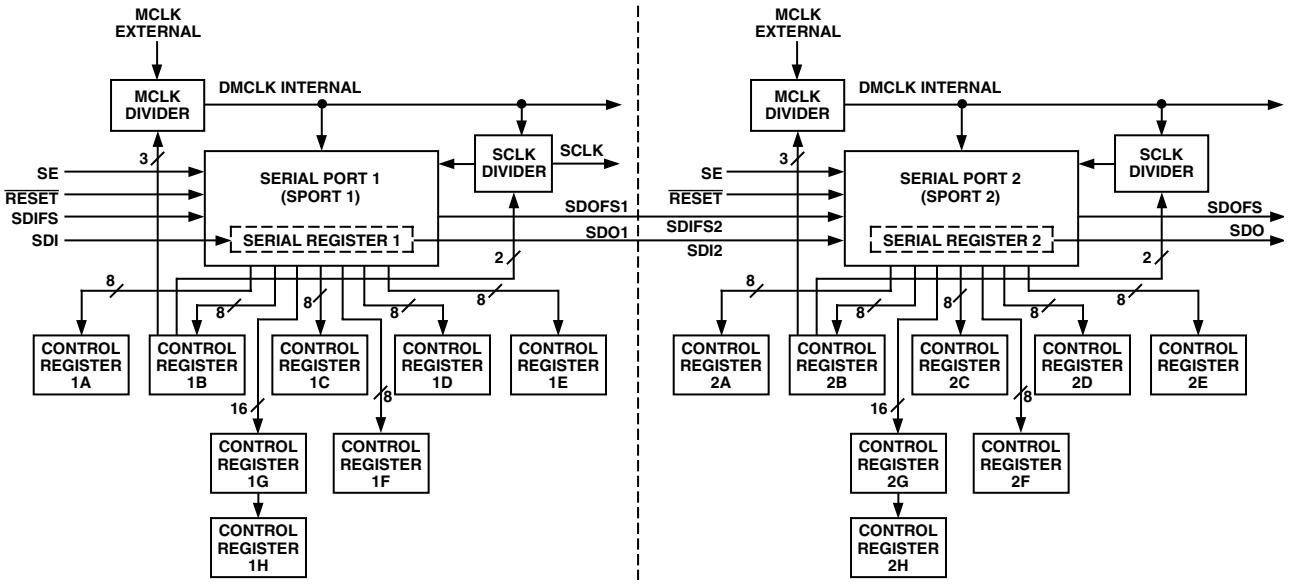


Figure 10. SPORT Block Diagram

Analog Gain Tap

The analog gain tap is configured as a programmable differential amplifier whose input is taken from the ADC's input signal path. The output of the analog gain tap is summed with the output of the DAC. The gain is programmable using Control Register F (CRF:0-4) to achieve a gain of –1 to +1 in 32 steps with muting being achieved through a separate control setting (Control Register F Bit 7). The gain increment per step is 0.0625. The AGT is enabled by powering-up the AGT control bit in the power control register (CRC:1). When this bit is set (=1) CRF becomes an AGT control register with CRF:0-4 holding the AGT coefficient, CRF:5 becomes an AGT enable and CRF:7 becomes an AGT mute control bit. Control bit CRF:5 connects/disconnects the AGT output to the summer block at the output of the DAC section while control bit CRF:7 overrides the gain tap setting with a mute, (zero gain) setting. Table V shows the gain versus digital setting for the AGT.

Table V. Analog Gain Tap Settings*

AGTC4	AGTC3	AGTC2	AGTC1	AGTC0	Gain (dB)
0	0	0	0	0	+1.00
0	0	0	0	1	+0.9375
0	0	0	1	0	+0.875
0	0	0	1	1	+0.8125
0	0	1	0	0	+0.75
0	1	1	1	1	+0.0625
1	0	0	0	0	–0.0625
1	1	1	0	1	–0.875
1	1	1	1	0	–0.9375
1	1	1	1	1	–1.00

*AGT and DGT weights are given for the case of VFBNx (connected to the sigma-delta modulator's positive input) being at a higher potential than VFBPx (connected to the sigma-delta modulator's negative input).

Digital Gain Tap

The digital gain tap features a programmable gain block whose input is taken from the bitstream output of the ADC's sigma-delta modulator. This single bit input (1 or 0) is used to add or subtract a programmable value, which is the digital gain tap setting, to the output of the DAC section's interpolator. The programmable setting has 16-bit resolution and is programmed using the settings in Control Registers G and H. (See Table VI).

Table VI. Digital Gain Tap Settings*

DGT15–0 (Hex)	Gain
0x8000	–1.00
0x9000	–0.875
0xA000	–0.75
0xC000	–0.5
0xE000	–0.25
0x0000	0.00
0x2000	+0.25
0x4000	+0.05
0x6000	+0.75
0x7FFF	+0.99999

*AGT and DGT weights are given for the case of VFBNx (connected to the sigma-delta modulator's positive input) being at a higher potential than VFBPx (connected to the sigma-delta modulator's negative input).

Serial Port (SPORT)

The codecs communicate with a host processor via the bidirectional synchronous serial port (SPORT), which is compatible with most modern DSPs. The SPORT is used to transmit and receive digital data and control information. The dual codec is implemented using two separate codec blocks that are internally cascaded with serial port access to the input of Codec1 and the output of Codec2. This allows other single or dual codec devices to be cascaded together (up to a limit of eight codec units).

In both transmit and receive modes, data is transferred at the serial clock (SCLK) rate with the MSB being transferred first. Due to the fact that the SPORT of each codec block uses a common serial register for serial input and output, communications between an AD73322L codec and a host processor (DSP engine) must always be initiated by the codecs themselves. In this configuration the codecs are described as being in Master mode. This ensures that there is no collision between input data and output samples.

SPORT Overview

The AD73322L SPORT is a flexible, full-duplex, synchronous serial port whose protocol has been designed to allow up to four AD73322L devices (or combinations of AD73322L dual codecs and AD73311 single codecs up to eight codec blocks) to be connected, in cascade, to a single DSP via a six-wire interface. It has a very flexible architecture that can be configured by programming two of the internal control registers in each codec block. The AD73322L SPORT has three distinct modes of operation: Control Mode, Data Mode and Mixed Control/Data Mode.

NOTE: As each codec has its own SPORT section, the register settings in both SPORTs must be programmed. The registers that control SPORT and sample rate operation (CRA and CRB) must be programmed with the same values, otherwise incorrect operation may occur.

In Control Mode (CRA:0 = 0), the device's internal configuration can be programmed by writing to the eight internal control registers. In this mode, control information can be written to or read from the codec. In Data Mode (CRA:0 = 1), (CRA:1 = 0), information sent to the device is used to update the decoder section (DAC), while the encoder section (ADC) data is read from the device. In this mode, only DAC and ADC data is written to or read from the device. Mixed mode (CRA:0 = 1 and CRA:1 = 1) allows the user to choose whether the information being sent to the device contains either control information or DAC data. This is achieved by using the MSB of the 16-bit frame as a flag bit. Mixed mode reduces the resolution to 15 bits with the MSB being used to indicate whether the information in the 16-bit frame is control information or DAC/ADC data.

The SPORT features a single 16-bit serial register that is used for both input and output data transfers. As the input and output data must share the same register, some precautions must be observed. The primary precaution is that no information must be written to the SPORT without reference to an output sample event, which is when the serial register will be overwritten with the latest ADC sample word. Once the SPORT starts to output the latest ADC word, it is safe for the DSP to write new control or data words to the codec. In certain configurations, data can be written to the device to coincide with the output sample being shifted out of the serial register—see section on interfacing devices. The serial clock rate (CRB:2–3) defines how many 16-bit words can be written to a device before the next output sample event will happen.

The SPORT block diagram shown in Figure 10 details the blocks associated with Codecs 1 and 2, including the eight control registers (A–H), external MCLK to internal DMCLK divider and serial clock divider. The divider rates are controlled by the setting of Control Register B. The AD73322L features a master clock divider that allows users the flexibility of dividing externally available high frequency DSP or CPU clocks to generate a lower frequency master clock internally in the codec, which may be more suitable for either serial transfer or sampling rate requirements. The master clock divider has five divider options (÷1 default condition, ÷2, ÷3, ÷4, ÷5) that are set by loading the master clock divider field in Register B with the appropriate code (see Table VII). Once the internal device master clock (DMCLK) has been set using the master clock divider, the sample rate and serial clock settings are derived from DMCLK.

The SPORT can work at four different serial clock (SCLK) rates: chosen from DMCLK, DMCLK/2, DMCLK/4 or DMCLK/8, where DMCLK is the internal or device master clock resulting from the external or pin master clock being divided by the master clock divider.

SPORT Register Maps

There are two register banks for each codec in the AD73322L: the control register bank and the data register bank. The control register bank consists of eight read/write registers, each eight bits wide. Table XI shows the control register map for the AD73322L. The first two control registers, CRA and CRB, are reserved for controlling the SPORT. They hold settings for parameters such as serial clock rate, internal master clock rate, sample rate and device count. As both codecs are internally cascaded, registers CRA and CRB on each codec must be programmed with the same setting to ensure correct operation (this is shown in the programming examples). The other five registers; CRC through CRH are used to hold control settings for the ADC, DAC, Reference, Power Control and Gain Tap sections of the device. It is not necessary that the contents of CRC through CRH on each codec be similar. Control registers are written to on the negative edge of SCLK. The data register bank consists of two 16-bit registers that are the DAC and ADC registers.

Master Clock Divider

The AD73322L features a programmable master clock divider that allows the user to reduce an externally available master clock, at pin MCLK, by one of the ratios 1, 2, 3, 4 or 5 to produce an internal master clock signal (DMCLK) that is used to calculate the sampling and serial clock rates. The master clock divider is programmable by setting CRB:4-6. Table VII shows the division ratio corresponding to the various bit settings. The default divider ratio is divide-by-one.

Table VII. DMCLK (Internal) Rate Divider Settings

MCD2	MCD1	MCD0	DMCLK Rate
0	0	0	MCLK
0	0	1	MCLK/2
0	1	0	MCLK/3
0	1	1	MCLK/4
1	0	0	MCLK/5
1	0	1	MCLK
1	1	0	MCLK
1	1	1	MCLK

Serial Clock Rate Divider

The AD73322L features a programmable serial clock divider that allows users to match the serial clock (SCLK) rate of the data to that of the DSP engine or host processor. The maximum SCLK rate available is DMCLK and the other available rates are: DMCLK/2, DMCLK/4 and DMCLK/8. The slowest rate (DMCLK/8) is the default SCLK rate. The serial clock divider is programmable by setting bits CRB:2–3. Table VIII shows the serial clock rate corresponding to the various bit settings.

Table VIII. SCLK Rate Divider Settings

SCD1	SCD0	SCLK Rate
0	0	DMCLK/8
0	1	DMCLK/4
1	0	DMCLK/2
1	1	DMCLK

Sample Rate Divider

The AD73322L features a programmable sample rate divider that allows users flexibility in matching the codec's ADC and DAC sample rates (decimation/interpolation rates) to the needs of the DSP software. The maximum sample rate available is DMCLK/256, which offers the lowest conversion group delay, while the other available rates are: DMCLK/512, DMCLK/1024 and DMCLK/2048. The slowest rate (DMCLK/2048) is the default sample rate. The sample rate divider is programmable by setting bits CRB:0-1. Table IX shows the sample rate corresponding to the various bit settings.

Table IX. Sample Rate Divider Settings

DIR1	DIR0	SCLK Rate
0	0	DMCLK/2048
0	1	DMCLK/1024
1	0	DMCLK/512
1	1	DMCLK/256

DAC Advance Register

The loading of the DAC is internally synchronized with the unloading of the ADC data in each sampling interval. The default DAC load event happens one SCLK cycle before the SDOFS flag is raised by the ADC data being ready. However, this DAC load position can be advanced before this time by modifying the contents of the DAC advance field in Control Register E (CRE:0–4). The field is five bits wide, allowing 31 increments of weight $1/(F_S \times 32)$; see Table X. The sample rate F_S is dependent on the setting of both the MCLK divider and the Sample Rate divider; see Tables VII and IX. In certain circumstances this DAC update adjustment can reduce the group delay when the ADC and DAC are used to process data in series. Appendix C details how the DAC advance feature can be used.

NOTE: The DAC advance register should not be changed while the DAC section is powered up.

Table X. DAC Timing Control

DA4	DA3	DA2	DA1	DA0	Time Advance
0	0	0	0	0	0 s
0	0	0	0	1	$1/(F_S \times 32)$ s
0	0	0	1	0	$2/(F_S \times 32)$ s
1	1	1	1	0	$30/(F_S \times 32)$ s
1	1	1	1	1	$31/(F_S \times 32)$ s

Table XI. Control Register Map

Address (Binary)	Name	Description	Type	Width	Reset Setting (Hex)
000	CRA	Control Register A	R/$\overline{W}$	8	0x00
001	CRB	Control Register B	R/$\overline{W}$	8	0x00
010	CRC	Control Register C	R/$\overline{W}$	8	0x00
011	CRD	Control Register D	R/$\overline{W}$	8	0x00
100	CRE	Control Register E	R/$\overline{W}$	8	0x00
101	CRF	Control Register F	R/$\overline{W}$	8	0x00
110	CRG	Control Register G	R/$\overline{W}$	8	0x00
111	CRH	Control Register H	R/$\overline{W}$	8	0x00

Table XII. Control Word Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C/$\overline{D}$	R/$\overline{W}$	Device Address			Register Address			Register Data							

Control	Frame	Description
Bit 15	Control/$\overline{Data}$	When set high, it signifies a control word in Program or Mixed Program/Data Modes. When set low, it signifies a data word in Mixed Program/Data Mode or an invalid control word in Program Mode.
Bit 14	Read/$\overline{Write}$	When set low, it tells the device that the data field is to be written to the register selected by the register field setting provided the address field is zero. When set high, it tells the device that the selected register is to be written to the data field in the input serial register and that the new control word is to be output from the device via the serial output.
Bits 13–11	Device Address	This 3-bit field holds the address information. Only when this field is zero is a device selected. If the address is not zero, it is decremented and the control word is passed out of the device via the serial output.
Bits 10–8	Register Address	This 3-bit field is used to select one of the eight control registers on the AD73322L.
Bits 7–0	Register Data	This 8-bit field holds the data that is to be written to or read from the selected register provided the address field is zero.

Table XIII. Control Register A Description

CONTROL REGISTER A

7	6	5	4	3	2	1	0
RESET	**DC2**	**DC1**	**DC0**	**SLB**	**DLB**	**MM**	**DATA/$\overline{\text{PGM}}$**

Bit	Name	Description
0	DATA/$\overline{\text{PGM}}$	Operating Mode (0 = Program; 1 = Data Mode)
1	MM	Mixed Mode (0 = Off; 1 = Enabled)
2	DLB	Digital Loop-Back Mode (0 = Off; 1 = Enabled)
3	SLB	SPORT Loop-Back Mode (0 = Off; 1 = Enabled)
4	DC0	Device Count (Bit 0)
5	DC1	Device Count (Bit 1)
6	DC2	Device Count (Bit 2)
7	RESET	Software Reset (0 = Off; 1 = Initiates Reset)

Table XIV. Control Register B Description

CONTROL REGISTER B

7	6	5	4	3	2	1	0
—	**RU**	**PUREF**	**PUDAC**	**PUADC**	**PUIA**	**PUAGT**	**PU**

Bit	Name	Description
0	DIR0	Decimation/Interpolation Rate (Bit 0)
1	DIR1	Decimation/Interpolation Rate (Bit 1)
2	SCD0	Serial Clock Divider (Bit 0)
3	SCD1	Serial Clock Divider (Bit 1)
4	MCD0	Master Clock Divider (Bit 0)
5	MCD1	Master Clock Divider (Bit 1)
6	MCD2	Master Clock Divider (Bit 2)
7	CEE	Control Echo Enable (0 = Off; 1 = Enabled)

Table XV. Control Register C Description

CONTROL REGISTER C

7	6	5	4	3	2	1	0
MUTE	**OGS2**	**OGS1**	**OGS0**	**RMOD**	**IGS2**	**IGS1**	**IGS0**

Bit	Name	Description
0	PU	Power-Up Device (0 = Power-Down; 1 = Power On)
1	PUAGT	Analog Gain Tap Power (0 = Power-Down; 1 = Power On)
2	PUIA	Input Amplifier Power (0 = Power-Down; 1 = Power On)
3	PUADC	ADC Power (0 = Power-Down; 1 = Power On)
4	PUDAC	DAC Power (0 = Power-Down; 1 = Power On)
5	PUREF	REF Power (0 = Power-Down; 1 = Power On)
6	RU	REFOUT Use (0 = Disable REFOUT; 1 = Enable REFOUT)
7	—	Reserved, must be programmed to 0.

Table XVI. Control Register D Description

CONTROL REGISTER D

7	6	5	4	3	2	1	0
MUTE	OGS2	OGS1	OGS0	RMOD	IGS2	IGS1	IGS0

Bit	Name	Description
0	IGS0	Input Gain Select (Bit 0)
1	IGS1	Input Gain Select (Bit 1)
2	IGS2	Input Gain Select (Bit 2)
3	RMOD	Reset ADC Modulator (0 = Off; 1 = Reset Enabled)
4	OGS0	Output Gain Select (Bit 0)
5	OGS1	Output Gain Select (Bit 1)
6	OGS2	Output Gain Select (Bit 2)
7	MUTE	Output Mute (0 = Mute Off; 1 = Mute Enabled)

Table XVII. Control Register E Description

CONTROL REGISTER E

7	6	5	4	3	2	1	0
—	DGTE	IBYP	DA4	DA3	DA2	DA1	DA0

Bit	Name	Description
0	DA0	DAC Advance Setting (Bit 0)
1	DA1	DAC Advance Setting (Bit 1)
2	DA2	DAC Advance Setting (Bit 2)
3	DA3	DAC Advance Setting (Bit 3)
4	DA4	DAC Advance Setting (Bit 4)
5	IBYP	Interpolator Bypass (0 = Bypass Disabled; 1 = Bypass Enabled)
6	DGTE	Digital Gain Tap Enable (0 = Disabled; 1 = Enabled)
7	—	Reserved (Program to 0)

Table XVIII. Control Register F Description

CONTROL REGISTER F

7	6	5	4	3	2	1	0
ALB/ AGTM	INV	SEEN/ AGTE	AGTC4	AGTC3	AGTC2	AGTC1	AGTC0

Bit	Name	Description
0	AGTC0	Analog Gain Tap Coefficient (Bit 0)
1	AGTC1	Analog Gain Tap Coefficient (Bit 1)
2	AGTC2	Analog Gain Tap Coefficient (Bit 2)
3	AGTC3	Analog Gain Tap Coefficient (Bit 3)
4	AGTC4	Analog Gain Tap Coefficient (Bit 4)
5	SEEN/	Single-Ended Enable (0 = Disabled; 1 = Enabled)
	AGTE	Analog Gain Tap Enable (0 = Disabled; 1 = Enabled)
6	INV	Input Invert (0 = Disabled; 1 = Enabled)
7	ALB/	Analog Loopback of Output to Input (0 = Disabled; 1 = Enabled)
	AGTM	Analog Gain Tap Mute (0 = Off; 1 = Muted)

Table XIX. Control Register G Description

CONTROL REGISTER G

7	6	5	4	3	2	1	0
DGTC7	DGTC6	DGTC5	DGTC4	DGTC3	DGTC2	DGTC1	DGTC0

Bit	Name	Description
0	DGTC0	Digital Gain Tap Coefficient (Bit 0)
1	DGTC1	Digital Gain Tap Coefficient (Bit 1)
2	DGTC2	Digital Gain Tap Coefficient (Bit 2)
3	DGTC3	Digital Gain Tap Coefficient (Bit 3)
4	DGTC4	Digital Gain Tap Coefficient (Bit 4)
5	DGTC5	Digital Gain Tap Coefficient (Bit 5)
6	DGTC6	Digital Gain Tap Coefficient (Bit 6)
7	DGTC7	Digital Gain Tap Coefficient (Bit 7)

Table XX. Control Register H Description

CONTROL REGISTER H

7	6	5	4	3	2	1	0
DGTC15	DGTC14	DGTC13	DGTC12	DGTC11	DGTC10	DGTC9	DGTC8

Bit	Name	Description
0	DGTC8	Digital Gain Tap Coefficient (Bit 8)
1	DGTC9	Digital Gain Tap Coefficient (Bit 9)
2	DGTC10	Digital Gain Tap Coefficient (Bit 10)
3	DGTC11	Digital Gain Tap Coefficient (Bit 11)
4	DGTC12	Digital Gain Tap Coefficient (Bit 12)
5	DGTC13	Digital Gain Tap Coefficient (Bit 13)
6	DGTC14	Digital Gain Tap Coefficient (Bit 14)
7	DGTC15	Digital Gain Tap Coefficient (Bit 15)

OPERATION

Resetting the AD73322L

The $\overline{\text{RESET}}$ pin resets all the control registers. All registers are reset to zero, indicating that the default SCLK rate (DMCLK/8) and sample rate (DMCLK/2048) are at a minimum to ensure that slow speed DSP engines can communicate effectively. As well as resetting the control registers using the $\overline{\text{RESET}}$ pin, the device can be reset using the RESET bit (CRA:7) in Control Register A. Both hardware and software resets require four DMCLK cycles. On reset, DATA/$\overline{\text{PGM}}$ (CRA:0) is set to 0 (default condition) thus enabling Program Mode. The reset conditions ensure that the device must be programmed to the correct settings after power-up or reset. Following a reset, the SDOFS will be asserted 2048 DMCLK cycles after $\overline{\text{RESET}}$ going high. The data that is output following reset and during Program Mode is random and contains no valid information until either data or mixed mode is set.

Power Management

The individual functional blocks of the AD73322L can be enabled separately by programming the power control register CRC. It allows certain sections to be powered down if not required, which adds to the device's flexibility in that the user need not incur the penalty of having to provide power for a certain section if it is not necessary to their design. The power control registers provide individual control settings for the major functional blocks on each codec unit and also a global override that allows all sections to be powered up by setting the bit. Using this method the user could, for example, individually enable a certain section, such as the reference (CRC:5), and disable all others. The global power-up (CRC:0) can be used to enable all sections, but if power-down is required using the global control, the reference will still be enabled, in this case, because its individual bit is set. Refer to Table XVI for details of the settings of CRC.

NOTE: As both codec units share a common reference, the reference control bits (CRC:5-7) in each SPORT are wire ORed to allow either device to control the reference.

Operating Modes

There are three main modes of operation available on the AD73322L; Program, Data and Mixed Program/Data modes. Two other operating modes are typically reserved as diagnostic modes: Digital and SPORT Loop-Back. The device configuration—register settings—can be changed only in Program and Mixed Program/Data Modes. In all modes, transfers of information to or from the device occur in 16-bit packets, therefore the DSP engine's SPORT will be programmed for 16-bit transfers.

Program (Control) Mode

In Program Mode, CRA:0 = 0, the user writes to the control registers to set up the device for desired operation—SPORT operation, cascade length, power management, input/output gain, etc. In this mode, the 16-bit information packet sent to the device by the DSP engine is interpreted as a control word whose format is shown in Table XII. In this mode, the user must address the device to be programmed using the address field of the control word. This field is read by the device and if it is zero (000 bin), the device recognizes the word as being addressed to it. If the address field is not zero, it is then decremented and the control word is passed out of the device—either to the next device in a cascade or back to the DSP engine. This 3-bit address format allows the user to uniquely address any one of up to eight devices in a cascade; please note that this addressing scheme is valid only in sending control information to the device —a different format is used to send DAC data to the device(s). As the AD73322L is a dual codec, it features two separate device addresses for programming purposes. If the AD73322L is used in a standalone configuration connected to a DSP, the two device addresses correspond to 0 and 1. If, on the other hand, the AD73322L is configured in a cascade of multiple, dual or single codecs (AD73322L or AD73311), its device addresses correspond with its hardwired position in the cascade.

Following reset, when the SE pin is enabled, the codec responds by raising the SDOFS pin to indicate that an output sample event has occurred. Control words can be written to the device to coincide with the data being sent out of the SPORT, as shown in Figure 11, or they can lag the output words by a time interval that should not exceed the sample interval. After reset, output frame sync pulses will occur at a slower default sample rate, which is DMCLK/2048, until Control Register B is programmed, after which the SDOFS pulses will be set according to the contents of DIR0-1. This is to allow slow controller devices to establish communication with the AD73322L. During Program Mode, the data output by the device is random and should not be interpreted as ADC data.

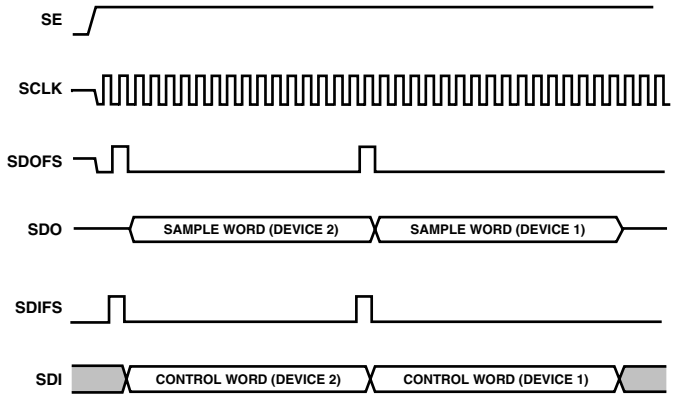


Figure 11. Interface Signal Timing for Control Mode Operation

Data Mode

Once the device has been configured by programming the correct settings to the various control registers, the device may exit Program Mode and enter Data Mode. This is done by programming the DATA/$\overline{\text{PGM}}$ (CRA:0) bit to a 1 and MM (CRA:1) to 0. Once the device is in Data Mode, the 16-bit input data frame is now interpreted as DAC data rather than a control frame. This data is therefore loaded directly to the DAC register. In Data Mode, see Figure 12, as the entire input data frame contains DAC data, the device relies on counting the number of input frame syncs received at the SDIFS pin. When that number equals the device count stored in the device count field of CRA, the device knows that the present data frame being received is its own DAC update data. When the device is in normal Data Mode (i.e., mixed mode disabled), it must receive a hardware reset to reprogram any of the control register settings.

In a single AD73322L configuration, each 16-bit data frame sent from the DSP to the device is interpreted as DAC data, but it is necessary to send two DAC words per sample period in order to ensure DAC update. Also, as the device count setting defaults to 1, it must be set to 2 (001b) to ensure correct update of both DACs on the AD73322L.

Appendix B details the initialization and operation of an AD73322L in normal Data Mode.

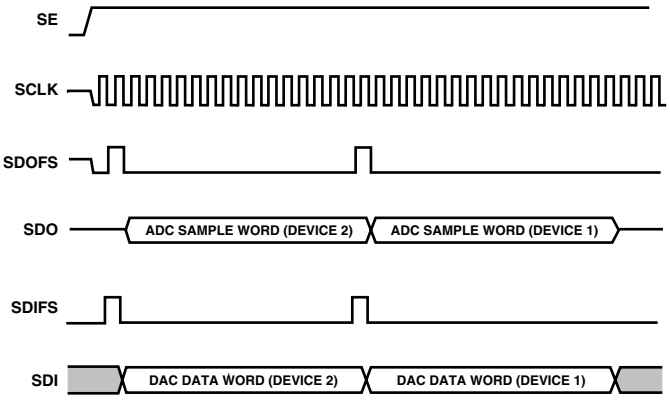


Figure 12. Interface Signal Timing for Data Mode Operation

Mixed Program/Data Mode

This mode allows the user to send control words to the device along with the DAC data. This permits adaptive control of the device whereby control of the input/output gains etc., can be affected by interleaving control words along with the normal flow of DAC data. The standard data frame remains 16 bits, but now the MSB is used as a flag bit to indicate whether the remaining 15 bits of the frame represent DAC data or control information. In the case of DAC data, the 15 bits are loaded with MSB justification and LSB set to 0 to the DAC register. Mixed mode is enabled by setting the MM bit (CRA:1) to 1 and the DATA/$\overline{\text{PGM}}$ bit (CRA:0) to 1. In the case where control setting changes will be required during normal operation, this mode allows the ability to load both control and data information with the slight inconvenience of formatting the data. Note that the output samples from the ADC will also have the MSB set to zero to indicate it is a data word.

Appendix C details the initialization and operation of an AD73322L operating in mixed mode. Note that it is not essential to load the control registers in Program Mode before setting mixed mode active. It is also possible to initiate mixed mode by programming CRA with the first control word and then interleaving control words with DAC data.

Digital Loop-Back

This mode can be used for diagnostic purposes and allows the user to feed the ADC samples from the ADC register directly to the DAC register. This forms a loop-back of the analog input to the analog output by reconstructing the encoded signal using the decoder channel. The serial interface will continue to work, which allows the user to control gain settings, etc. Only when DLB is enabled with mixed mode operation can the user disable the DLB, otherwise the device must be reset.

SPORT Loop-Back

This mode allows the user to verify the DSP interfacing and connection by writing words to the SPORT of the devices and have them returned back unchanged after a delay of 16 SCLK cycles. The frame sync and data word that are sent to the device are returned via the output port. Again, SLB mode can only be disabled when used in conjunction with mixed mode, otherwise the device must be reset.

Analog Loop-Back

In Analog Loop-Back mode, the differential DAC output is connected, via a loop-back switch, to the ADC input (see Figure 13). This mode allows the ADC channel to check functionality of the DAC channel as the reconstructed output signal can be monitored using the ADC as a sampler. Analog Loop-Back is enabled by setting the ALB bit (CRF:7).

NOTE: Analog Loop-Back can only be enabled if the Analog Gain Tap is powered down (CRC:1 = 0).

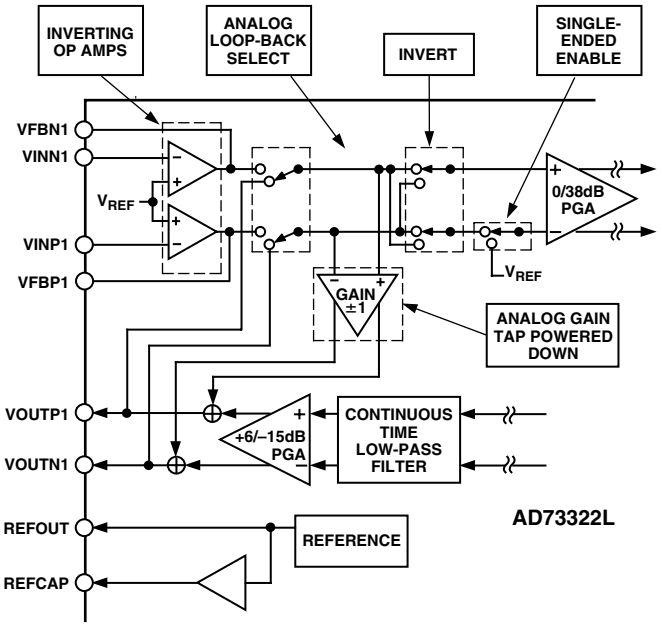


Figure 13. Analog Loop-Back Connectivity

INTERFACING

The AD73322L can be interfaced to most modern DSP engines using conventional serial port connections and an extra enable control line. Both serial input and output data use an accompanying frame synchronization signal that is active high one clock cycle before the start of the 16-bit word or during the last bit of the previous word if transmission is continuous. The serial clock (SCLK) is an output from the codec and is used to define the serial transfer rate to the DSP's Tx and Rx ports. Two primary configurations can be used: the first is shown in Figure 14 where the DSP's Tx data, Tx frame sync, Rx data and Rx frame sync are connected to the codec's SDI, SDIFS, SDO and SDOFS respectively. This configuration, referred to as indirectly coupled or nonframe sync loop-back, has the effect of decoupling the transmission of input data from the receipt of output data. The delay between receipt of codec output data and transmission of input data for the codec is determined by the DSP's software latency.

When programming the DSP serial port for this configuration, it is necessary to set the Rx FS as an input and the Tx FS as an output generated by the DSP. This configuration is most useful when operating in mixed mode, as the DSP has the ability to decide how many words (either DAC or control) can be sent to the codecs. This means that full control can be implemented over the device configuration as well as updating the DAC in a given sample interval.

The second configuration (shown in Figure 15) has the DSP's Tx data and Rx data connected to the codec's SDI and SDO, respectively, while the DSP's Tx and Rx frame syncs are connected to the codec's SDIFS and SDOFS. In this configuration, referred to as directly coupled or frame sync loop-back, the frame sync signals are connected together and the input data to the codec is forced to be synchronous with the output data from the codec. The DSP must be programmed so that both the Tx FS and Rx FS are inputs as the codec SDOFS will be input to both. This configuration guarantees that input and output events occur simultaneously and is the simplest configuration for operation in normal Data Mode. Note that when programming the DSP in this configuration it is advisable to preload the Tx register with the first control word to be sent before the codec is taken out of reset. This ensures that this word will be transmitted to coincide with the first output word from the device(s).

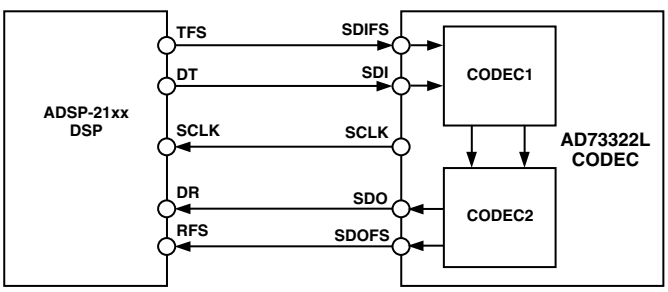


Figure 14. Indirectly Coupled or Nonframe Sync Loop-Back Configuration

Cascade Operation

The AD73322L has been designed to support cascading of codecs from a single DSP serial port (see Figure 27). Cascaded operation can support mixes of dual or single channel devices with the maximum number of codec units being eight (the AD73322L is equivalent to two codec units). The SPORT interface protocol has been designed so that device addressing is built into the packet of information sent to the device. This allows the cascade to be formed with no extra hardware overhead for control signals or addressing. A cascade can be formed in either of the two modes previously discussed.

There may be some restrictions in cascade operation due to the number of devices configured in the cascade and the sampling rate and serial clock rate chosen. The following relationship details the restrictions in configuring a codec cascade.

Number of Codecs × *Word Size (16)* × *Sampling Rate* <= *Serial Clock Rate*

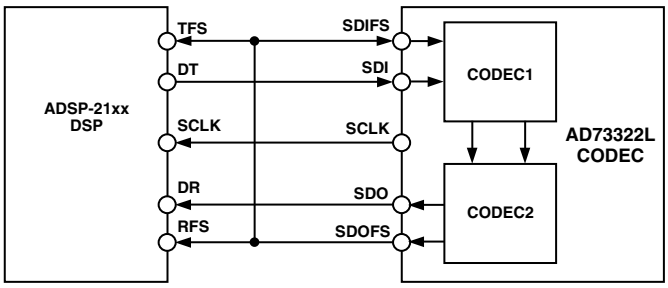


Figure 15. Directly Coupled or Frame Sync Loop-Back Configuration

When using the indirectly coupled frame sync configuration in cascaded operation, it is necessary to be aware of the restrictions in sending data to all devices in the cascade. Effectively the time allowed is given by the sampling interval (M/DMCLK—where *M* can be one of 256, 512, 1024 or 2048), which is 125 µs for a sample rate of 8 kHz. In this interval, the DSP must transfer N × 16 bits of information where *N* is the number of devices in the cascade. Each bit will take 1/SCLK and, allowing for any latency between the receipt of the Rx interrupt and the transmission of the Tx data, the relationship for successful operation is given by:

$$M/DMCLK > ((N \times 16/SCLK) + T_{INTERRUPT\ LATENCY})$$

The interrupt latency will include the time between the ADC sampling event and the Rx interrupt being generated in the DSP—this should be 16 SCLK cycles.

As the AD73322L is configured in cascade mode, each device must know the number of devices in the cascade because the data and mixed modes use a method of counting input frame sync pulses to decide when they should update the DAC register from the serial input register. Control Register A contains a 3-bit field (DC0-2) that is programmed by the DSP during the programming phase. The default condition is that the field contains 000b, which is equivalent to a single device in cascade (see Table XXI). However, for cascade operation this field must contain a binary value that is one less than the number of devices in the cascade, which is 001b for a single AD73322L device configuration.

Table XXI. Device Count Settings

DC2	DC1	DC0	Cascade Length
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

PERFORMANCE

As the AD73322L is designed to provide high performance, low cost conversion, it is important to understand the means by which this high performance can be achieved in a typical application. This section will, by means of spectral graphs, outline the typical performance of the device and highlight some of the options available to users in achieving their desired sample rate, either directly in the device or by doing some post-processing in the DSP, while also showing the advantages and disadvantages of the different approaches.

Encoder Section

The AD73322L offers a variable sampling rate from a fixed MCLK frequency—with 64 kHz, 32 kHz, 16 kHz and 8 kHz being available with a 16.384 MHz external clock. Each of these sampling rates preserves the same sampling rate in the ADC's sigma-delta modulator, which ensures that the noise performance is optimized in each case. The examples below will show the performance of a 1 kHz sine wave when converted at the various sample rates.

The range of sampling rates is aimed to offer the user a degree of flexibility in deciding how their analog front end is to be implemented. The high sample rates of 64 kHz and 32 kHz are suited to those applications, such as active control, where low conversion group delay is essential. On the other hand, the lower sample rates of 16 kHz and 8 kHz are better suited for applications such as telephony, where the lower sample rates result in lower DSP overhead.

Figure 20 shows the spectrum of the 1 kHz test tone sampled at 64 kHz. The plot shows the characteristic shaped noise floor of a sigma-delta converter, which is initially flat in the band of interest but then rises with increasing frequency. If a suitable digital filter is applied to this spectrum, it is possible to eliminate the noise floor in the higher frequencies. This signal can then be used in DSP algorithms or can be further processed in a decimation algorithm to reduce the effective sample rate. Figure 17 shows the resulting spectrum following the filtering and decimation of the spectrum of Figure 16 from 64 kHz to an 8 kHz rate.

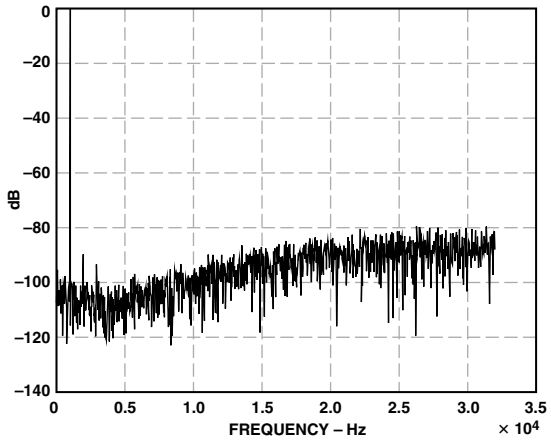


Figure 16. FFT (ADC 64 kHz Sampling)

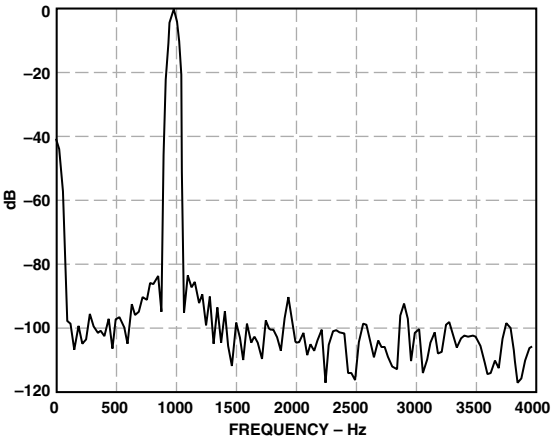


Figure 17. FFT (ADC 8 kHz Filtered and Decimated from 64 kHz)

The AD73322L also features direct sampling at the lower rate of 8 kHz. This is achieved by the use of extended decimation registers within the decimator block, which allows for the increased word growth associated with the higher effective oversampling ratio. Figure 18 details the spectrum of a 1 kHz test tone converted at an 8 kHz rate.

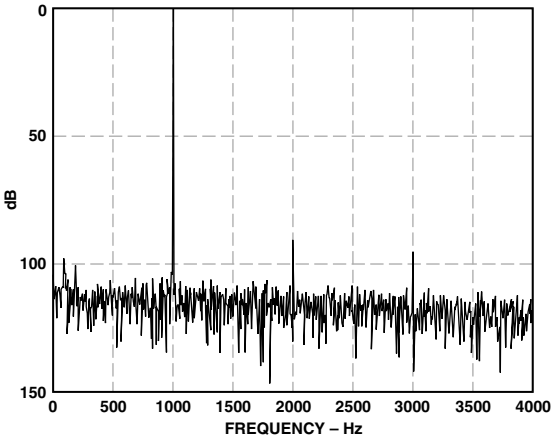


Figure 18. FFT (ADC 8 kHz Direct Sampling)

The device features an on-chip master clock divider circuit that allows the sample rate to be reduced as the sampling rate of the sigma-delta converter is proportional to the output of the MCLK Divider (whose default state is divide-by-one).

The decimator's frequency response (Sinc3) gives some pass-band attenuation (up to $F_S/2$) which continues to roll off above the Nyquist frequency. If it is required to implement a digital filter to create a sharper cutoff characteristic, it may be prudent to use an initial sample rate of greater than twice the Nyquist rate in order to avoid aliasing due to the smooth roll-off of the Sinc3 filter response.

In the case of voiceband processing where 4 kHz represents the Nyquist frequency, if the signal to be measured were externally bandlimited then an 8 kHz sampling rate would suffice. However if it is required to limit the bandwidth using a digital filter, then it may be more appropriate to use an initial sampling rate of 16 kHz and to process this sample stream with a filtering and decimating algorithm to achieve a 4 kHz bandlimited signal at an 8 kHz rate. Figure 19 details the initial 16 kHz sampled tone.

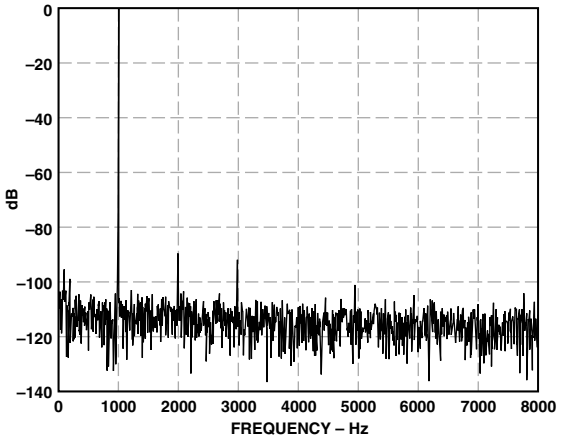


Figure 19. FFT (ADC 16 kHz Direct Sampling)

Figure 20 details the spectrum of the final 8 kHz sampled filtered tone.

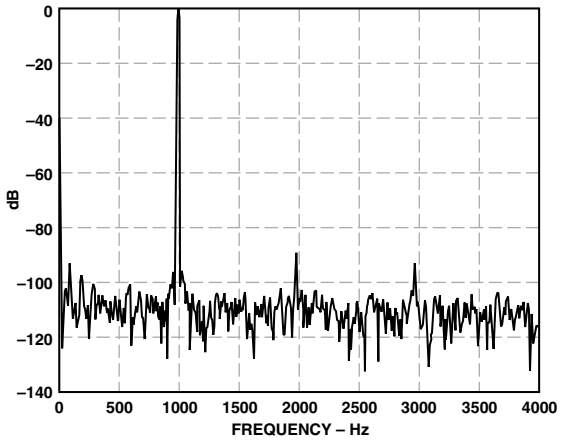


Figure 20. FFT (ADC 8 kHz Filtered and Decimated from 16 kHz)

Encoder Group Delay

When programmed for high sampling rates, the AD73322L offers a very low level of group delay, which is given by the following relationship:

$$Group\ Delay\ (Decimator) = Order \times ((M - 1)/2) \times T_{DEC}$$

where:

Order is the order of the decimator (= 3),

M is the decimation factor (= 32 @ 64 kHz, = 64 @ 32 kHz, = 128 @ 16 kHz , = 256 @ 8 kHz) and

T_{DEC} is the decimation sample interval (= 1/2.048e6) (based on DMCLK = 16.384 MHz) => Group Delay (Decimator @ 64 kHz) = $3 \times (32 - 1)/2 \times (1/2.048e6) = 22.7\ \mu s$

If final filtering is implemented in the DSP, the final filter's group delay must be taken into account when calculating overall group delay.

Decoder Section

The decoder section updates (samples) at the same rate as the encoder section. This rate is programmable as 64 kHz, 32 kHz, 16 kHz or 8 kHz (from a 16.384 MHz MCLK). The decoder section represents a reverse of the process that was described in the encoder section. In the case of the decoder section, signals are applied in the form of samples at an initial low rate. This sample rate is then increased to the final digital sigma-delta modulator rate of DMCLK/8 by interpolating new samples between the original samples. The interpolating filter also has the action of canceling images due to the interpolation process using spectral nulls that exist at integer multiples of the initial sampling rate. Figure 21 shows the spectral response of the decoder section sampling at 64 kHz. Again, its sigma-delta modulator shapes the noise so it is reduced in the voice bandwidth dc–4 kHz. For improved voiceband SNR, the user can implement an initial anti-imaging filter, preceded by 8 kHz to 64 kHz interpolation, in the DSP.

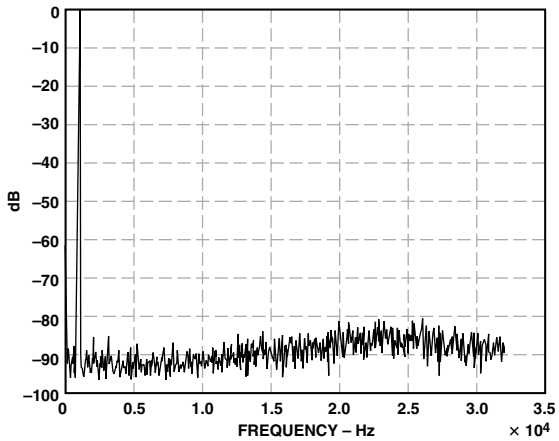


Figure 21. FFT (DAC 64 kHz Sampling)

As the AD73322L can be operated at 8 kHz (see Figure 22) or 16 kHz sampling rates, which make it particularly suited for voiceband processing, it is important to understand the action of the interpolator's Sinc3 response. As was the case with the encoder section, if the output signal's frequency response is not bounded by the Nyquist frequency, it may be necessary to perform some initial digital filtering to eliminate signal energy above Nyquist to ensure that it is not imaged at the integer multiples of the sampling frequency. If the user chooses to bypass the interpolator, perhaps to reduce group delay, images of the original signal will be generated at integer intervals of the sampling frequency. In this case these images must be removed by external analog filtering.

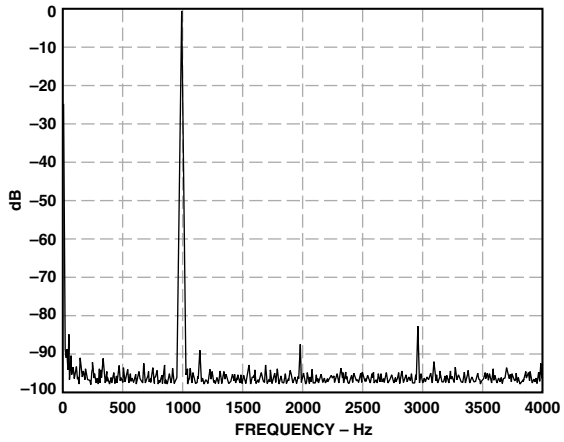


Figure 22. FFT (DAC 8 kHz Sampling)

Figure 23 shows the output spectrum of a 1 kHz tone being generated at an 8 kHz sampling rate with the interpolator bypassed.

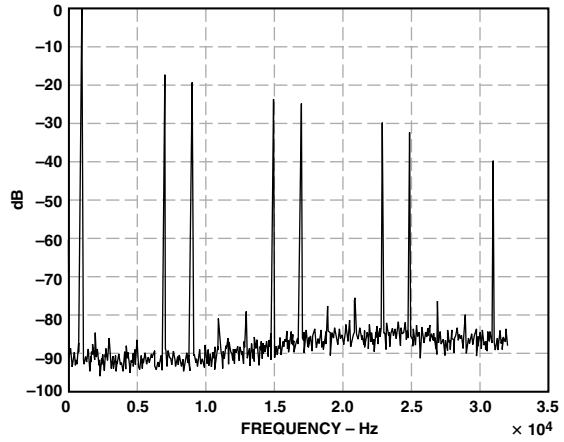


Figure 23. FFT (DAC 8 kHz Sampling—Interpolator Bypassed)

Decoder Group Delay

The interpolator roll-off is mainly due to its sinc-cubed function characteristic, which has an inherent group delay given by the equation:

$$Group\ Delay\ (Interpolator) = Order \times (L - 1)/2) \times T_{INT}$$

where:

Order is the interpolator order (= 3),

L is the interpolation factor (= 32 @ 64 kHz, = 64 @ 32 kHz, = 128 @ 16 kHz, = 256 @ 8 kHz) and

T_{INT} is the interpolation sample interval (= 1/2.048e6)

=> Group Delay (Interpolator @ 64 kHz)

= 3 × (32 – 1)/2 × (1/2.048e6)

= 22.7 µs

The analog section has a group delay of approximately 25 µs.

On-Chip Filtering

The primary function of the system filtering's sinc-cubed (Sinc3) response is to eliminate aliases or images of the ADCs or DAC's resampling, respectively. Both modulators are sampled at a nominal rate of DMCLK/8 (which is 2.048 MHz for a DMCLK of 16.384 MHz) and the simple, external RC antialias filter is sufficient to provide the required stopband rejection above the Nyquist frequency for this sample rate. In the case of the ADC section, the decimating filter is required to both decrease sample rate and increase sample resolution. The process of changing sample rate (resampling) leads to aliases of the original sampled waveform appearing at integer multiples of the new sample rate. These aliases would get mapped into the required signal passband without the application of some further antialias filtering. In the AD73322L, the sinc-cubed response of the decimating filter creates spectral nulls at integer multiples of the new sample rate. These nulls coincide with the aliases of the original waveform which were created by the down-sampling process, therefore reducing or eliminating the aliasing due to sample rate reduction.

In the DAC section, increasing the sampling rate by interpolation creates images of the original waveform at intervals of the original sampling frequency. These images may be sufficiently rejected by external circuitry but the sinc-cubed filter in the interpolator again nulls the output spectrum at integer intervals of the original sampling rate which corresponds with the images due to the interpolation process.

The spectral response of a sinc-cubed filter shows the characteristic nulls at integer intervals of the sampling frequency. Its passband characteristic (up to Nyquist frequency) features a roll-off that continues up to the sampling frequency, where the first null occurs. In many applications this smooth response will not give sufficient attenuation of frequencies outside the band of interest; therefore, it may be necessary to implement a final filter in the DSP which will equalize the passband roll-off and provide a sharper transition band and greater stopband attenuation.

DESIGN CONSIDERATIONS

The AD73322L features both differential inputs and outputs on each channel to provide optimal performance and avoid common mode noise. It is also possible to interface either inputs or outputs in single-ended mode. This section details the choice of input and output configurations and also gives some tips towards successful configuration of the analog interface sections.

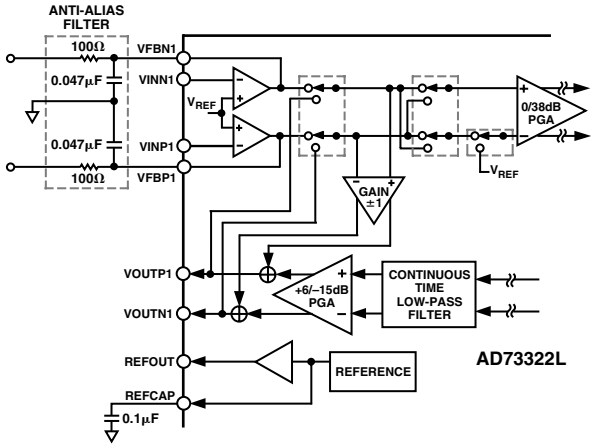


Figure 24. Analog Input (DC-Coupled)

Analog Inputs

There are several different ways in which the analog input (encoder) section of the AD73322L can be interfaced to external circuitry. It provides optional input amplifiers which allows sources with high source impedance to drive the ADC section correctly. When the input amplifiers are enabled, the input channel is configured as a differential pair of inverting amplifiers referenced to the internal reference (REFCAP) level. The inverting terminals of the input amplifier pair are designated as pins VINP1 and VINN1 for Channel 1 (VINP2 and VINN2 for Channel 2) and the amplifier feedback connections are available on pins VFBP1 and VFBN1 for Channel 1 (VFBP2 and VFBN2 for Channel 2).

For applications where external signal buffering is required, the input amplifiers can be bypassed and the ADC driven directly. When the input amplifiers are disabled, the sigma-delta modulator's input section (SC PGA) is accessed directly through the VFBP1 and VFBN1 pins for Channel 1 (VFBP2 and VFBN2 for Channel 2).

It is also possible to drive the ADCs in either differential or single-ended modes. If the single-ended mode is chosen it is possible using software control to multiplex between two single-ended inputs connected to the positive and negative input pins.

The primary concerns in interfacing to the ADC are first to provide adequate antialias filtering and to ensure that the signal source will drive the switched-capacitor input of the ADC correctly. The sigma-delta design of the ADC and its over sampling characteristics simplify the antialias requirements but it must be remembered that the single pole RC filter is primarily intended to eliminate aliasing of frequencies above the Nyquist frequency of the sigma-delta modulator's sampling rate (typically 2.048 MHz). It may still require a more specific digital filter implementation in the DSP to provide the final signal frequency response characteristics. It is recommended that for optimum performance that the capacitors used for the antialiasing filter be of high quality dielectric (NPO). The second issue mentioned above is interfacing the signal source to the ADC's switched capacitor input load. The SC input presents a complex dynamic load to a signal source, therefore, it is important to understand that the slew rate characteristic is an important consideration when choosing external buffers for use with the AD73322L. The internal inverting op amps on the AD73322L are specifically designed to interface to the ADC's SC input stage.

The AD73322L's on-chip 38 dB preamplifier can be enabled when there is not enough gain in the input circuit; the preamplifier is configured by bits IGS0-2 of CRD. The total gain must be configured to ensure that a full-scale input signal produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed the maximum input range.

The dc biasing of the analog input signal is accomplished with an on-chip voltage reference. If the input signal is not biased at the internal reference level (via REFOUT), then it must be ac-coupled with external coupling capacitors. C_{IN} should be 0.1 μF or larger. The dc biasing of the input can then be accomplished using resistors to REFOUT as in Figures 27 and 28.

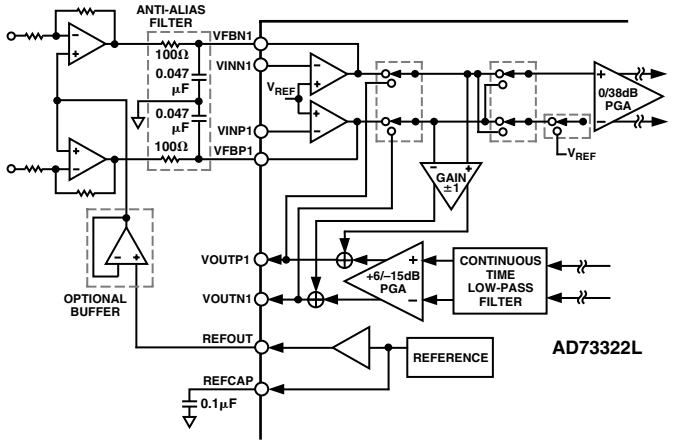


Figure 25. Analog Input (DC-Coupled) Using External Amplifiers

The AD73322L's ADC inputs are biased about the internal reference level (REFCAP level); therefore, it may be necessary to bias external signals to this level using the buffered REFOUT level as the reference. This is applicable in either dc- or ac-coupled configurations. In the case of dc coupling, the signal (biased to REFOUT) may be applied directly to the inputs (using amplifier bypass), as shown in Figure 24, or it may be conditioned in an external op amp where it can also be biased to the reference level using the buffered REFOUT signal, as shown in Figure 25, or it is possible to connect inputs directly to the AD73322L's input op amps as shown in Figure 26.

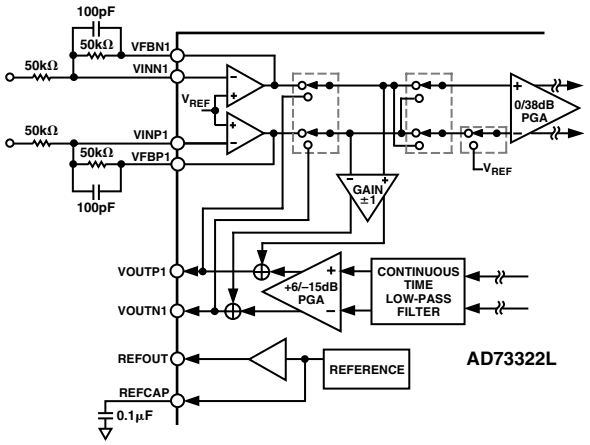


Figure 26. Analog Input (DC-Coupled) Using Internal Amplifiers

In the case of ac coupling, a capacitor is used to couple the signal to the input of the ADC. The ADC input must be biased to the internal reference (REFCAP) level which is done by connecting the input to the REFOUT pin through a 10 kΩ resistor as shown in Figure 27.

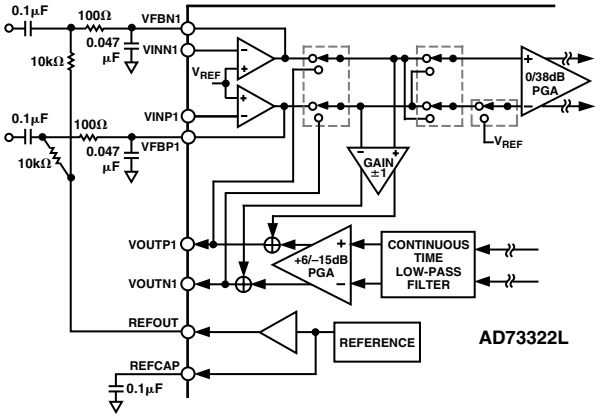


Figure 27. Analog Input (AC-Coupled) Differential

If the ADC is being connected in single-ended mode, the AD73322L should be programmed for single-ended mode using the SEEN and INV bits of CRF and the inputs connected as shown in Figure 28. When operated in single-ended input mode, the AD73322L can multiplex one of the two inputs to the ADC input.

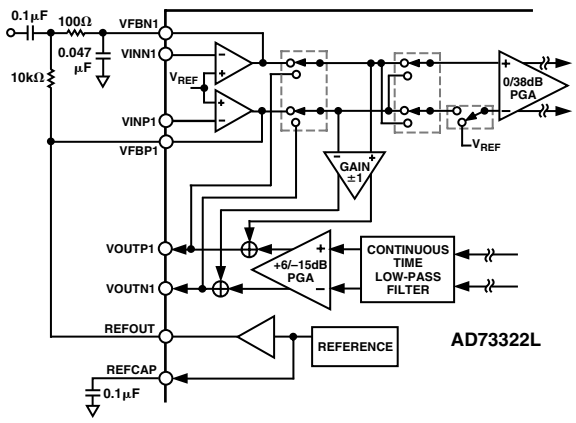


Figure 28. Analog Input (AC-Coupled) Single-Ended

If best performance is required from a single-ended source, it is possible to configure the AD73322L's input amplifiers as a single-ended to differential converter as shown in Figure 29.

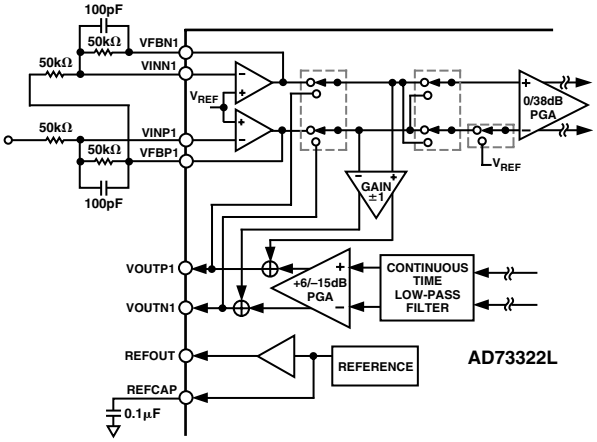


Figure 29. Single-Ended to Differential Conversion On Analog Input

Interfacing to an Electret Microphone

Figure 30 details an interface for an electret microphone which may be used in some voice applications. Electret microphones typically feature a FET amplifier whose output is accessed on the same lead which supplies power to the microphone; therefore this output signal must be capacitively coupled to remove the power supply (dc) component. In this circuit the AD73322L input channel is being used in single-ended mode where the internal inverting amplifier provides suitable gain to scale the input signal relative to the ADC's full-scale input range. The buffered internal reference level at REFOUT is used via an external buffer to provide power to the electret microphone. This provides a quiet, stable supply for the microphone. If this is not a concern, then the microphone can be powered from the system power supply.

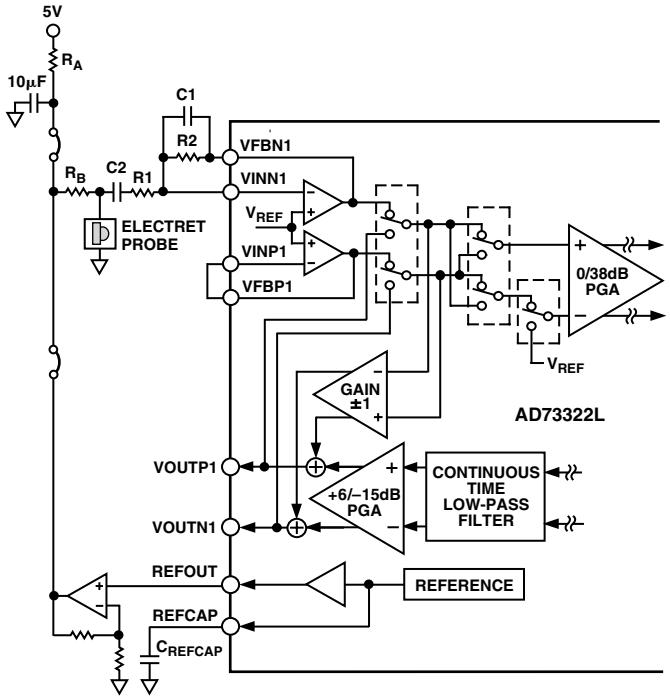


Figure 30. Electret Microphone Interface Circuit

Analog Output

The AD73322L's differential analog output (VOUT) is produced by an on-chip differential amplifier. The differential output can be ac-coupled or dc-coupled directly to a load which can be a headset or the input of an external amplifier (the specified minimum resistive load on the output section is 150 Ω.) It is possible to connect the outputs in either a differential or a single-ended configuration but please note that the effective maximum output voltage swing (peak to peak) is halved in the case of single-ended connection. Figure 31 shows a simple circuit providing a differential output with ac coupling. The capacitors in this circuit (C_{OUT}) are optional; if used, their value can be chosen as follows:

$$C_{OUT} = \frac{1}{2\pi f_C R_{LOAD}}$$

where f_C = desired cutoff frequency.

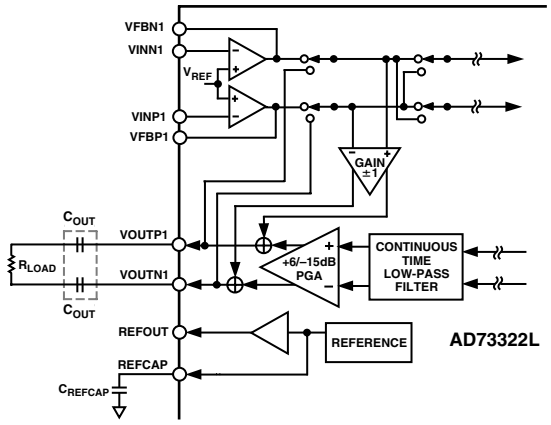


Figure 31. Example Circuit for Differential Output

Figure 32 shows an example circuit for providing a single-ended output with ac coupling. The capacitor of this circuit (C_{OUT}) is not optional if dc current drain is to be avoided.

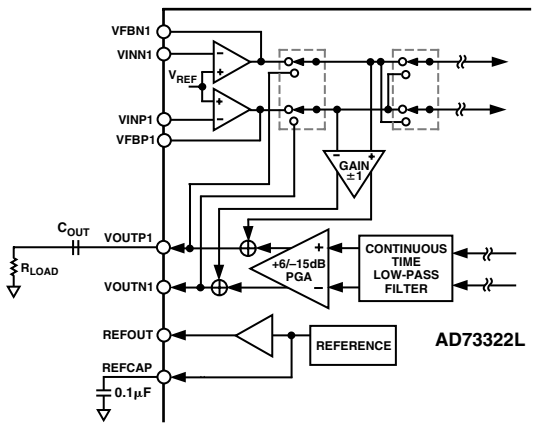


Figure 32. Example Circuit for Single-Ended Output

Differential to Single-Ended Output

In some applications it may be desirable to convert the full differential output of the decoder channel to a single-ended signal. The circuit of Figure 33 shows a scheme for doing this.

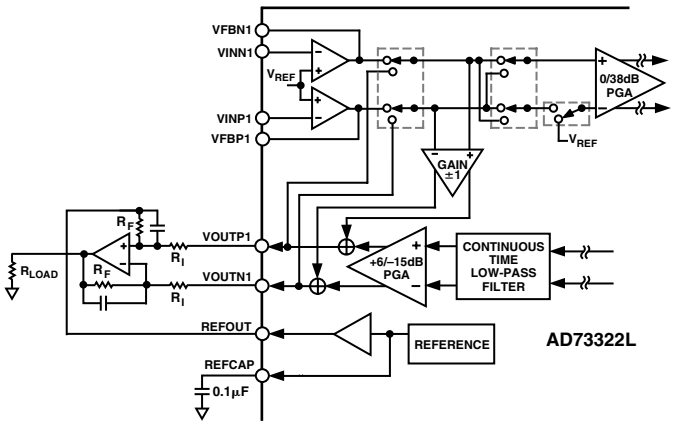


Figure 33. Example Circuit for Differential to Single-Ended Output Conversion

Digital Interfacing

The AD73322L is designed to easily interface to most common DSPs. The SCLK, SDO, SDOFS, SDI and SDIFS must be connected to the DSP's Serial Clock, Receive Data, Receive Data Frame Sync, Transmit Data and Transmit Data Frame Sync pins respectively. The SE pin may be controlled from a parallel output pin or flag pin such as FL0-2 on the ADSP-21xx (or XF on the TMS320C5x) or, where SPORT power-down is not required, it can be permanently strapped high using a suitable pull-up resistor. The $\overline{\text{RESET}}$ pin may be connected to the system hardware reset structure or it may also be controlled using a dedicated control line. In the event of tying it to the global system reset, it is advisable to operate the device in mixed mode, which allows a software reset, otherwise there is no convenient way of resetting the device. Figures 34 and 35 show typical connections to an ADSP-218x and TMS320C5x respectively.

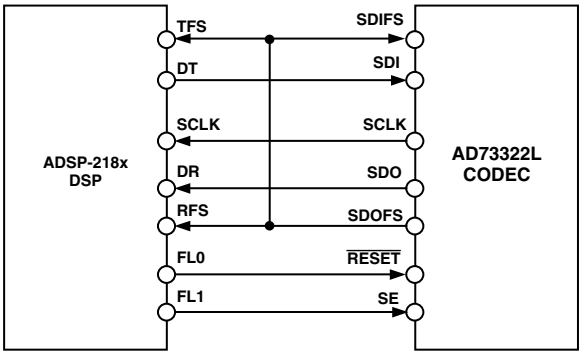


Figure 34. AD73322L Connected to ADSP-218x

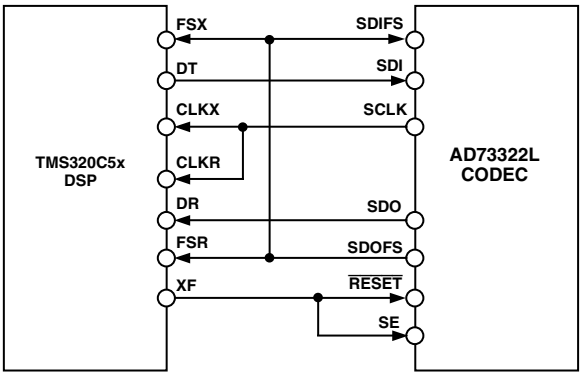


Figure 35. AD73322L Connected to TMS320C5x

Cascade Operation

Where it is required to configure a cascade of up to eight codecs (four AD73322L dual codecs), it is necessary to ensure that the timing of the SE and $\overline{\text{RESET}}$ signals is synchronized at each device in the cascade. A simple D type flip flop is sufficient to sync each signal to the master clock MCLK, as in Figure 36.

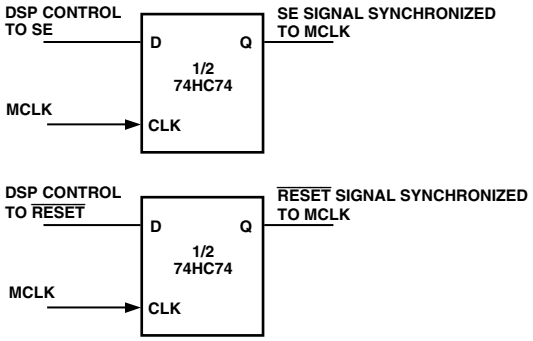


Figure 36. SE and $\overline{\text{RESET}}$ Sync Circuit for Cascaded Operation

Connection of a cascade of devices to a DSP, as shown in Figure 37, is no more complicated than connecting a single device. Instead of connecting the SDO and SDOFS to the DSP's Rx port, these are now daisy-chained to the SDI and SDIFS of the next device in the cascade. The SDO and SDOFS of the final device in the cascade are connected to the DSP's Rx port to complete the cascade. SE and $\overline{\text{RESET}}$ on all devices are fed from the signals that were synchronized with the MCLK using the circuit as described above. The SCLK from only one device need be connected to the DSP's SCLK input(s) as all devices will be running at the same SCLK frequency and phase.

Grounding and Layout

Since the analog inputs to the AD73322L are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part will remove common-mode noise on these inputs. The analog and digital supplies of the AD73322L are independent and separately pinned out to minimize coupling between analog and digital sections of the device. The digital filters on the encoder section will provide rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filters also remove noise from the analog inputs provided the noise source does not saturate the analog modulator. However, because the resolution of the AD73322L's ADC is high, and the noise levels from the AD73322L are so low, care must be taken with regard to grounding and layout.

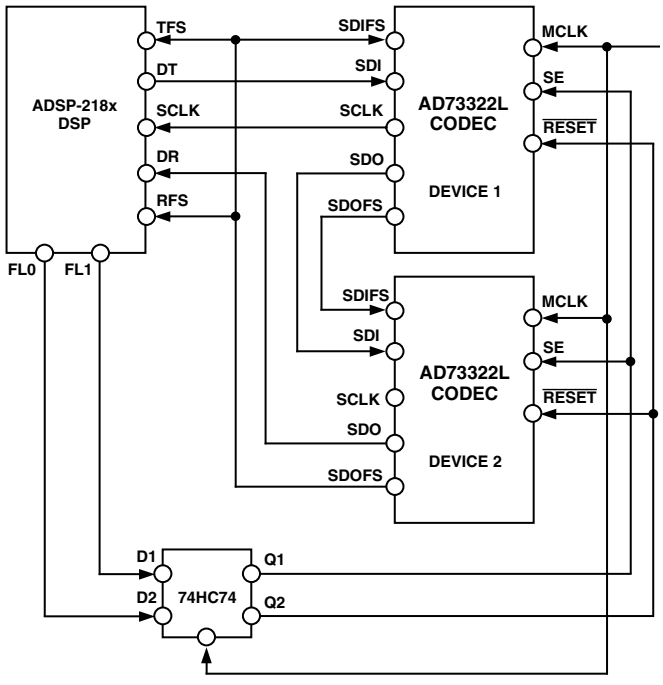


Figure 37. Connection of Two AD73322Ls Cascaded to ADSP-218x

The printed circuit board that houses the AD73322L should be designed so the analog and digital sections are separated and confined to certain sections of the board. The AD73322L pin configuration offers a major advantage in that its analog and digital interfaces are connected on opposite sides of the package. This facilitates the use of ground planes that can be easily separated, as shown in Figure 38. A minimum etch technique is generally best for ground planes as it gives the best shielding. Digital and analog ground planes should be joined in only one place. If this connection is close to the device, it is recommended to use a ferrite bead inductor as shown in Figure 38.

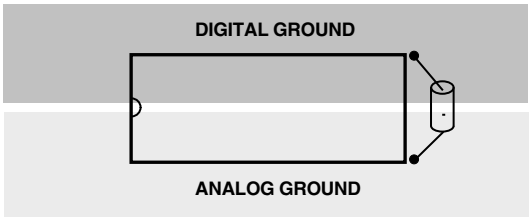


Figure 38. Ground Plane Layout

Avoid running digital lines under the device for they will couple noise onto the die. The analog ground plane should be allowed to run under the AD73322L to avoid noise coupling. The power supply lines to the AD73322L should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply lines. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other sections of the board, and clock signals should never be run near the analog inputs. Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the other side.

Good decoupling is important when using high speed devices. On the AD73322L both the reference (REFCAP) and supplies need to be decoupled. It is recommended that the decoupling capacitors used on both REFCAP and the supplies, be placed as close as possible to their respective pins to ensure high performance from the device. All analog and digital supplies should be decoupled to AGND and DGND respectively, with 0.1 µF ceramic capacitors in parallel with 10 µF tantalum capacitors. In systems where a common supply voltage is used to drive both the AVDD and DVDD of the AD73322L, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pins of the AD73322L and AGND and the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

DSP PROGRAMMING CONSIDERATIONS

This section discusses some aspects of how the serial port of the DSP should be configured and the implications of whether Rx and Tx interrupts should be enabled.

DSP SPORT Configuration

Following are the key settings of the DSP SPORT required for the successful operation with the AD73322L:

- Configure for External SCLK.
- Serial Word Length = 16 bits.
- Transmit and Receive Frame Syncs required with every word.
- Receive Frame Sync is an input to the DSP.
- Transmit Frame Sync is an:
  Input—in Frame Sync Loop-Back Mode
  Output—in Nonframe Sync Loop-Back Mode.
- Frame Syncs occur one SCLK cycle before the MSB of the serial word.
- Frame Syncs are active high.

DSP SPORT Interrupts

If SPORT interrupts are enabled, it is important to note that the active signals on the frame sync pins do not necessarily correspond with the positions in time of where SPORT interrupts are generated.

On ADSP-21xx processors, it is necessary to enable SPORT interrupts and use Interrupt Service Routines (ISRs) to handle Tx/Rx activity, while on the TMS320CSx processors it is possible to poll the status of the Rx and Tx registers, which means that Rx/Tx activity can be monitored using a single ISR that would ideally be the Tx ISR as the Tx interrupt will typically occur before the Rx ISR.

DSP SOFTWARE CONSIDERATIONS WHEN INTERFACING TO THE AD73322L

It is important when choosing the operating mode and hardware configuration of the AD73322L to be aware of their implications for DSP software operation. The user has the flexibility of choosing from either FSLB or NonFSLB when deciding on DSP to AFE connectivity. There is also a choice to be made between using autobuffering of input and output samples or simply choosing to accept them as individual interrupts. As most modern DSP engines support these modes, this appendix will attempt to discuss these topics in a generic DSP sense.

Operating Mode

The AD73322L supports two basic operating modes: Frame Sync Loop Back (FSLB) and NonFSLB (See Interfacing section). As described previously, FSLB has some limitations when used in Mixed Mode but is very suitable for use with the autobuffering feature that is offered on many modern DSPs. Autobuffering allows the user to specify the number of input or output words (samples) that are transferred before a specific Tx or Rx SPORT interrupt is generated. Given that the AD73322L outputs two sample words per sample period, it is possible using autobuffering to have the DSP's SPORT generate a single interrupt on receipt of the second of the two sample words. Additionally, both samples could be stored in a data buffer within the data memory store. This technique has the advantage of reducing the number of both Tx and Rx SPORT interrupts to a single one at each sample interval. The user also knows where each sample is stored. The alternative is to handle a larger number of SPORT interrupts (twice as many in the case of a single AD73322L) while also having some status flags to indicate where each new sample comes from (or is destined for).

Mixed-Mode Operation
To take full advantage of mixed-mode operation, it is necessary to configure the DSP/Codec interface in NonFSLB and to disable autobuffering. This allows a variable numbers of words to be sent to the AD73322L in each sample period—the extra words being control words that are typically used to update gain settings in adaptive control applications. The recommended sequence for updating control registers in mixed mode is to send the control word(s) first before the DAC update word.

It is possible to use mixed-mode operation when configured in FSLB, but it is necessary to replace the DAC update with a control word write in each sample period which may cause some discontinuity in the output signal due to a sample point being missed and the previous sample being repeated. This however may be acceptable in some cases as the effect may be masked by gain changes, etc.

Interrupts
The AD73322L transfers and receives information over the serial connection from the DSP's SPORT. This occurs following reset —during the initialization phase—and in both data-mode and mixed-mode. Each transfer of data to or from the DSP can cause a SPORT interrupt to occur. However even in FSLB configuration where serial transfers in and out of the DSP are synchronous, it is important to note that Tx and Rx interrupts do not occur at the same time due to the way that Tx and Rx interrupts are generated internally within the DSP's SPORT. This is especially important in time critical control loop applications where it may be necessary to use Rx interrupts only, as the relative positioning of the Tx interrupts relative to the Rx interrupts in a single sample interval are not suitable for quick update of new DAC positions.

Initialization
Following reset, the AD73322L is in its default condition which ensures that the device is in Control Mode and must be programmed or initialized from the DSP to start conversions. As communications between AD73322L and the DSP are interrupt driven, it is usually not practical to embed the initialization codes into the body of the initialization routine. It is more practical to put the sequence of initialization codes in a data (or program) memory buffer and to access this buffer with a pointer that is updated on each interrupt. If a circular buffer is used, it allows the interrupt routine to check when the circular buffer pointer has wrapped around—at which point the initialization sequence is complete.

In FSLB configurations, a single control word per codec per sample period is sent to the AD73322L whereas in NonFSLB, it is possible to initialize the device in a single sample period provide the SCLK rate is programmed to a high rate. It is also possible to use autobuffering in which case an interrupt is generated when the entire initialization sequence has been sent to the AD73322L.

Running the AD73322L with ADCs or DACs in Power-Down
The programmability of the AD73322L allows the user flexibility in choosing what sections of the AD73322L need be powered up. This allows better matching of the power consumption to the application requirements as the AD73322L offers two ADCs and two DACs in any combination. The AD73322L always interfaces to the DSP in a standard way regardless of what ADC or DAC sections are enabled or disabled. Therefore the DSP will expect to receive two ADC samples per sample period and to transmit two DAC samples per sample period. If a particular ADC is disabled (in power-down) then its sample value will be invalid. Likewise a sample sent to a DAC which is disabled will have no effect.

There are two distinct phases of operation of the AD73322L: initialization of the device via each codec section's control registers, and operation of the converter sections of each codec. The initialization phase involves programming the control registers of the AD73322L to ensure the required operating characteristics such as sampling rate, serial clock rate, I/O gain, etc. There are several ways in which the DSP can be programmed to initialize the AD73322L. These range from hard-coding a sequence of DSP SPORT Tx register writes with constants used for the initialization words, to putting the initialization sequence in a circular data buffer and using an autobuffered transmit sequence.

Hard-coding involves creating a sequence of writes to the DSP's SPORT Tx buffer which are separated by loops or instructions that idle and wait for the next Tx interrupt to occur as shown in the code below.

```
ax0     = b#1000100100000100;
tx0     = ax0;
idle; {wait for tx register to send current word}
```

The circular buffer approach can be useful if a long initialization sequence is required. The list of initialization words is put into the buffer in the required order:

```
.VAR/DM/RAM/CIRC   init_cmds[16];   {Codec init sequence}
.VAR/DM/RAM    stat_flag;
.INIT   init_cmds:
  b#1000100100000100,
  b#1000000100000100,
  b#1000101011111001,
  b#1000001011111001,
  b#1000101100000000,
  b#1000001100000000,
  b#1000110000000000,
  b#1000010000000000,
  b#1000110100000000,
  b#1000010100000000,
  b#1000111000000000,
  b#1000011000000000,
  b#1000111100000000,
  b#1000011100000000,
  b#1000100000010001,
  b#1000000000010001;
```

and the DSP program initializes pointers to the top of the buffer

```
i3 = ^init_cmds;          l3 = %init_cmds;
```

and puts the first entry in the DSP's transmit buffer so that it is available at the first SDOFS pulse.

```
ax0 = dm(i3,m1);
tx0 = ax0;
```

The DSP's transmit interrupt is enabled.

```
imask = b#0001000000;
```

At each occurrence of an SDOFS pulse, the DSP's transmit buffer contents are sent to the SDI pin of the AD73322L. This also causes a subsequent DSP Tx interrupt which transfers the initialization word, pointed to by the circular buffer pointer, to the Tx buffer. The buffer pointer is updated to point to the next unsent initialization word. When the circular buffer pointer wraps around, which happens after the last word has been accessed, it indicates that the initialization phase is complete. This can be done "manually" in the DSP using a simple address check, or auto-buffered mode can be used to complete the transfer automatically.

```
txcdat: ar = dm(stat_flag);
   ar = pass ar;
   if eq rti;
   ena sec_reg;
   ax0 = dm (i3, m1);
   tx0 = ax0;
   ax0 = i3;
   ay0 = ^init_cmds;
   ar = ax0 - ay0;
   if gt rti;
   ax0 = 0x00;
   dm (stat_flag) = ax0;
   rti;
```

In the main body of the program, the code loops waiting for the initialization sequence to be completed.

```
check_init:
   ax0 = dm (stat_flag);
   af = pass ax0;
   if ne jump check_init;
```

As the AD73322L is effectively a cascade of two codec units, it is important to observe some restrictions in the sequence of sending initialization words to the two codecs. It is preferable to send pairs of control words for the corresponding control registers in each codec, and it is essential to send the control word for codec 2 before that for codec 1. Control Registers A and B contain settings, such as sampling rate, serial clock rate, etc., which critically require synchronous update in both codecs.

Once the device has been initialized, Control Register A on both codecs is written with a control word which changes the operating mode from Program Mode to either data mode or Mixed Control Data Mode. The device count field which defaults to 000b will have to be programmed to 001b for a single AD73322L device. In data mode or mixed mode, the main function of the device is to return ADC samples from both codecs and to accept DAC words for both codecs. During each sample interval, two ADC samples will be returned from the device, while in the same interval two DAC update samples will be sent to the device. In order to reduce the number of interrupts and to reduce complexity, autobuffering can be used to ensure that only one interrupt is generated during each sampling interval.

APPENDIX A

DAC Timing Control Example

The AD73322L's DAC is loaded from the DAC register contents just before the ADC register contents are loaded to the serial register (SDOFS going high). This default DAC load position can be advanced in time to occur earlier with respect to the SDOFS going high. Figure 45 shows an example of the ADC unload and DAC load sequence. At time t_1 the SDOFS is raised to indicate that a new ADC word is ready. Following the SDOFS pulse, 16 bits of ADC data are clocked out on SDO in the subsequent 16 SCLK cycles finishing at time t_2 where the DSP's SPORT will have received the 16-bit word. The DSP may process this information and generate a DAC word to be sent to the AD73322L. Time t_3 marks the beginning of the sequence of sending the DAC word to the AD73322L. This sequence ends at time t_4 where the DAC register will be updated from the 16 bits in the AD73322L's serial register. However, the DAC will not be updated from the DAC register until time t_5, which may not be acceptable in certain applications. In order to reduce this delay and load the DAC at time t_6, the DAC advance register can be programmed with a suitable setting corresponding to the required time advance (refer to Table X for details of DAC Timing Control settings).

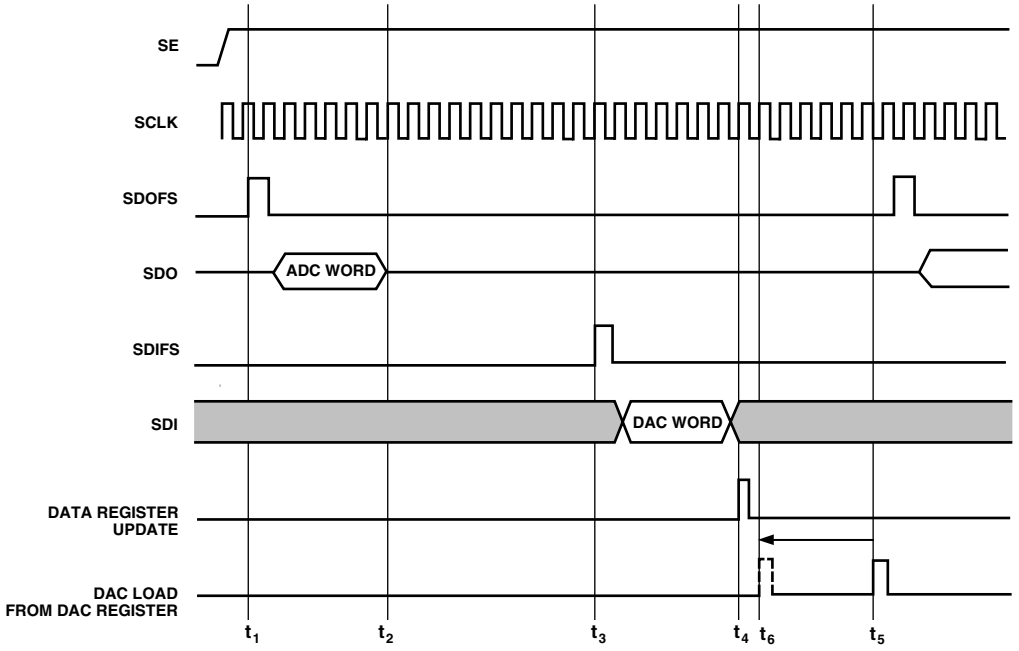


Figure 39. DAC Timing Control

APPENDIX B

Configuring an AD73322L to Operate in Data Mode[1]

This section describes the typical sequence of control words that are required to be sent to an AD73322L to set it up for data mode operation. In this sequence Registers B, C and A are programmed before the device enters data mode. This description panel refers to Table XXII.

At each sampling event, a pair of SDOFS pulses will be observed which will cause a pair of control (programming) words to be sent to the device from the DSP. It is advisable that each pair of control words should program a single register in each Channel. The sequence to be followed is Channel 2 followed by Channel 1.

In Step 1, we have the first output sample event following device reset. The SDOFS signal is raised on both channels[2] simultaneously, which prepares the DSP Rx register to accept the ADC word from Channel 2, while SDOFS from Channel 1 becomes an SDIFS to Channel 2. As the SDOFS of Channel 2 is coupled to the DSP's TFS and RFS, and to the SDIFS of Channel 1, this event also forces a new control word to be output from the DSP Tx register to Channel 1[3].

In Step 2, we observe the status of the channels following the transmission of the first control word. The DSP has received the output word from Channel 2, while Channel 2 has received the output word from Channel 1. Channel 1 has received the Control word destined for Channel 2. At this stage, the SDOFS of both channels are again raised because Channel 2 has received Channel 1's output word, and as it is not a valid control word addressed to Channel 2, it is passed on to the DSP. Likewise, Channel 1 has received a control word destined for Channel 2—address field is not zero—and it decrements the address field of the control word and passes it on.

Step 3 shows completion of the first series of control word writes. The DSP has now received both output words and each channel has received a control word that addresses control register B and sets the internal MCLK divider ratio to 1, SCLK rate to DMCLK/2 and sampling rate to DMCLK/256. Note that both channels are updated simultaneously as both receive the addressed control word at the same time. This is an important factor in cascaded operation as any latency between updating the SCLK or DMCLK of channels can result in corrupted operation. This will not happen in the case of an FSLB configuration as shown here, but must be taken into account in a non-FSLB configuration. One other important observation of this sequence is that the data words are received and transmitted in reverse order, i.e., the ADC words are received by the DSP, Channel 2 first, then Channel 1 and, similarly, the transmit words from the DSP are sent to Channel 2 first, then to Channel 1. This ensures that all channels are updated at the same time.

Steps 4–6 are similar to Steps 1–3, but instead, program Control Register C to power up the analog sections of the device (ADCs, DACs, and reference).

Steps 7–9 are similar to Steps 1–3, but instead, program Control Register A, with a device count field equal to two channels in cascade and sets the PGM/DATA bit to one to put the channel in data mode.

In Step 10, the programming phase is complete and we now begin actual channel data read and write. The words loaded into the serial registers of the two channels at the ADC sampling event now contain valid ADC data and the words written to the channels from the DSP's Tx register will now be interpreted as DAC words. The DSP Tx register contains the DAC word for Channel 2.

In Step 11, the first DAC word has been transmitted into the cascade and the ADC word from Channel 2 has been read from the cascade. The DSP Tx register now contains the DAC word for Channel 1. As the words being sent to the cascade are now being interpreted as 16-bit DAC words, the addressing scheme now changes from one where the address was embedded in the transmitted word, to one where the serial port now counts the SDIFS pulses. When the number of SDIFS pulses received equals the value in the channel count field of Control Register A, the length of the cascade—each channel updates its DAC register with the present word in its serial register. In Step 11 each channel has received only one SDIFS pulse; Channel 2 received one SDIFS from the SDOFS of Channel 1 when it sent its ADC word, and Channel 1 received one SDIFS pulse when it received the DAC word for Channel 2 from the DSP's Tx register. Therefore, each channel raises its SDOFS line to pass on the current word in its serial register, and each channel now receives another SDIFS pulse.

Step 12 shows the completion of an ADC read and DAC write cycle. Following Step 11, each channel has received two SDIFS pulses that equal the setting of the channel count field in Control Register A. The DAC register in each channel is now updated with the contents of the word that accompanied the SDIFS pulse that satisfied the channel count requirement. The internal frame sync counter is now reset to zero and will begin counting for the next DAC update cycle.

Steps 10–12 are repeated on each sampling event.

NOTES

[1]Channel 1 and Channel 2 of the description refer to the two AFE sections of the AD73322L device.

[2]The AD73322L is configured as two channels in cascade. The internal cascade connections between Channels 1 and 2 are detailed in Figure 14. The connections SDI/SDIFS are inputs to Channel 1 while SDO/SDOFS are outputs from Channel 2.

[3]This sequence assumes that the DSP SPORT's Rx and Tx interrupts are enabled. It is important to ensure that there is no latency (separation) between control words in a cascade configuration. This is especially the case when programming Control Registers A and B as they must be updated synchronously in each channel.

Table XXII. Data Mode Operation

Step	DSP Tx	AD73322L Channel 1	AD73322L Channel 2	DSP Rx
1	CRB–CH2 1000100100001011	OUTPUT CH1 0000000000000000	OUTPUT CH2 0000000000000000	DON'T CARE xxxxxxxxxxxxxxxx
2	CRB–CH1 1000000100001011	CRB–CH2 1000100100001011	OUTPUT CH1 0000000000000000	OUTPUT CH2 0000000000000000
3	CRC–CH2 1000101011111001	CRB–CH1 1000000100001011	CRB–CH2 1000000100001011	OUTPUT CH1 0000000000000000
4	CRC–CH2 1000101011111001	OUTPUT CH1 1000000100001011	OUTPUT CH2 1000000100001011	DON'T CARE xxxxxxxxxxxxxxxx
5	CRC–CH1 1000001011111001	CRC–CH2 1000101011111001	OUTPUT CH2 1011100100001011	OUTPUT CH2 1011100100001011
6	CRA–CH2 1000100000010001	CRC-CH1 1000001011111001	CRC–CH2 1000001011111001	OUTPUT CH1 1011000100001011
7	CRA–CH2 1000100000010001	OUTPUT CH1 1000001011111001	OUTPUT CH2 1000001011111001	DON'T CARE xxxxxxxxxxxxxxxx
8	CRA–CH1 1000000000010001	CRA-CH2 1000100000010001	OUTPUT CH2 1011101011111001	OUTPUT CH2 1011101011111001
9	CRB-CH2 0111111111111111	CRA-CH1 1000000000010001	CRA–CH2 1000000000010001	OUTPUT CH1 1011001011111001
10	DAC WORD CH 2 0111111111111111	ADC RESULT CH1 ????????????????	ADC RESULT CH2 ????????????????	DON'T CARE xxxxxxxxxxxxxxxx
11	DAC WORD CH 1 1000000000000000	DAC WORD CH 2 0111111111111111	ADC RESULT CH1 ????????????????	ADC RESULT CH2 ????????????????
12	DON'T CARE xxxxxxxxxxxxxxxx	DAC WORD CH 1 1000000000000000	DAC WORD CH 2 0111111111111111	ADC RESULT CH1 ????????????????

APPENDIX C

Configuring an AD73322L to Operate in Mixed Mode[1]

This section describes a typical sequence of control words that would be sent to an AD73322L to configure it for operation in mixed mode. It is not intended to be a definitive initialization sequence, but will show users the typical input/output events that occur in the programming and operation phases[2]. This description panel refers to Table XXIII.

Steps 1–5 detail the transfer of the control words to Control Register A, which programs the device for Mixed-Mode operation. In Step 1, we have the first output sample event following device reset. The SDOFS signal is simultaneously raised on both channels, which prepares the DSP Rx register to accept the ADC word from Channel 2 while SDOFS from Channel 1 becomes an SDIFS to Channel 2. The cascade is configured as nonFSLB, which means that the DSP has control over what is transmitted to the cascade[3] and in this case we will not transmit to the devices until both output words have been received from the AD73322L.

In Step 2, we observe the status of the channels following the reception of the Channel 2 output word. The DSP has received the ADC word from Channel 2, while Channel 2 has received the output word from Channel 1. At this stage, the SDOFS of Channel 2 is again raised because Channel 2 has received Channel 1's output word and, as it is not addressed to Channel 2, it is passed on to the DSP.

In Step 3 the DSP has now received both ADC words. Typically, an interrupt will be generated following reception of the two output words by the DSP (this involves programming the DSP to use autobuffered transfers of two words). The transmit register of the DSP is loaded with the control word destined for Channel 2. This generates a transmit frame-sync (TFS) that is input to the SDIFS input of the AD73322L to indicate the start of transmission.

In Step 4, Channel 1 now contains the Control Word destined for Channel 2. The address field is decremented, SDOFS1 is raised (internally) and the Control word is passed on to Channel 2. The Tx register of the DSP has now been updated with the Control Word destined for Channel 1 (this can be done using autobuffering of transmit or by handling transmit interrupts following each word sent).

In Step 5 each channel has received a control word that addresses Control Register A and sets the device count field equal to two channels and programs the channels into Mixed Mode—MM and $\overline{\text{PGM}}$/DATA set to one.

Following Step 5, the device has been programmed into mixed mode although none of the analog sections have been powered up (controlled by Control Register C). Steps 6–10 detail update of Control Register B in mixed mode. In Steps 6–8, the ADC samples, which are invalid as the ADC section is not yet powered up, are transferred to the DSP's Rx section. In the subsequent interrupt service routine the Tx register is loaded with the control word for Channel 2. In Steps 9–10, Channels 1 and 2 are loaded with a control word setting for Control Register B which programs DMCLK = MCLK, the sampling rate to DMCLK/256, SCLK = DMCLK/2.

Steps 11–17 are similar to Steps 6–12 except that Control Register C is programmed to power up all analog sections (ADC, DAC, Reference = 2.4 V, REFOUT). In Steps 16–17, DAC words are sent to the device—both DAC words are necessary as each channel will only update its DAC when the device has counted a number of SDIFS pulses, accompanied by DAC words (in mixed-mode, the MSB = 0), that is equal to the device count field of Control Register A[4]. As the channels are in mixed mode, the serial port interrogates the MSB of the 16-bit word sent to determine whether it contains DAC data or control information. DAC words should be sent in the sequence Channel 2 followed by Channel 1.

Steps 11–17 illustrate the implementation of Control Register update and DAC update in a single sample period. Note that this combination is not possible in the FSLB configuration[3].

Steps 18–25 illustrate a Control Register readback cycle. In Step 22, both channels have received a Control Word that addresses Control Register C for readback (Bit 14 of the Control Word = 1). When the channels receive the readback request, the register contents are loaded to the serial registers as shown in Step 23. SDOFS is raised in both channels, which causes these readback words to be shifted out toward the DSP. In Step 24, the DSP has received the Channel 2 readback word while Channel 2 has received the Channel 1 readback word (note that the address field in both words has been decremented to 111b). In Step 25, the DSP has received the Channel 1 readback word (its address field has been further decremented to 110b).

Steps 26–30 detail an ADC and DAC update cycle using the nonFSLB configuration. In this case no Control Register update is required.

NOTES

[1]Channel 1 and Channel 2 of the description refer to the two AFE sections of the AD73322L device.

[2]This sequence assumes that the DSP SPORT's Rx and Tx interrupts are enabled. It is important to ensure there is no latency (separation) between control words in a cascade configuration. This is especially the case when programming Control Registers A and B.

[3]Mixed-mode operation with the FSLB configuration is more restricted in that the number of words sent to the cascade equals the number of channels in the cascade, which means that DAC updates may need to be substituted with a register write or read. Using the FSLB configuration introduces a corruption of the ADC samples in the sample period following a Control Register write. This corruption is predictable and can be corrected in the DSP. The ADC word is treated as a Control Word and the Device Address field is decremented in each channel that it passes through before being returned to the DSP.

[4]In mixed mode, DAC update is done using the same SDIFS counting scheme as in normal data mode with the exception that only DAC words (MSB set to zero) are recognized as being able to increment the frame sync counters.

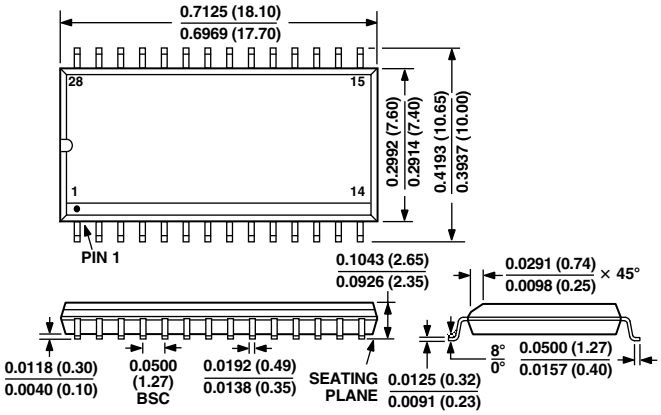
Table XXIII. Mixed Mode Operation

Step	DSP Tx	AD73322L Channel 1	AD73322L Channel 2	DSP Rx
	DON'T CARE	OUTPUT CH1	OUTPUT CH2	DON'T CARE
1	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	OUTPUT CH1	OUTPUT CH2
2	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRA-CH2	DON'T CARE	DON'T CARE	OUTPUT CH1
3	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRA-CH1	CRA-CH2	DON'T CARE	DON'T CARE
4	1000000000010011	1000100000010011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRA-CH1	CRA-CH2	DON'T CARE
5	xxxxxxxxxxxxxxxx	1000000000010011	1000000000010011	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
6	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
7	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRB-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
8	1000100100001011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRB-CH1	CRB-CH2	DON'T CARE	DON'T CARE
9	1000000100001011	1000100100001011	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRB-CH1	CRB-CH2	DON'T CARE
10	xxxxxxxxxxxxxxxx	1000000100001011	1000000100001011	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
11	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
12	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRC-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
13	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRC-CH1	CRC-CH2	DON'T CARE	DON'T CARE
14	1000001011111001	1000101011111001	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DAC WORD CH 2	CRC-CH1	CRC-CH2	DON'T CARE
15	0111111111111111	1000001011111001	1000001011111001	xxxxxxxxxxxxxxxx
	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE	DON'T CARE
16	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE
17	xxxxxxxxxxxxxxxx	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
18	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
19	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000	0000000000000000
	CRC-CH2	DON'T CARE	DON'T CARE	ADC RESULT CH1
20	11001010xxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	0000000000000000
	CRC-CH1	CRC-CH2	DON'T CARE	DON'T CARE
21	10000010xxxxxxxx	11001010xxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	CRC-CH1	CRC-CH2	DON'T CARE
22	xxxxxxxxxxxxxxxx	10000010xxxxxxxx	10000010xxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	READBACK CH 1	READBACK CH 2	DON'T CARE
23	xxxxxxxxxxxxxxxx	1100001011111001	1100001011111001	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	READBACK CH 1	READBACK CH 2
24	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	1111101011111001	1111101011111001
	DON'T CARE	DON'T CARE	DON'T CARE	READBACK CH 1
25	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	1111001011111001
	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2	DON'T CARE
26	xxxxxxxxxxxxxxxx	????????????????	????????????????	xxxxxxxxxxxxxxxx
	DON'T CARE	DON'T CARE	ADC RESULT CH1	ADC RESULT CH2
27	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	????????????????	????????????????
	DAC WORD CH 2	DON'T CARE	DON'T CARE	ADC RESULT CH1
28	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx	????????????????
	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE	DON'T CARE
29	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx	xxxxxxxxxxxxxxxx
	DON'T CARE	DAC WORD CH 1	DAC WORD CH 2	DON'T CARE
30	xxxxxxxxxxxxxxxx	1000000000000000	0111111111111111	xxxxxxxxxxxxxxxx

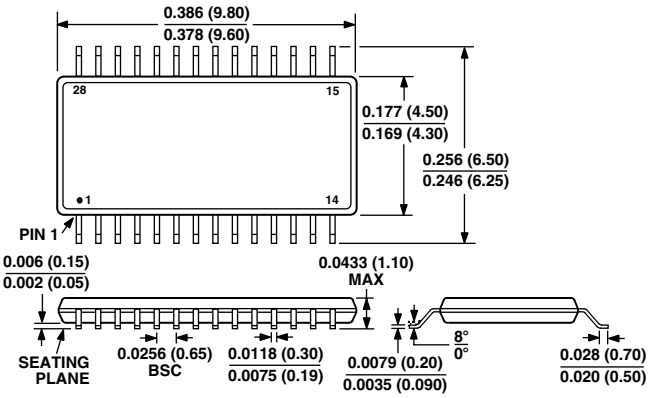
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

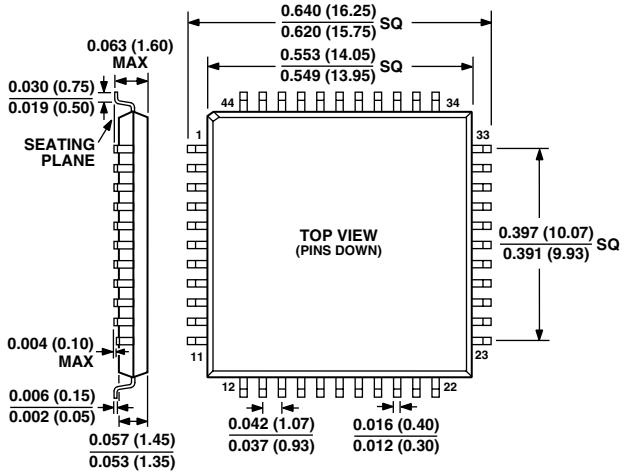
28-Lead Wide Body SOIC
(R-28)



28-Lead Thin Shrink SO (TSSOP)
(RU-28)



44-Lead Plastic Thin Quad Flatpack (LQFP)
(ST-44A)



C00691–2.5–4/01(0)

PRINTED IN U.S.A.