intersil

HGTD8P50G1, HGTD8P50G1S

March 1997

8A, 500V P-Channel IGBTs

Features

- 8A, 500V
- 3.7V $V_{CE(SAT)}$
- Typical Fall Time - 1800ns
- High Input Impedance
- T_J = +150°C

Description

The HGTD8P50G1 and the HGTD8P50G1S are P-channel enhancement-mode insulated gate bipolar transistors (IGBTs) designed for high voltage, low on-dissipation applications such as switching regulators and motor drives. This P- channel IGBT can be paired with N-Channel IGBTs to form a complementary power switch and it is ideal for half bridge circuit configurations. These types can be operated directly from low power integrated circuits.

PACKAGING AVAILABILITY

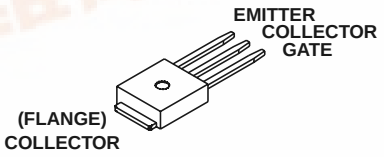
PART NUMBER	PACKAGE	BRAND
HGTD8P50G1	TO-251AA	G8P50G
HGTD8P50G1S	TO-252AA	G8P50G

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., HGTD8P50G1S9A.

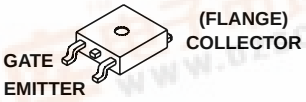
The development type number for these devices is TA49015.

Package

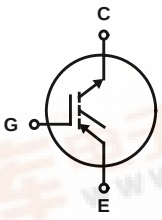
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings

T_C = +25°C, Unless Otherwise Specified

		HGTD8P50G1/G1S	UNITS
Collector-Emitter Breakdown Voltage	BV_{CES}	-500	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	10	V
Collector Current Continuous			
At T_C = +25°C	I_{C25}	-12	A
At T_C = +90°C	I_{C90}	-8	A
Collector Current Pulsed (Note 1)	I_{CM}	-18	A
Gate-Emitter Voltage Continuous	V_{GES}	±20	V
Gate-Emitter Voltage Pulsed	V_{GEM}	±30	V
Switching SOA at T_C = +25°C, V_{CL} = -350V	SSOA		
No Snubber, Figure 17 - Circuit 1		-3	A
With 0.1µF Capacitor, Figure 17 - Circuit 2		-18	A
Power Dissipation Total at T_C = +25°C	P_D	66	W
Power Dissipation Derating T_C > +25°C		0.53	W/°C
Operating and Storage Junction Temperature	T_J, T_{STG}	-40 to +150	°C
Maximum Lead Temperature for Soldering (0.125" from case for 5s)	T_L	+260	°C

NOTE:

1. T_J = 25°C, V_{CL} = 350V, R_{GE} = 25Ω, Figure 17 - Circuit 2 (C_1 = 0.1µF)

Specifications HGTD8P50G1, HGTD8P50G1S

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Collector-Emitter Breakdown Voltage	BV_{CES}	I_{CE} = -250μA V_{CL} = -600V	V_{GE} = 0V	-500	-	-	V
Emitter-Collector Breakdown Voltage	BV_{ECS}	I_{EC} = 1mA	V_{GE} = 0V	10	-	-	V
Collector-Emitter Leakage Current	I_{CES}	$V_{CE} = BV_{CES}$	$T_C = +25^oC$	-	-	-250	μA
		$V_{CE} = 0.8\ BV_{CES}$	$T_C = +150^oC$	-	-	-1.0	mA
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	I_{CE} = -3.0A V_{GE} = -15V	$T_C = +25^oC$	-	-2.5	-2.9	V
			$T_C = +150^oC$	-	-2.3	-2.8	V
		$I_{CE} = I_{C90}$ V_{GE} = -15V	$T_C = +25^oC$	-	-3.0	-3.7	V
			$T_C = +150^oC$	-	-3.3	-4.0	V
Gate-Emitter Threshold Voltage	$V_{GE(TH)}$	I_{CE} = -1.0mA	$V_{CE} = V_{GE}$	-4.5	-6.0	-7.5	V
Gate-Emitter Leakage Current	I_{GES}	V_{GE} = ±20V		-	-	±100	nA
Gate-Emitter Plateau Voltage	$V_{GE(PL)}$	I_C = 3A	$V_{CE} = 0.5\ BV_{CES}$	-	-7.0	-	V
On-State Gate Charge	$Q_{G(ON)}$	I_C = 3A, $V_{CE} = 0.5\ BV_{CES}$	V_{GE} = -15V	-	16	25	nC
			V_{GE} = -20V	-	22	30	nC
Current Turn-On Delay Time	$t_{D(ON)I}$	R_L = 113Ω	I_{CE} = -3A, V_{GE} = -15V V_{CE} = -350V R_G = 25Ω $T_J = +150^oC$ Fig. 17, Circuit 1	-	45	-	ns
Current Rise Time	t_{RI}			-	85	-	ns
Current Turn-off Delay Time	$t_{D(OFF)I}$	L = 100μH		-	480	680	ns
Current Fall Time	t_{FI}			-	1800	2500	ns
Turn-Off Energy (Note 1)	E_{OFF}			-	0.8	-	mJ
Current Turn-Off Delay Time	$t_{D(OFF)I}$	L = 100μH	I_{CE} = -8A, V_{GE} = -15V V_{CE} = -350V R_G = 25Ω $T_J = +150^oC$ Fig. 17, Circuit 2 C_1 = .022μF	-	100	200	ns
Current Fall Time	t_{FI}			-	3500	4000	ns
Turn-Off Energy (Note 1)	E_{OFF}			-	1.3	-	mJ
Latching Current	I_L	L = 100μH	V_{GE} = -15V R_G = 25Ω $T_J = +25^oC$ V_{CE} = -350V Fig. 17, Circuit 1	-3	-	-	A
Thermal Resistance	$R_{\theta JC}$			-	1.75	1.90	$^oC/W$

NOTE:

1. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). The HGTD8P50G1 and HGTD8P50G1S were tested per JEDEC standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss. Turn-On losses include diode losses.

Typical Performance Curves

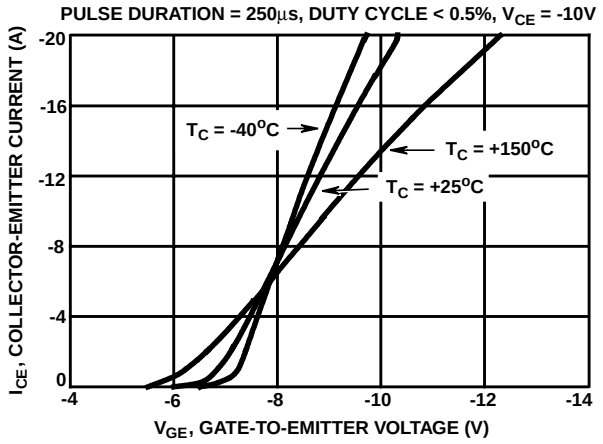


FIGURE 1. TRANSFER CHARACTERISTICS

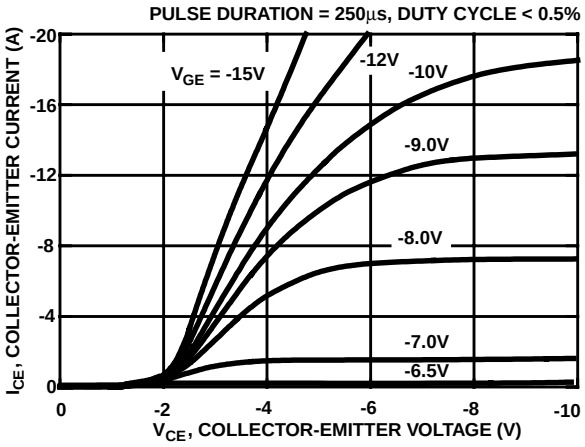


FIGURE 2. SATURATION CHARACTERISTICS

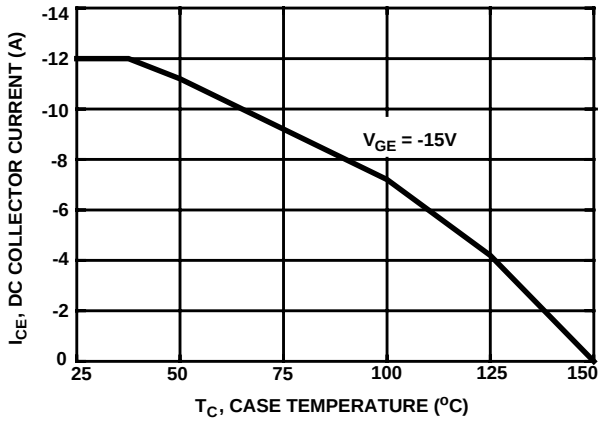


FIGURE 3. MAXIMUM DC COLLECTOR CURRENT AS A FUNCTION OF CASE TEMPERATURE

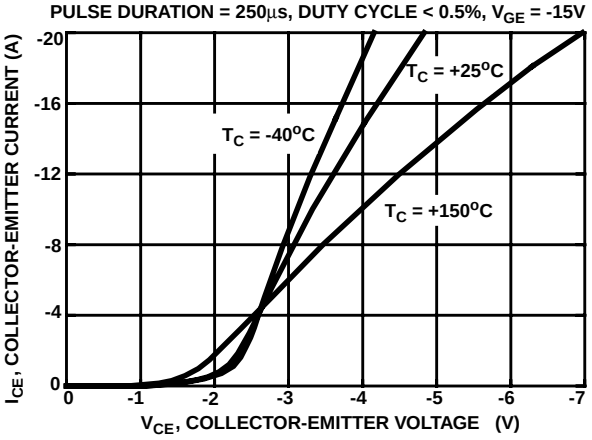


FIGURE 4. COLLECTOR-EMITTER SATURATION VOLTAGE

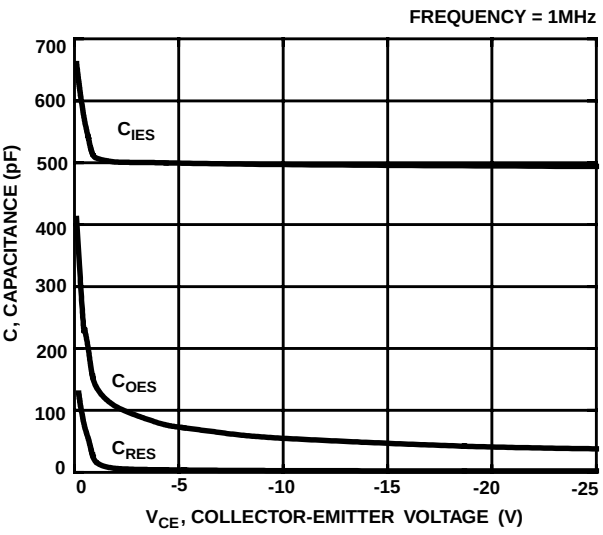


FIGURE 5. CAPACITANCE AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

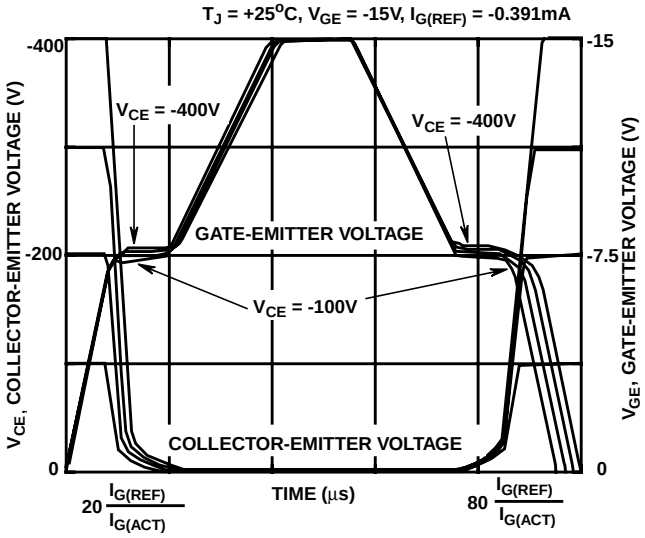


FIGURE 6. NORMALIZED SWITCHING WAVEFORMS AT CONSTANT GATE CURRENT. (REFER TO APPLICATION NOTES AN7254 AND AN7260)

Typical Performance Curves (Continued)

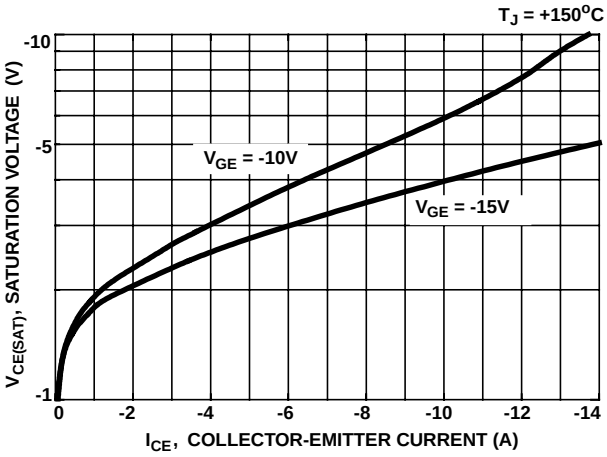


FIGURE 7. SATURATION VOLTAGE AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

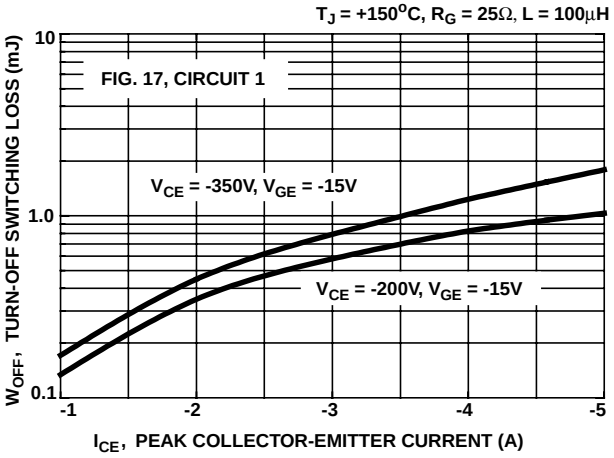


FIGURE 8. TURN-OFF SWITCHING LOSS AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

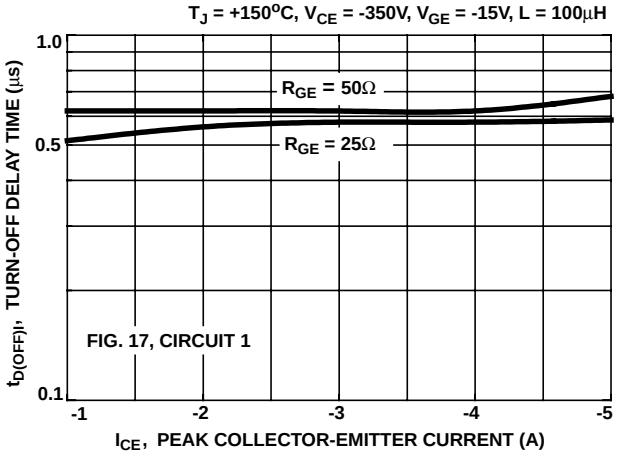


FIGURE 9. TURN-OFF DELAY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

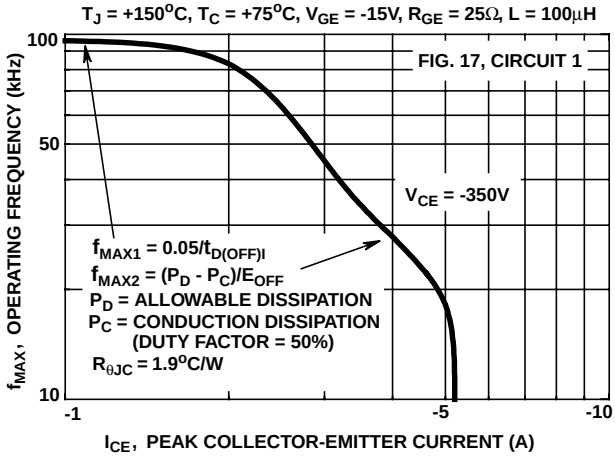


FIGURE 10. OPERATING FREQUENCY AS A FUNCTION OF COLLECTOR-EMITTER CURRENT AND VOLTAGE

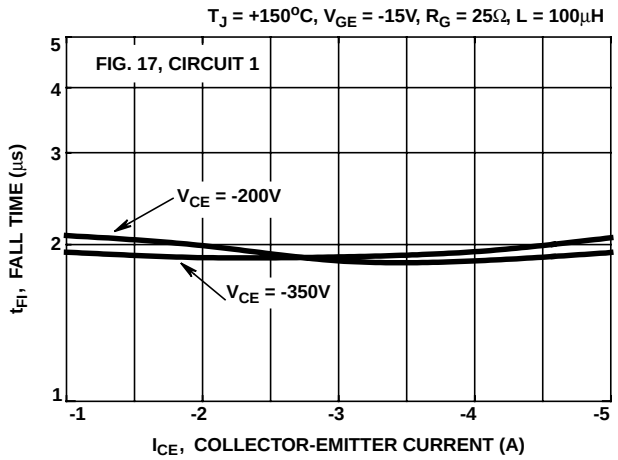


FIGURE 11. FALL TIME AS A FUNCTION OF COLLECTOR-EMITTER CURRENT

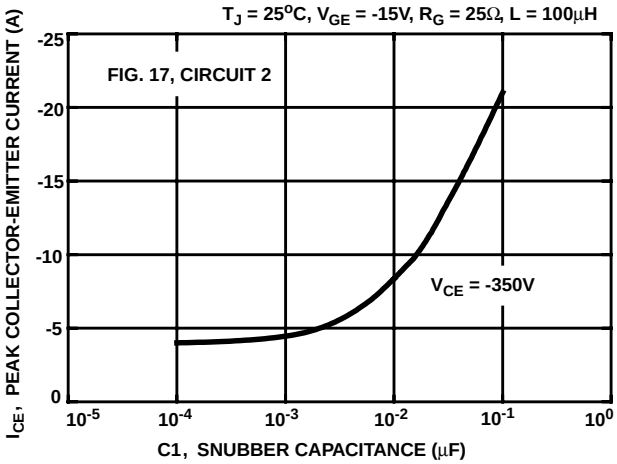


FIGURE 12. LATCHING CURRENT AS A FUNCTION OF SNUBBER CAPACITANCE

Typical Performance Curves (Continued)

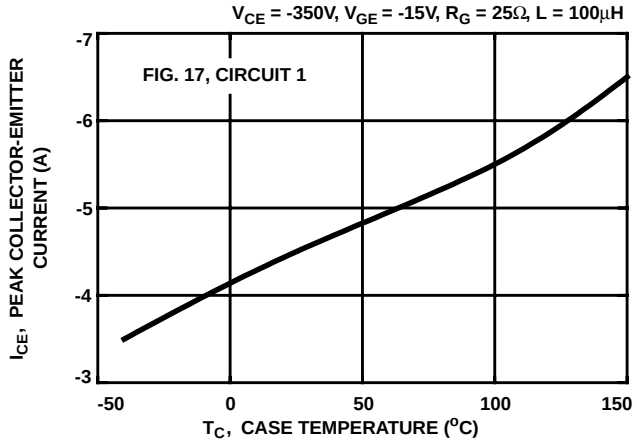


FIGURE 13. LATCHING CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

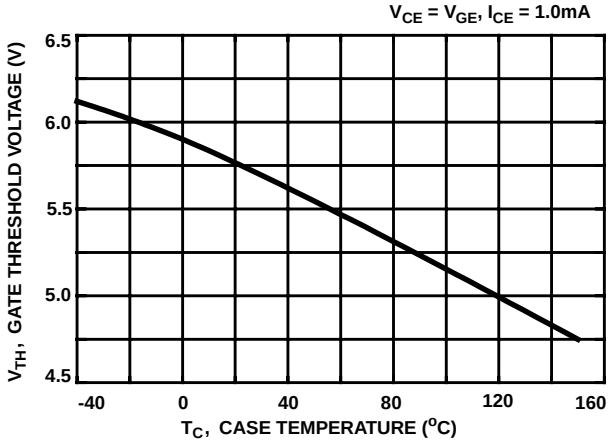


FIGURE 14. GATE THRESHOLD VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

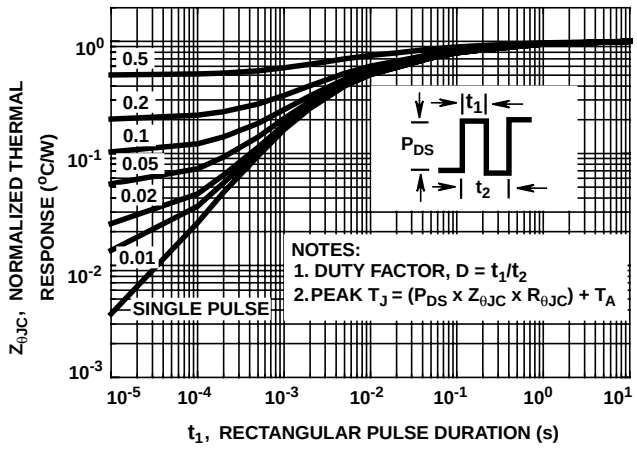


FIGURE 15. IGBT NORMALIZED TRANSIENT THERMAL IMPEDANCE, JUNCTION TO CASE

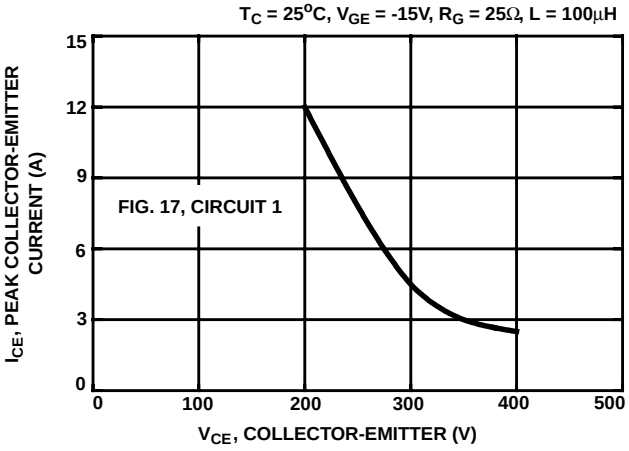


FIGURE 16. LATCHING CURRENT AS A FUNCTION OF COLLECTOR-EMITTER VOLTAGE

Test Circuits

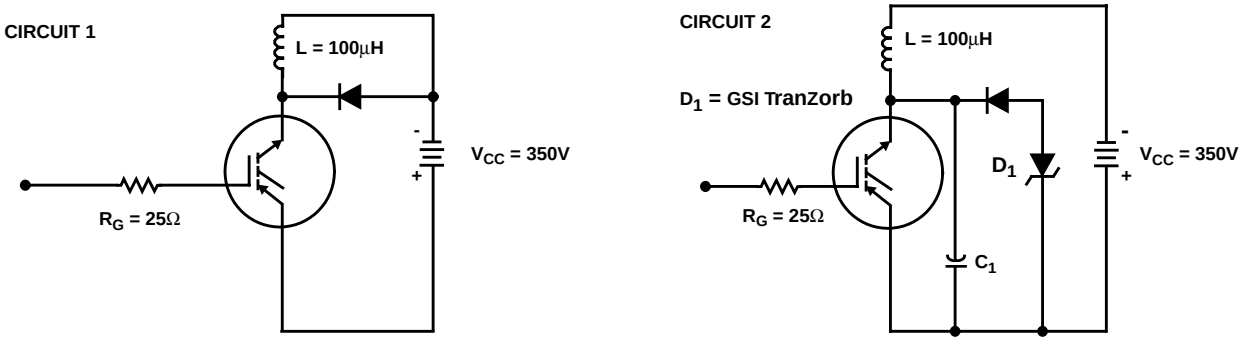


FIGURE 17. INDUCTIVE SWITCHING TEST CIRCUITS

Operating Frequency Information

Operating frequency information for a typical device (Figure 10) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figure 7, Figure 8 and Figure 9. The operating frequency plot (Figure 10) of a typical device shows f_{MAX1} or f_{MAX2} whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/t_{D(OFF)I}$. $t_{D(OFF)I}$ deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{D(OFF)I}$ is defined as the time between the 90% point of the trailing edge of the input pulse and the point where the collector current falls to 90% of its maximum value. Device Turn-Off delay can establish an additional frequency limiting condition for an application other than T_{JMAX}. $t_{D(OFF)I}$ is important when controlling output ripple under a lightly loaded condition. f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/E_{OFF}$. The allowable dissipation (P_D) is defined by $P_D = (T_{JMAX} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed Pd. A 50% duty factor was used (Figure 10) and the conduction losses (Pc) are approximated by $Pc = (V_{CE} \bullet I_{CE})/2$. E_{OFF} is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A).

The switching power loss (Figure 10) is defined as $f_{MAX2} \bullet E_{OFF}$. Turn-On switching losses are not included because they can be greatly influenced by external circuit conditions and components.

Handling Precautions for IGBTs

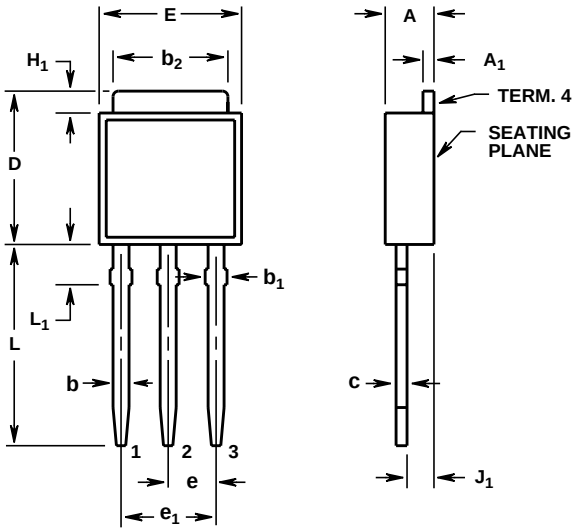
Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "†ECCOSORBD LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in Turn-On of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic zener diode from gate to emitter. If gate protection is required an external zener is recommended.

† Trademark Emerson and Cumming, Inc.

TO-251AA

3 LEAD JEDEC TO-251AA PLASTIC PACKAGE



Lead 1	Gate
Lead 2	Collector
Lead 3	Emitter
Term. 4	Collector

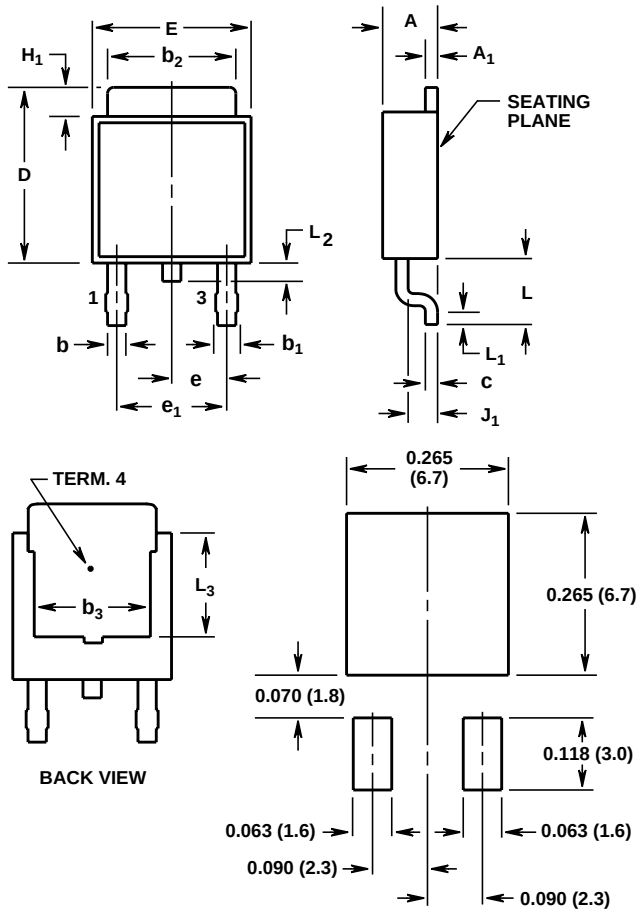
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



Lead 1	Gate
Lead 3	Source
Term. 4	Collector

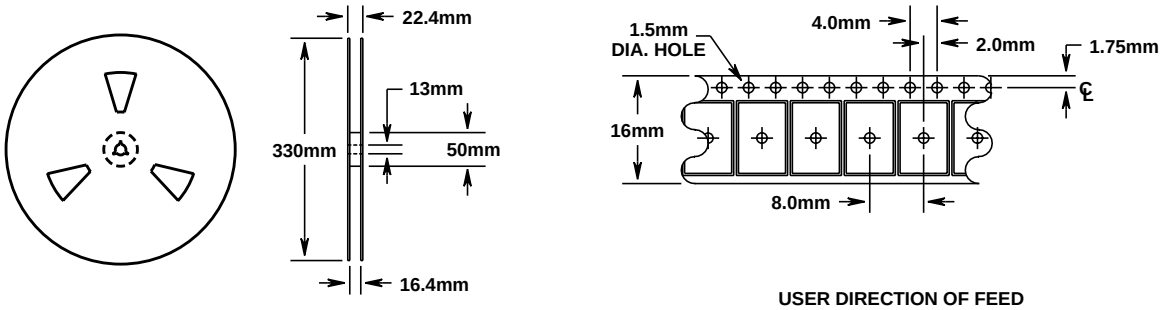
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

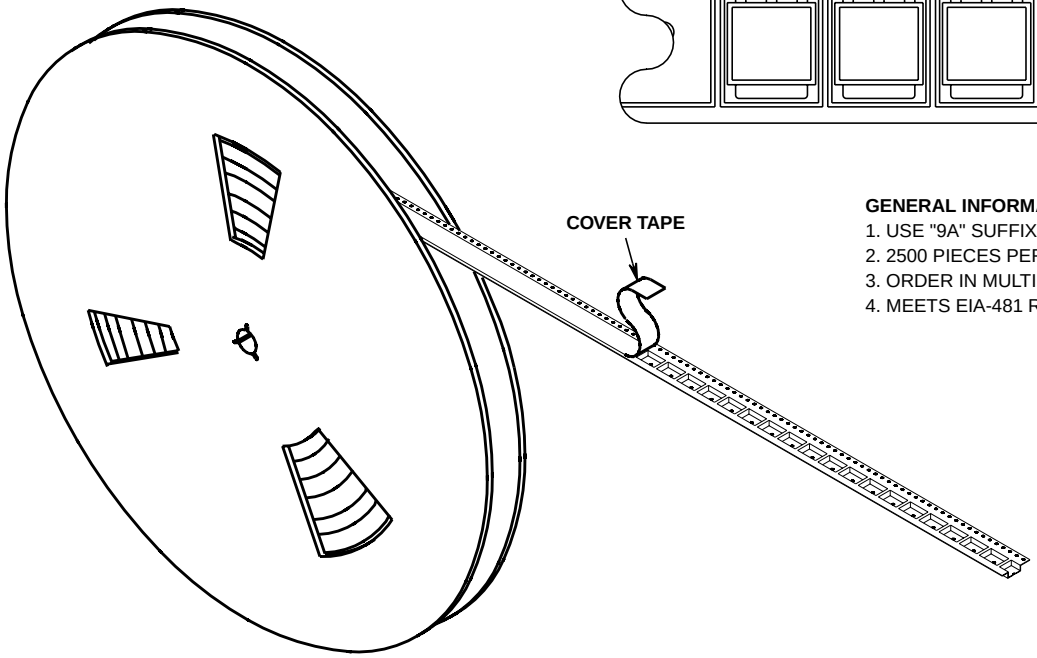
NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 10-95.

TO-252AA

16mm TAPE AND REEL





GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

Revision 5 dated 10-95

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

For information regarding Intersil Corporation and its products, see web site **http://www.intersil.com**

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