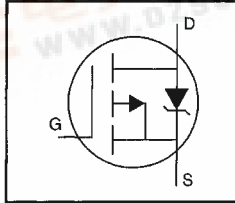


HEXFET® Power MOSFET

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- Fast Switching
- Ease of Paralleling



$$V_{DSS} = -200V$$

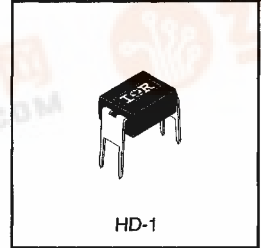
$$R_{DS(on)} = 1.5\Omega$$

$$I_D = -0.56A$$

Description

The HEXFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-0.56	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10 V$	-0.36	
I_{DM}	Pulsed Drain Current ①	-4.5	
$P_D @ T_C = 25^\circ C$	Power Dissipation	1.0	W
	Linear Derating Factor	0.0083	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	420	mJ
I_{AR}	Avalanche Current ①	-0.56	A
E_{AR}	Repetitive Avalanche Energy ①	0.10	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J	Operating Junction and Storage Temperature Range	-55 to +150	°C
T_{STG}			
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance


	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient	—	—	120	°C/W




IRFD9220



Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-200	—	—	V	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.22	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D=-1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	1.5	Ω	$V_{GS}=10\text{V}$, $I_D=-0.34\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$
g_{fs}	Forward Transconductance	0.55	—	—	S	$V_{DS}=-50\text{V}$, $I_D=-0.35\text{A}$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	-100	μA	$V_{DS}=-200\text{V}$, $V_{GS}=0\text{V}$
		—	—	-500		$V_{DS}=-160\text{V}$, $V_{GS}=0\text{V}$, $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS}=-20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS}=20\text{V}$
Q_g	Total Gate Charge	—	—	15	nC	$I_D=-2.1\text{A}$
Q_{GS}	Gate-to-Source Charge	—	—	3.2		$V_{DS}=-160\text{V}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	8.4		$V_{GS}=-10\text{V}$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	8.8	—	ns	$V_{DD}=-100\text{V}$
t_r	Rise Time	—	27	—		$I_D=-3.9\text{A}$
$t_{d(off)}$	Turn-Off Delay Time	—	7.3	—		$R_G=18\Omega$
t_f	Fall Time	—	19	—		$R_D=24\Omega$ See Figure 10 ④
L_D	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance	—	6.0	—		
C_{iss}	Input Capacitance	—	340	—	pF	$V_{GS}=0\text{V}$
C_{oss}	Output Capacitance	—	110	—		$V_{DS}=-25\text{V}$
C_{rss}	Reverse Transfer Capacitance	—	33	—		$f=1.0\text{MHz}$ See Figure 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-0.56	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-4.5		
V_{SD}	Diode Forward Voltage	—	—	-6.3	V	$T_J=25^\circ\text{C}$, $I_S=-0.56\text{A}$, $V_{GS}=0\text{V}$ ④
t_{rr}	Reverse Recovery Time	—	150	300	ns	$T_J=25^\circ\text{C}$, $I_F=-3.9\text{A}$
Q_{rr}	Reverse Recovery Charge	—	0.97	2.0	μC	$di/dt=100\text{A}/\mu\text{s}$ ④

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ② $V_{DD}=-50\text{V}$, starting $T_J=25^\circ\text{C}$, $L=130\text{mH}$
 $R_G=25\Omega$, $I_{AS}=-2.2\text{A}$ (See Figure 12)
- ③ $I_{SD} \leq -3.9\text{A}$, $di/dt \leq 95\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.

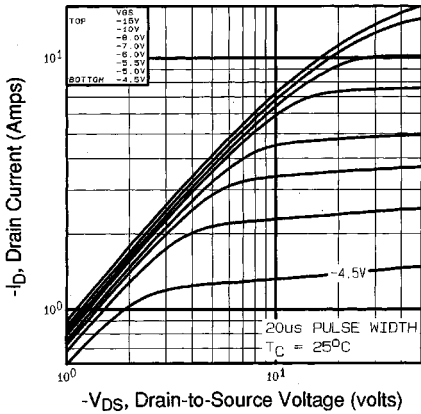


Fig 1. Typical Output Characteristics,
 $T_C=25^{\circ}\text{C}$

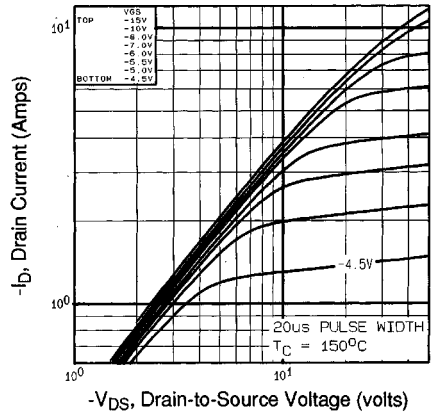


Fig 2. Typical Output Characteristics,
 $T_C=150^{\circ}\text{C}$

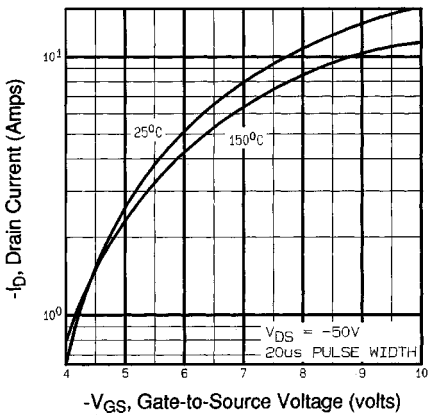


Fig 3. Typical Transfer Characteristics

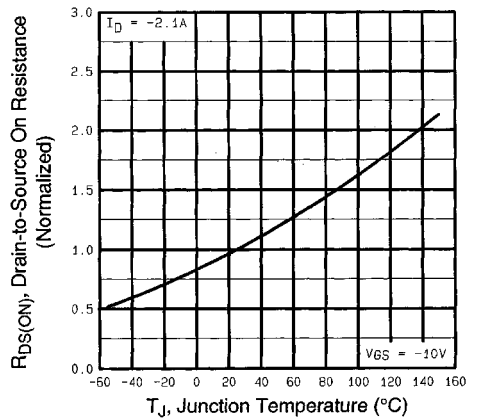


Fig 4. Normalized On-Resistance
Vs. Temperature

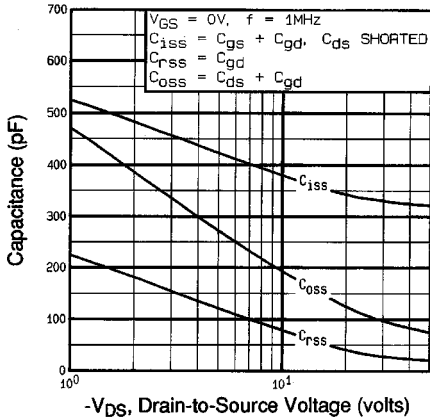


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

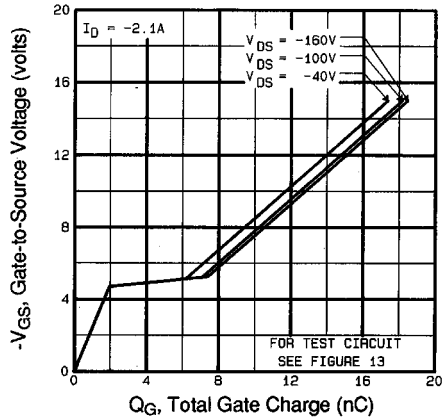


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

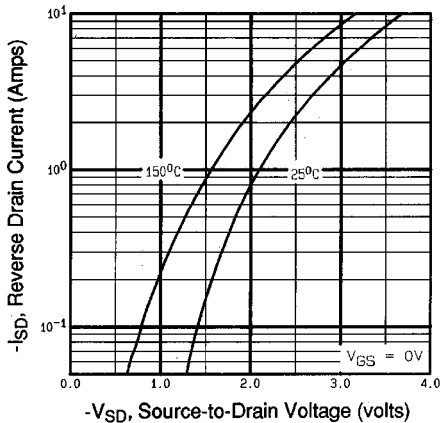


Fig 7. Typical Source-Drain Diode Forward Voltage

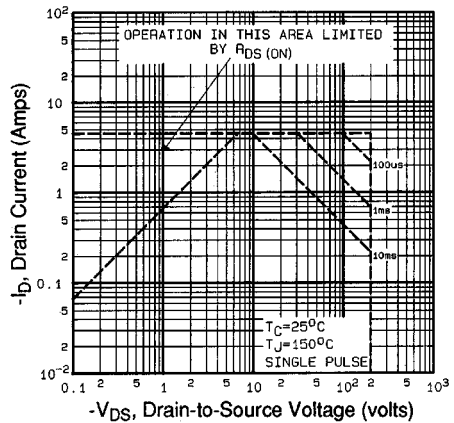


Fig 8. Maximum Safe Operating Area

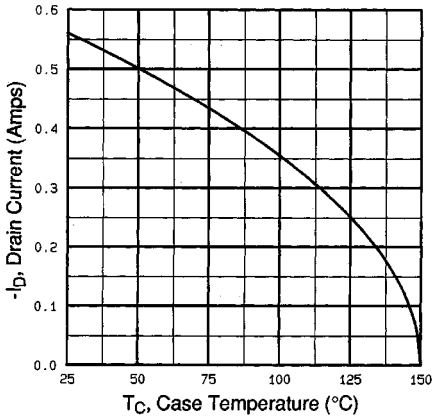


Fig 9. Maximum Drain Current Vs. Case Temperature

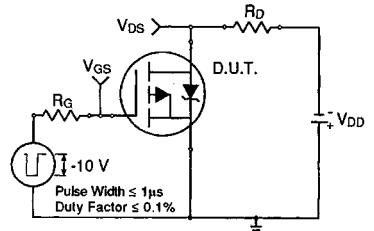


Fig 10a. Switching Time Test Circuit

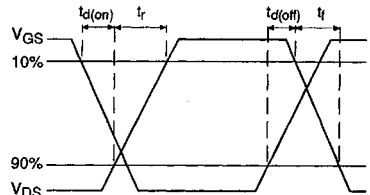


Fig 10b. Switching Time Waveforms

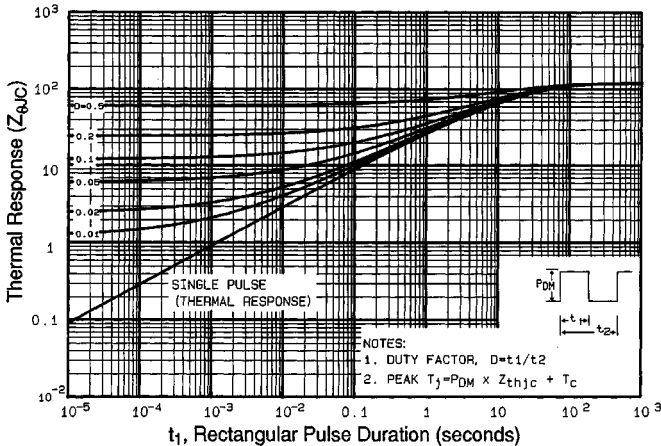


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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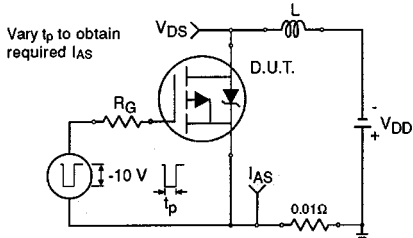


Fig 12a. Unclamped Inductive Test Circuit

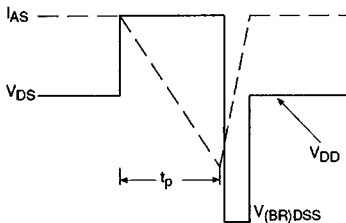


Fig 12b. Unclamped Inductive Waveforms

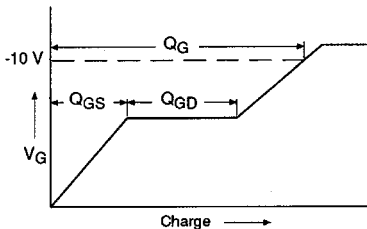


Fig 13a. Basic Gate Charge Waveform

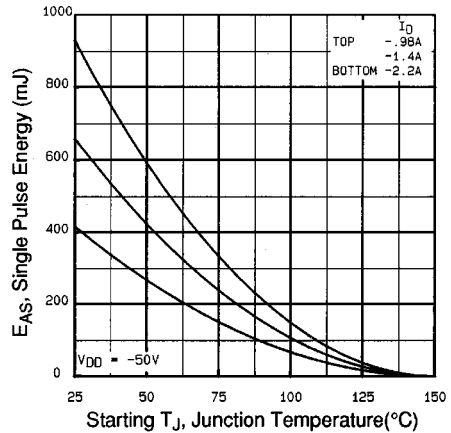


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

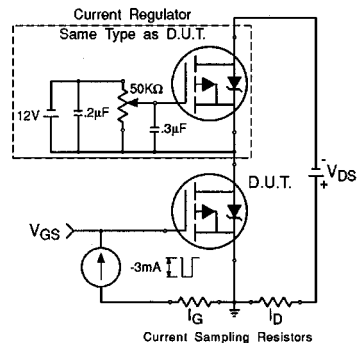


Fig 13b. Gate Charge Test Circuit

Appendix A: Figure 14, Peak Diode Recovery dv/dt Test Circuit – See page 1506

Appendix B: Package Outline Mechanical Drawing – See page 1507

Appendix C: Part Marking Information – See page 1515