Complete 10-Bit 18 MSPS CCD Signal Processor

AD9804

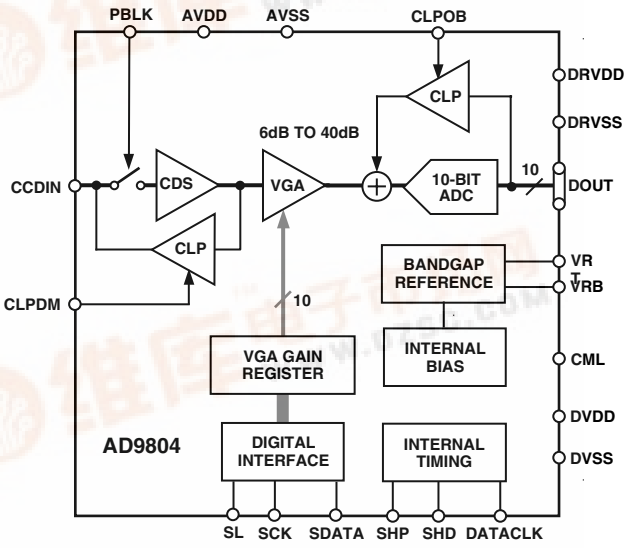
FEATURES

18 MSPS Correlated Double Sampler (CDS)
6 dB to 40 dB 10-Bit Variable Gain Amplifier (VGA)
Low Noise Clamp Circuits
Preblanking Function
10-Bit 18 MSPS A/D Converter
3-Wire Serial Digital Interface
3 V Single Supply Operation
Low Power CMOS
48-Lead LQFP Package

APPLICATIONS

PC Cameras
Digital Still Cameras

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9804 is a complete analog signal processor for CCD applications. It features an 18 MHz single-channel architecture designed to sample and condition the outputs of interlaced and progressive scan area CCD arrays. The AD9804's signal chain consists of an input clamp, correlated double sampler (CDS), digitally controlled VGA, black level clamp, and a 10-bit A/D converter. The internal VGA gain register is programmed through a 3-wire serial digital interface.

REV. 0

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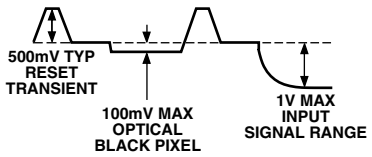
AD9804–SPECIFICATIONS

ANALOG SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = DVDD = 3.0 V, $f_{DATACLK} = f_{SHP} = f_{SHD}$ = 18 MHz, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	–20		+85	°C
Storage	–65		+150	°C
POWER SUPPLY VOLTAGE				
Analog, Digital, Digital Driver	2.8	3.0	3.6	V
POWER CONSUMPTION		85		mW
MAXIMUM CLOCK RATE	18			MHz
CORRELATED DOUBLE SAMPLER (CDS)				
Allowable CCD Reset Transient[1]		500		mV
Max Input Range before Saturation[1]		1.0		V p-p
Max CCD Black Pixel Amplitude[1]		100		mV
VARIABLE GAIN AMPLIFIER (VGA)				
Gain Control Resolution		1024		Steps
Gain Range (VGA Gain Curve Shown in Figure 5)				
Min Gain (Code 95)	4	6	8	dB
Max Gain (Code 1023)	38	40	42	dB
BLACK LEVEL CLAMP				
Clamp Level (At ADC Output)		32		LSB
A/D CONVERTER				
Resolution		10		Bits
No Missing Codes	10			Bits Guaranteed
Full-Scale Input Voltage		2.0		V
VOLTAGE REFERENCE				
Reference Top Voltage (VRT)		2.0		V
Reference Bottom Voltage (VRB)		1.0		V

NOTES
[1]Input signal characteristics defined as follows:



Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (DRVDD = 2.7 V, C_L = 20 pF.)

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	2.1			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V_{OH}	2.1			V
Low Level Output Voltage	V_{OL}			0.6	V
High Level Output Current	I_{OH}		50		µA
Low Level Output Current	I_{OL}		50		µA

Specifications subject to change without notice.

TIMING SPECIFICATIONS (C_L = 20 pF, f_{CLK} = 18 MHz, timing shown in Figures 1 and 2.)

Parameter	Symbol	Min	Typ	Max	Unit
SAMPLE CLOCKS					
DATACLK, SHP, SHD Clock Period	t_{CONV}		55.6		ns
DATACLK Hi/Low Pulsewidth	t_{ADC}	20	27.7		ns
SHP Pulsewidth	t_{SHP}	10	14		ns
SHD Pulsewidth	t_{SHD}	10	14		ns
CLPDM Pulsewidth	t_{CDM}	4	10		Pixels
CLPOB Pulsewidth[1]	t_{COB}	2	10		Pixels
SHP Rising Edge to SHD Falling Edge	t_{S1}	20	27		ns
SHP Rising Edge to SHD Rising Edge	t_{S2}	20	27		ns
Internal Clock Delay	t_{ID}		3.0		ns
Inhibited Clock Period	t_{INH}	10			ns
DATA OUTPUTS					
Output Delay	t_{OD}		14.5	16	ns
Output Hold Time	t_H	6.0	7.6		ns
Pipeline Delay			9		Cycles
SERIAL INTERFACE					
Maximum SCK Frequency	f_{SCLK}	10			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
SCK Falling Edge to SDATA Valid Read	t_{DV}	10			ns

NOTES
[1]Minimum CLPOB pulsewidth is for functional operation only. Wider typical pulses are recommended to achieve low noise clamp performance.

Specifications subject to change without notice

ABSOLUTE MAXIMUM RATINGS

Parameter	With Respect To	Min	Max	Unit
AVDD	AVSS	–0.3	+3.9	V
DVDD	DVSS	–0.3	+3.9	V
DRVDD	DRVSS	–0.3	+3.9	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
SHP, SHD, DATACLK	DVSS	–0.3	DVDD + 0.3	V
CLPOB, CLPDM, PBLK	DVSS	–0.3	DVDD + 0.3	V
SCK, SL, SDATA	DVSS	–0.3	DVDD + 0.3	V
VRT, VRB, CMLEVEL	AVSS	–0.3	AVDD + 0.3	V
BYP1–4, CCDIN	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9804JST	–20°C to +85°C	Thin Plastic Quad Flatpack (LQFP)	ST-48

THERMAL CHARACTERISTICS

Thermal Resistance

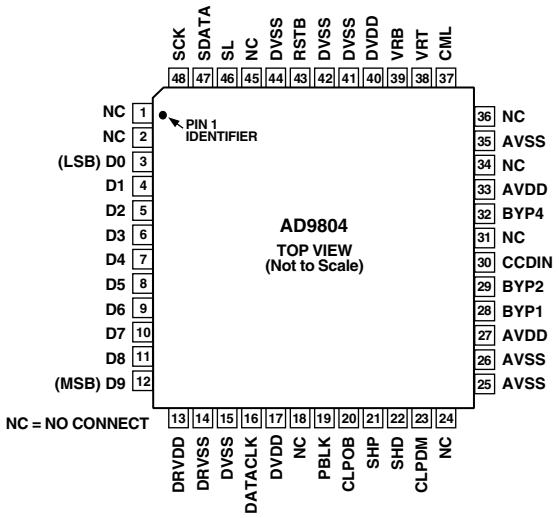
48-Lead LQFP Package

θ_{JA} = 92°C/W

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9804 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

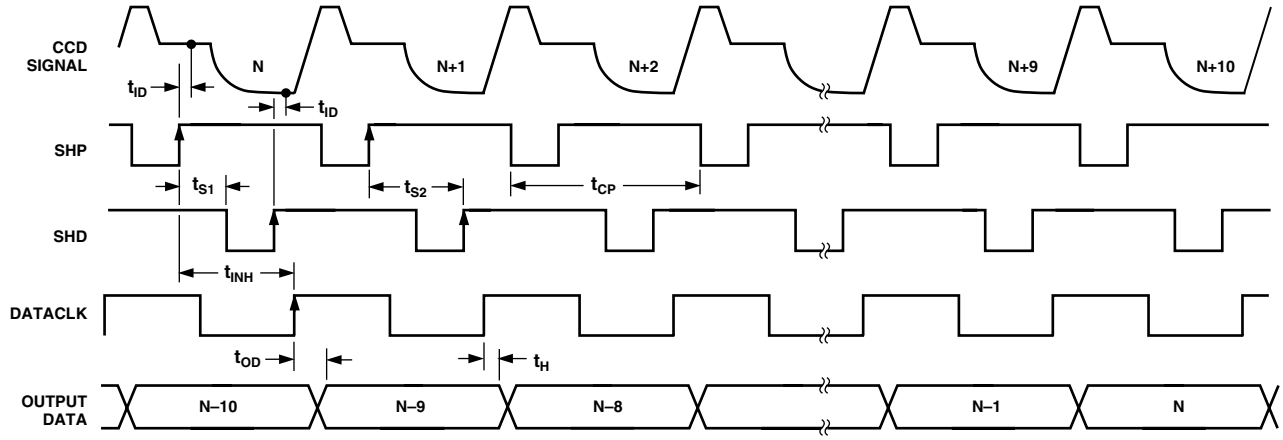


PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Type	Description
1, 2, 18, 24, 31 34, 36, 45	NC	NC	Internally Not Connected
3–12	D0–D9	DO	Digital Data Outputs
13	DRVDD	P	Digital Output Driver Supply
14	DRVSS	P	Digital Output Driver Ground
15, 41, 42, 44	DVSS	P	Digital Ground
16	DATACLK	DI	Digital Data Output Latch Clock
17, 40	DVDD	P	Digital Supply
19	PBLK	DI	Preblanking Clock Input
20	CLPOB	DI	Black Level Clamp Clock Input
21	SHP	DI	CDS Sampling Clock for CCD's Reference Level
22	SHD	DI	CDS Sampling Clock for CCD's Data Level
23	CLPDM	DI	Input Clamp Clock Input
25, 26, 35	AVSS	P	Analog Ground
27, 33	AVDD	P	Analog Supply
28	BYP1	AO	Internal Bias Level Decoupling
29	BYP2	AO	Internal Bias Level Decoupling
30	CCDIN	AI	Analog Input for CCD Signal
32	BYP4	AO	Internal Bias Level Decoupling
37	CML	AO	Internal Bias Level Decoupling
38	VRT	AO	A/D Converter Top Reference Voltage Decoupling
39	VRB	AO	A/D Converter Bottom Reference Voltage Decoupling
43	RSTB	DI	Chip Reset Control. Active Low
46	SL	DI	Serial Digital Interface Load Pulse.
47	SDATA	DI	Serial Digital Interface Data
48	SCK	DI	Serial Digital Interface Clock

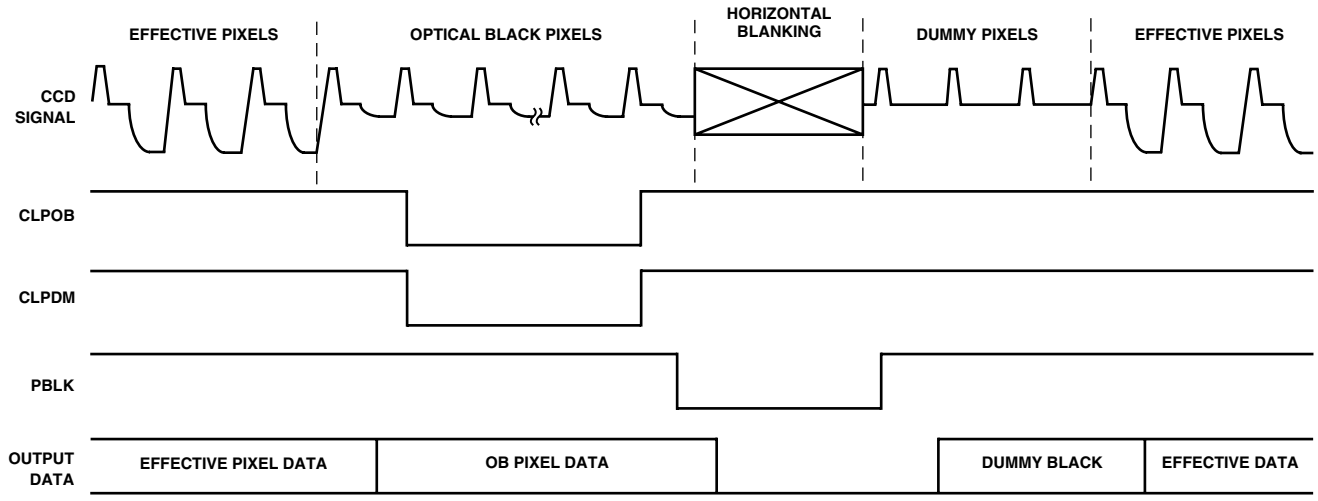
TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input, DO = Digital Output, P = Power.

TIMING DIAGRAMS



NOTES:
1. RECOMMENDED PLACEMENT FOR DATACLK RISING EDGE IS BETWEEN THE SHD RISING EDGE AND NEXT SHP FALLING EDGE.
2. CCD SIGNAL IS SAMPLED AT SHP AND SHD RISING EDGES.

Figure 1. Pixel Rate Timing



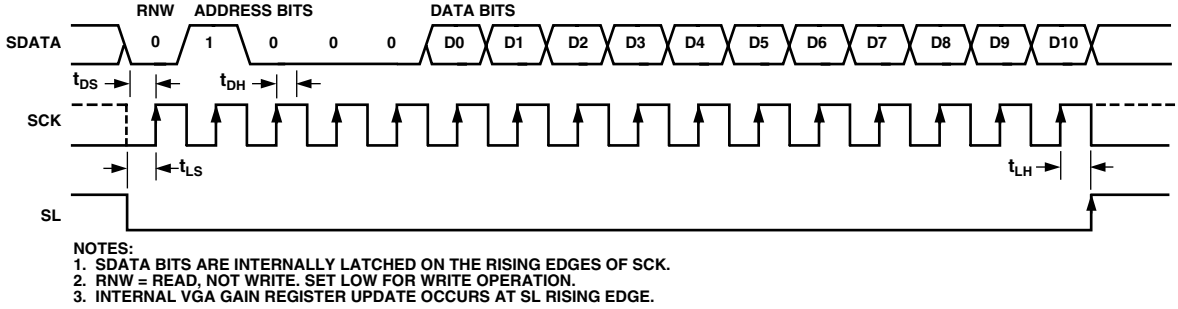
NOTES:
1. CLPOB AND CLPDM WILL OVERWRITE PBLK. PBLK WILL NOT AFFECT CLAMP OPERATION IF OVERLAPPING CLPDM AND/OR CLPOB.
2. PBLK SIGNAL IS OPTIONAL.
3. DIGITAL OUTPUT DATA WILL BE ALL ZEROS DURING PBLK. OUTPUT DATA LATENCY IS 9 DATACLK CYCLES.

Figure 2. Typical Line Clamp Timing

PROGRAMMING THE SERIAL INTERFACE

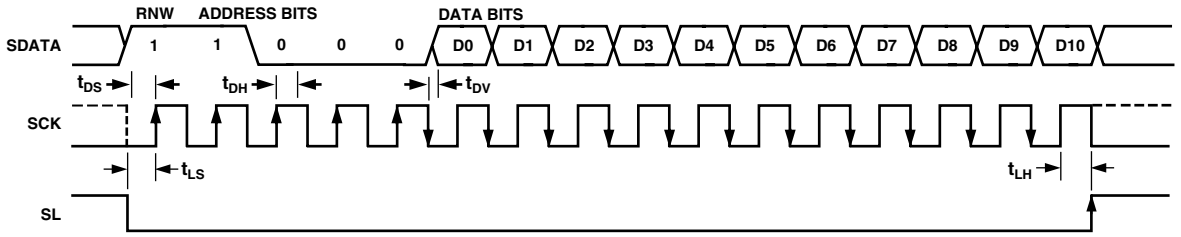
Table I. VGA Gain Register Contents (Default Value x096)

MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	Gain (dB)
0	0	0	1	0	1	1	1	1	1	6.0
					•					•
					•					•
					•					•
1	1	1	1	1	1	1	1	1	0	39.965
1	1	1	1	1	1	1	1	1	1	40.0



NOTES:
1. SDATA BITS ARE INTERNALLY LATCHED ON THE RISING EDGES OF SCK.
2. RNW = READ, NOT WRITE. SET LOW FOR WRITE OPERATION.
3. INTERNAL VGA GAIN REGISTER UPDATE OCCURS AT SL RISING EDGE.

Figure 3. Serial Write Operation



NOTES:
1. RNW = READ, NOT WRITE. SET HIGH FOR READ OPERATION.
2. THE RNW BIT AND THE FOUR ADDRESS BITS MUST BE WRITTEN TO THE AD9804. SDATA IS LATCHED ON SCK RISING EDGES.
3. SERIAL DATA FROM VGA GAIN REGISTER IS VALID STARTING AFTER THE 5TH SCK FALLING EDGE, AND IS UPDATED ON SCK FALLING EDGES.

Figure 4. Serial Readback Operation

VARIABLE GAIN AMPLIFIER (VGA) OPERATION DETAILS

The VGA stage provides a gain range of 6 dB to 40 dB, programmable with 10-bit resolution through the serial digital interface. The minimum gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems (such as ADI's AD9803), the equivalent gain range is 0 dB to 34 dB.

The VGA gain curve is divided into two separate regions. When the VGA Gain Register code is between 0 and 511, the curve follows a (1 + x)/(1 – x) shape, which is similar to a "linear-in-dB" characteristic. From code 512 to code 1023, the curve follows a "linear-in-dB" shape. The exact VGA gain can be calculated for any Gain Register value by using the following two equations:

Code Range	Gain Equation (dB)
0–511	$Gain = 20 \log_{10}([658 + code]/[658 - code]) + 3.6$
512–1023	$Gain = (0.0354)(code) + 3.6$

As shown in the Analog Specifications, only the VGA gain range from 2 dB to 36 dB has been specified. This corresponds to a VGA gain code range of 95 to 1023.

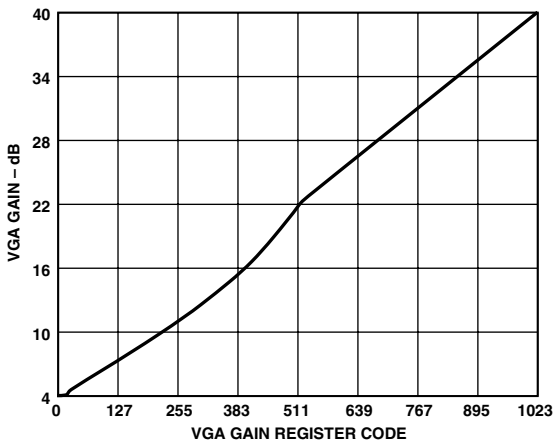


Figure 5. VGA Gain Curve

APPLICATIONS INFORMATION

The AD9804 is a complete Analog Front-End (AFE) product for PC camera, digital still camera, and camcorder applications. As shown in Figure 6, the CCD image (pixel) data is buffered and sent to the AD9804 analog input through a series input capacitor. The AD9804 performs the dc restoration, CDS, gain adjustment, black level correction, and analog-to-digital conversion. The AD9804's digital output data is then processed by the image processing ASIC. The internal registers of the AD9804 used to control gain, offset level, and other functions are programmed by the ASIC or microprocessor through a 3-wire serial digital interface. A system timing generator provides the clock signals for both the CCD and the AFE.

Generating the Reset (RSTB) Signal

After power-on, the AD9804 must be reset using Pin 43 (RSTB). The reset pulse must be an active low signal, which goes low for at least 100 ns after the power supplies have settled. After the RSTB signal returns high, the AD9804 is internally reset to the default VGA gain register value. If a system reset pulse is not available, a simple RC network may be used, as shown in Figure 7. The time constant of this network should be comparable to the power-on time of the AD9804's power supplies. For example, if the power supplies have a power-on time of 10 ms, the RC network should have a time constant of 10 ms, giving R = 10 kΩ and C = 1.0 µF.

Serial writes to the AD9804 internal registers must not be performed until 20 µs after the reset pulse has occurred. This allows enough time for internal calibration routines to be completed. SDATA and SCK may be active before the reset sequence, but SL should be held logic HIGH until 20 µs or more after the reset.

Alternatively, placing series resistors close to the digital output pins may help reduce noise.

Grounding and Decoupling Recommendations

As shown in Figure 7, a single ground plane is recommended for the AD9804. This ground plane should be as continuous as possible, particularly around Pins 25 through 39. This will ensure that all analog decoupling capacitors provide the lowest possible impedance path between the power and bypass pins and their respective ground pins. All decoupling capacitors should be located as close as possible to the package pins. A single clean power supply is recommended for the AD9804, but a separate digital driver supply may be used for DRVDD (Pin 13). DRVDD should always be decoupled to DRVSS (Pin 14), which should be connected to the analog ground plane. Advantages of using a separate digital driver supply include using a lower voltage (2.7 V) to match levels with a 2.7 V ASIC, reducing digital power dissipation, and reducing potential noise coupling. If the digital outputs (Pins 3–12) must drive a load larger than 20 pF, buffering is recommended to reduce digital code transition noise.

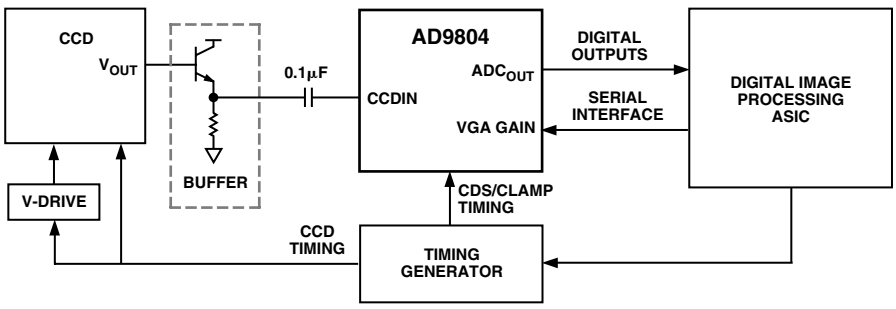


Figure 6. System Block Diagram

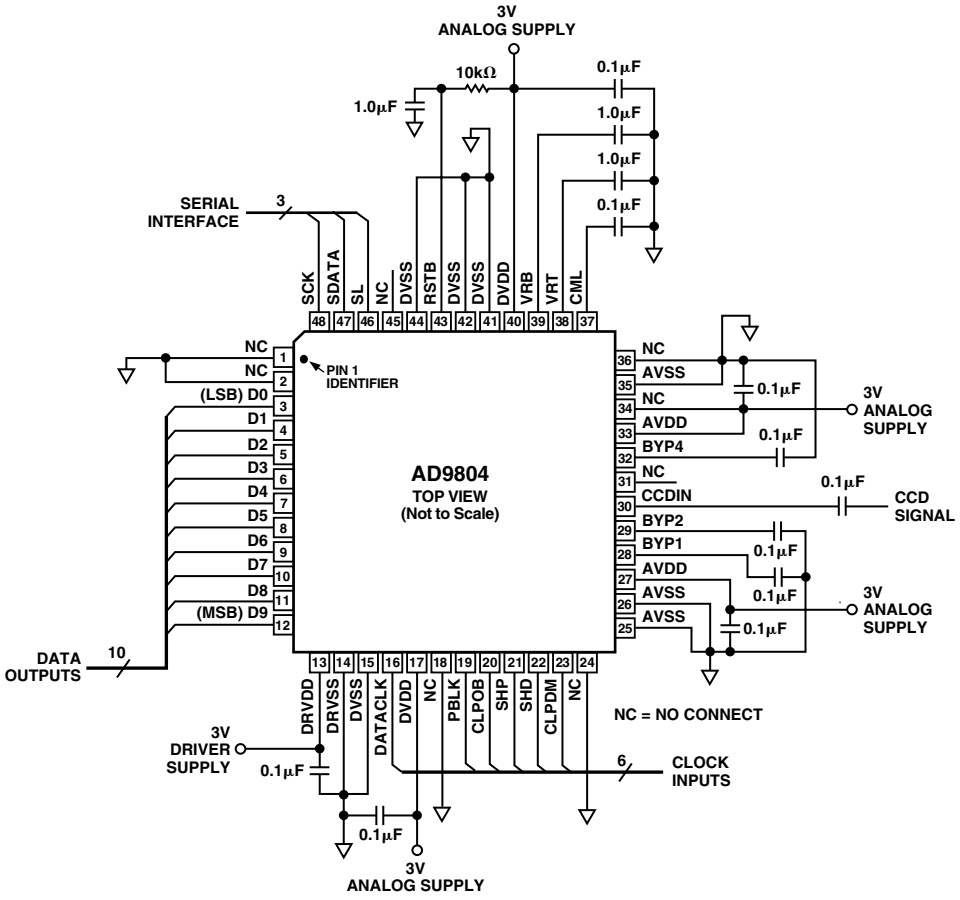


Figure 7. AD9804 Circuit Configuration

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

48-Lead, LQFP
(ST-48)