



# Complete 12-Bit 6 MSPS CCD/CIS Signal Processor

## AD9816

### FEATURES

- 12-Bit 6 MSPS A/D Converter
- No Missing Codes Guaranteed
- 3-Channel or 1-Channel Operation
- Correlated Double Sampling
- 8-Bit Programmable Gain
- 8-Bit Offset Adjustment
- PGA Output Monitor
- Input Clamp Circuitry
- Internal Voltage Reference
- 3-Wire Serial Interface
- +3.3 V/+5 V Digital Output Compatibility
- 44-Lead MQFP Package
- Low Power CMOS: 420 mW Typ

### PRODUCT DESCRIPTION

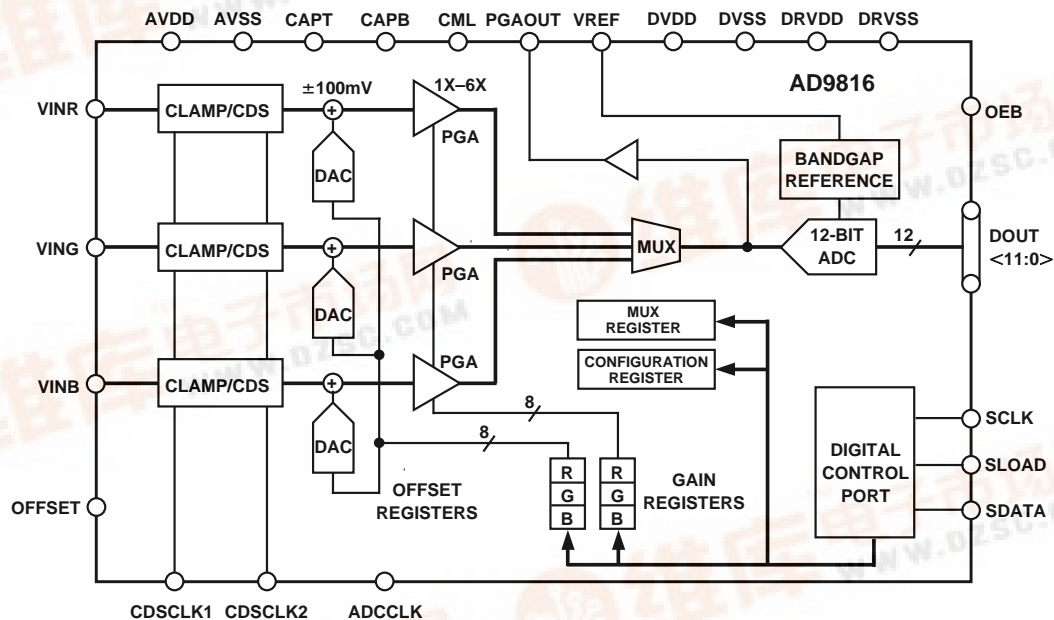
The AD9816 is a complete analog signal processor for CCD and CIS applications. Included is all the necessary circuitry to perform three-channel conditioning and sampling for a variety of imaging applications.

The signal chain consists of an input clamp, correlated double sampler (CDS), offset adjust DAC, programmable gain amplifier and a 12-bit A/D converter. The CDS and input clamp may be disabled for CIS applications.

The internal registers are programmed using a 3-wire serial interface and provide adjustment of the gain, offset and operating mode.

The AD9816 operates from a +5 V supply, typically consumes 420 mW of power and is packaged in a 44-lead MQFP.

### FUNCTIONAL BLOCK DIAGRAM



REV. A

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# AD9816—SPECIFICATIONS

## ANALOG SPECIFICATIONS

( $T_{\text{MIN}}$  to  $T_{\text{MAX}}$  with  $AVDD = +5.0\text{ V}$ ,  $DVDD = +5.0\text{ V}$ ,  $DRVDD = +5.0\text{ V}$ , CDS Mode,  $f_{\text{ADCCLK}} = 6\text{ MHz}$ ,  $f_{\text{CDSCLK1}} = 2\text{ MHz}$ ,  $f_{\text{CDSCLK2}} = 2\text{ MHz}$ , PGA Gain = 1, Input Range = 3 V p-p, Input Capacitor = 1200 pF, unless otherwise noted)

Parameter	AD9816	AD9816-80010	Units
MAXIMUM CONVERSION RATE			
3-Channel Mode with CDS	6	6	MSPS min
1-Channel Mode with CDS	6	6	MSPS min
ACCURACY (Includes Entire Signal Path)			
ADC Resolution	12	12	Bits min
Differential Nonlinearity (DNL)	$\pm 0.4$ $\pm 1.0$	$\pm 0.75$	LSB typ LSB max
No Missing Codes	12		Bits Guaranteed
Integral Nonlinearity (INL)	$\pm 1.5$ $\pm 4.0$	$\pm 2.5$	LSB typ LSB max
Offset Error	2.4		% FSR max
Gain Error <sup>1</sup>	4.3		% FSR max
ANALOG INPUTS			
Input Voltage Range <sup>2</sup>	0 3	0 3	V min V max
Input Limits <sup>3</sup>	$AVSS - 0.3$ $AVDD + 0.3$	$AVSS - 0.3$ $AVDD + 0.3$	V min V max
Input Capacitance	10	10	pF typ
Input Current	10	10	nA typ
AMPLIFIERS			
PGA Gain Range	1 5.98	1 5.98	V/V min V/V max
PGA Gain Resolution	256	256	Steps
Offset Range	-100 +100	-100 +100	mV min mV max
Offset Resolution	256	256	Steps
NOISE AND CROSSTALK			
Total Output Noise at Min PGA Gain <sup>4</sup>	0.5		LSB rms typ
Total Output Noise at Max PGA Gain <sup>4</sup>	0.8		LSB rms typ
Channel-to-Channel Crosstalk <sup>5</sup>	1		LSB max
POWER SUPPLY REJECTION			
( $AVDD = +5\text{ V} \pm 0.25\text{ V}$ )	0.28		% FSR max
VOLTAGE REFERENCE			
0.75 V Reference Tolerance (@ +25°C)	$\pm 20$		mV max
1.5 V Reference Tolerance (@ +25°C)	$\pm 34$		mV max
TEMPERATURE RANGE			
Operating	0 +70	0 +70	°C min °C max
POWER SUPPLIES			
Operating Voltages			
AVDD, DVDD	+4.75 +5.25	+4.75 +5.25	V min V max
DRVDD	+3.3 +5.25	+3.3 +5.25	V min V max
Operating Current	84	84	mA typ
POWER CONSUMPTION	420 500	420 500	mW typ mW max

### NOTES

<sup>1</sup>Includes internal voltage reference error.

<sup>2</sup>Input voltage range is the linear region over which the input signal can be processed by the input stage of the AD9816.

<sup>3</sup>The input limits are defined as the maximum tolerable input voltage into the AD9816. This is not intended to be the linear input range of the device. Signals beyond the input limits will turn on the overvoltage protection diodes.

<sup>4</sup>The total output noise is measured with the inputs of the AD9816 grounded.

<sup>5</sup>The channel-to-channel crosstalk is measured with one input grounded, and the other two inputs at full scale.

Specifications subject to change without notice.

## DIGITAL SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with AVDD = +5.0 V, DVDD = +5.0 V, DRVDD = +5.0 V, f<sub>ADCCLK</sub> = 6 MHz, f<sub>CDSCLK1</sub> = 2 MHz, f<sub>CDSCLK2</sub> = 2 MHz, C<sub>L</sub> = 10 pF unless otherwise noted)

Parameter	Symbol	Min	Typ	Max	Units
LOGIC INPUTS					
High Level Input Voltage	V <sub>IH</sub>	3.5			V
Low Level Input Voltage	V <sub>IL</sub>			1.0	V
High Level Input Current	I <sub>IH</sub>		10		μA
Low Level Input Current	I <sub>IL</sub>		10		μA
Input Capacitance	C <sub>IN</sub>		10		pF
LOGIC OUTPUTS					
High Level Output Voltage	V <sub>OH</sub>	4.5			V
Low Level Output Voltage	V <sub>OL</sub>			0.1	V
High Level Output Current	I <sub>OH</sub>		50		μA
Low Level Output Current	I <sub>OL</sub>		50		μA

Specifications subject to change without notice.

## TIMING SPECIFICATIONS (T<sub>MIN</sub> to T<sub>MAX</sub> with DVDD = +5.0 V, DRVDD = +5.0 V)

Parameter	Symbol	Min	Typ	Max	Units
CLOCK PARAMETERS					
3-Channel Conversion Rate	t <sub>CRA</sub>	500			ns
1-Channel Conversion Rate	t <sub>CRB</sub>	160			ns
ADCCLK Pulsewidth	t <sub>ADCLK</sub>	80			ns
CDSCLK1 Pulsewidth	t <sub>C1</sub>	20			ns
CDSCLK2 Pulsewidth	t <sub>C2</sub>	60		2 t <sub>ADCLK</sub> – 30	ns
CDSCLK1 Falling to CDSCLK2 Rising	t <sub>C1C2</sub>	5			ns
ADCCLK Falling to CDSCLK2 Rising	t <sub>ADC2</sub>	0			ns
CDSCLK2 Falling to ADCCLK Falling	t <sub>C2AD</sub>	30			ns
CDSCLK2 Falling to CDSCLK1 Rising	t <sub>C2C1</sub>	10			ns
Aperture Delay for CDS Clocks	t <sub>AD</sub>	10			ns
SERIAL INTERFACE					
Maximum SCLK Frequency	f <sub>SCLK</sub>	10			MHz
SLOAD to SCLK Set-Up Time	t <sub>LS</sub>	10			ns
SCLK to SLOAD Hold Time	t <sub>LH</sub>	10			ns
SDATA to SCLK Rising Set-Up Time	t <sub>DS</sub>	10			ns
SCLK Rising to SDATA Hold Time	t <sub>DH</sub>	10			ns
SCLK Falling to SDATA Valid	t <sub>RDV</sub>	10			ns
DATA OUTPUT					
Output Delay	t <sub>OD</sub>		13		ns
3-State to Data Valid	t <sub>DV</sub>		15		ns
Output Enable High to 3-State	t <sub>HZ</sub>		5		ns
Latency (Pipeline Delay)			3 (Fixed)		ADCCLK Cycles

# AD9816

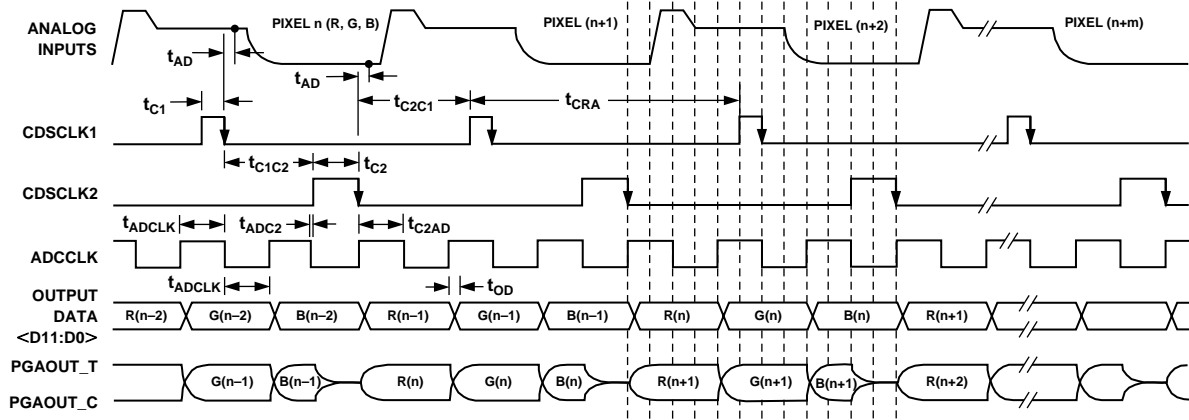


Figure 1. 3-Channel CDS Mode Timing

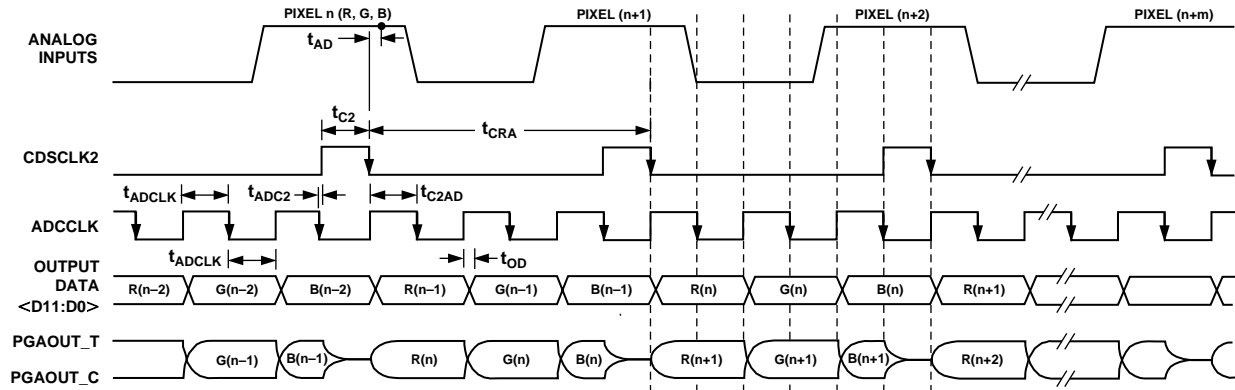


Figure 2. 3-Channel SHA Mode Timing

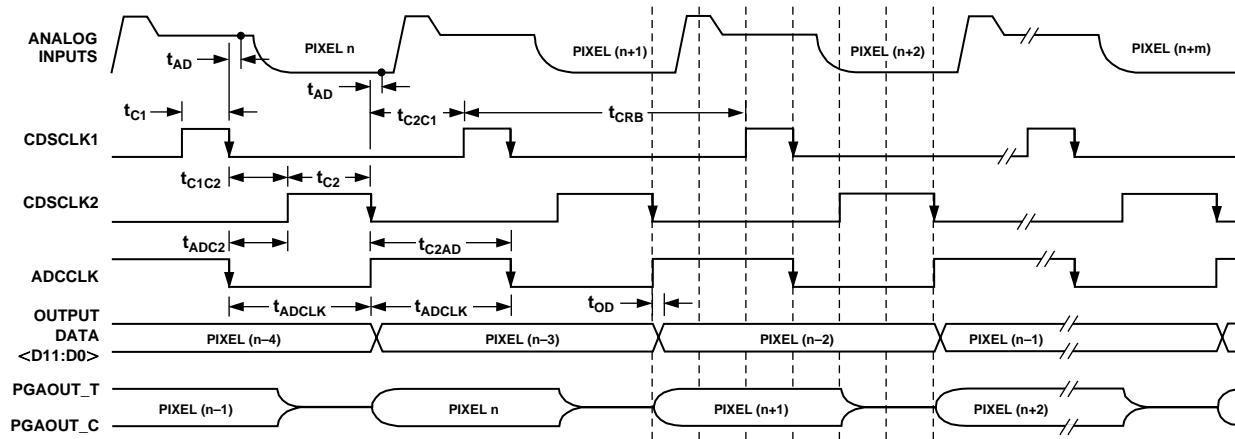


Figure 3. 1-Channel CDS Mode Timing

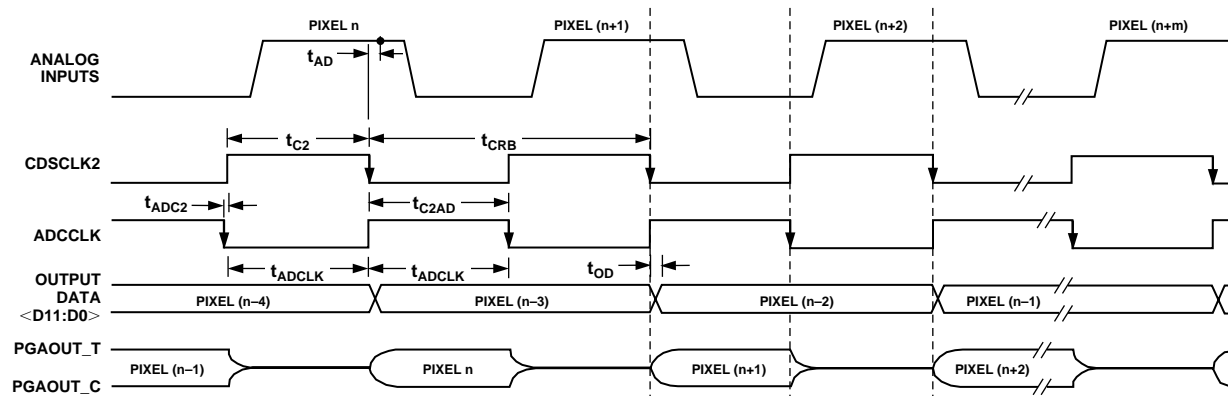


Figure 4. 1-Channel SHA Mode Timing

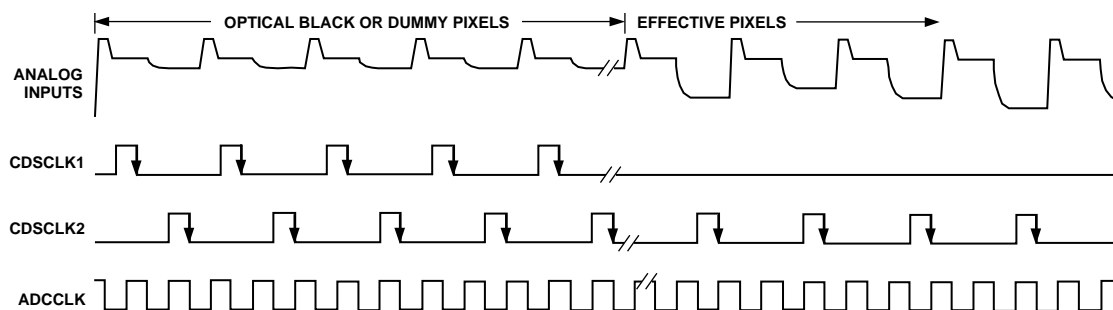


Figure 5. Line Clamp Timing for 3-Channel CDS Mode

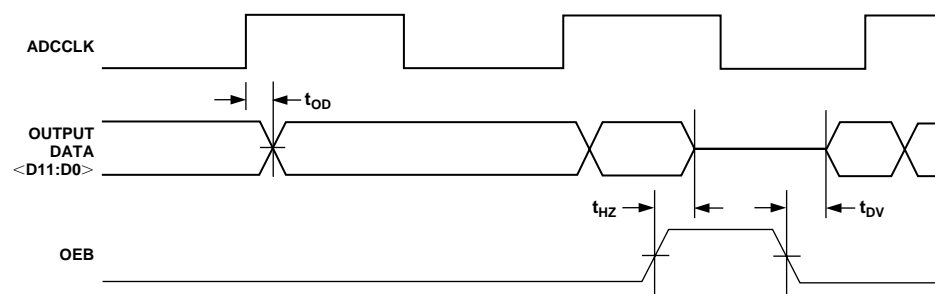


Figure 6. Output Enable Timing

# AD9816

## ABSOLUTE MAXIMUM RATINGS\*

Parameter	With Respect To	Min	Max	Units
VIN, VREF	AVSS	−0.3	AVDD + 0.3	V
PGA Outputs	AVSS	−0.3	AVDD + 0.3	V
Clock Inputs	DVSS	−0.3	DVDD + 0.3	V
AVDD	AVSS	−0.5	+6.5	V
DVDD	DVSS	−0.5	+6.5	V
DRVDD	DRVSS	−0.5	+6.5	V
AVSS	DVSS	−0.3	+0.3	V
Digital Outputs	DRVSS	−0.3	DRVDD + 0.3	V
Digital Inputs	DVSS	−0.3	DVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			+300	°C

\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9816JS	0°C to +70°C	44-Lead MQFP (Metric) Plastic Quad Flatpack	S-44
AD9816JS-80010	0°C to +70°C	44-Lead MQFP (Metric) Plastic Quad Flatpack	S-44
AD9816-EB		Evaluation Board	

## CAUTION

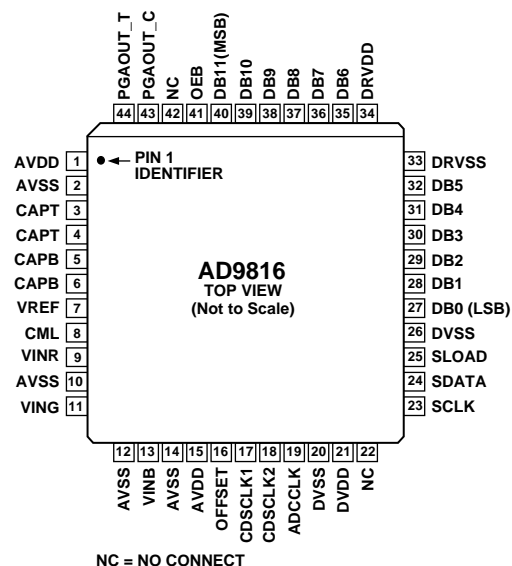
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9816 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN FUNCTION DESCRIPTIONS

Pin	Pin Name	Type	Description
1	AVDD	P	+5 V Analog Supply.
2	AVSS	P	Analog Ground.
3, 4	CAPT	AO	Reference Decoupling.
5, 6	CAPB	AO	Reference Decoupling.
7	VREF	AO	Internal Reference Output.
8	CML	AO	Internal Bias Level.
9	VINR	AI	Analog Input, Red Channel.
10	AVSS	P	Analog Ground.
11	VING	AI	Analog Input, Green Channel.
12	AVSS	P	Analog Ground.
13	VINB	AI	Analog Input, Blue Channel.
14	AVSS	P	Analog Ground.
15	AVDD	P	+5 V Analog Supply.
16	OFFSET	AI	Clamp bias level in CDS mode. Offset adjustment input in SHA mode.
17	CDSCLK1	DI	CDS Reset Level Sampling Clock.
18	CDSCLK2	DI	CDS Data Level Sampling Clock.
19	ADCCLK	DI	A/D Converter Sampling Clock.
20	DVSS	P	Digital Ground.
21	DVDD	P	+5 V Digital Supply.
22	NC		No Connect.
23	SCLK	DI	Clock Input for Serial Interface.
24	SDATA	DIO	Serial Data Input-Output.
25	SLOAD	DI	Load Pulse for Serial Interface.
26	DVSS	P	Digital Ground.
27	DB0	DO	Data Output (LSB).
28–32	DB1–DB5	DO	Data Outputs.
33	DRVSS	P	Digital Driver Ground.
34	DRVDD	P	Digital Driver Supply.
35–39	DB6–DB10	DO	Data Outputs.
40	DB11	DO	Data Output (MSB).
41	OEB	DI	Output Enable, Active Low.
42	NC		No Connect.
43	PGAOUT_C	AO	PGA Output, Negative. This pin should be left unconnected except during evaluation.
44	PGAOUT_T	AO	PGA Output, Positive. This pin should be left unconnected except during evaluation.

## PIN CONFIGURATION



## NOTES

See Applications Information for circuit configurations.

TYPE: AI = Analog Input, AO = Analog Output, DI = Digital Input,  
DO = Digital Output, DIO = Digital Input/Output, P = Power.

# AD9816

## DEFINITIONS OF SPECIFICATIONS

### INTEGRAL NONLINEARITY (INL)

Integral nonlinearity error refers to the deviation of each individual code from a line drawn from “zero scale” through “positive full scale.” The point used as “zero scale” occurs 1/2 LSB before the first code transition. “Positive full scale” is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

### DIFFERENTIAL NONLINEARITY (DNL)

An ideal ADC exhibits code transitions which are exactly 1 LSB apart. DNL is the deviation from this ideal value. Thus every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

### OFFSET ERROR

The first ADC code transition should occur at a level 1/2 LSB above the nominal zero scale voltage. The offset error is the deviation of the actual first code transition level from the ideal level.

### GAIN ERROR

The last code transition should occur for an analog value 1 1/2 LSB below the nominal full scale voltage. Gain error is the deviation of the *actual* difference between first and last code transitions and the *ideal* difference between the first and last code transitions.

### TOTAL OUTPUT NOISE

An ideal ADC outputs only one code value for a dc input voltage. A real converter has noise sources that will cause a spread of codes at the output for a dc input voltage. The total output noise is measured with a grounded input and is equal to the standard deviation of the histogram of output codes.

### CHANNEL-TO-CHANNEL CROSSTALK

In an ideal three-channel system, the signal in one channel will not influence the signal level of another channel. The channel-to-channel crosstalk specification is a measure of the change that occurs in one channel as the other two channels are varied. In the AD9816, one channel is grounded and the other two channels are exercised with full-scale input signals. The change in the output codes from the first channel is measured and compared with the result when all three channels are grounded. The difference is the channel-to-channel crosstalk, stated in LSBs.

### APERTURE DELAY

The aperture delay is the time delay that occurs from when a sampling edge is applied to the AD9816 until the actual sample of the input signal is held. For CDSCLK1, the aperture delay represents the amount of time it takes for the clamp switch to open after CDSCLK1 transitions from high to low. For CDSCLK2, the aperture delay is the amount of time after the CDSCLK2 falling edge that the input signal is sampled.

### POWER SUPPLY REJECTION

Power supply rejection specifies the maximum full-scale change that occurs from the initial value when the supplies are varied over the specified limits.

## FUNCTIONAL DESCRIPTION

The AD9816 can be operated in several different modes:

3-channel CDS mode, 3-channel SHA mode, 1-channel CDS mode, and 1-channel SHA mode. Each mode is selected by programming the Configuration Register through the serial interface. For more detail on CDS or SHA mode operation, see Circuit Descriptions section.

### 3-Channel CDS Mode

In 3-channel CDS mode, the AD9816 simultaneously samples the red, green and blue input voltages from the CCD outputs. The sampling points for each Correlated Double Sampler (CDS) are controlled by CDSCLK1 and CDSCLK2. CDSCLK1's falling edge clamps the reference level of the CCD waveform at the analog inputs of the AD9816. CDSCLK2's falling edge samples the data level of the CCD waveform. Each CDS amplifier outputs the difference between the CCD reference and data levels. Next, the output voltage of each CDS amplifier is level-shifted by an Offset DAC. The voltages are then scaled by the three Programmable Gain Amplifiers before being multiplexed to the common 12-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

Timing for this mode is shown in Figure 1, using a 2× master clock. Although it is not required, it is recommended that the falling edge of CDSCLK2 be aligned with the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by  $t_{ADC2}$ . The maximum allowable width of CDSCLK2 will be dependent on the ADCCLK period, and equal to one ADCCLK period minus 30 ns. The output data latency is three clock cycles.

The offset and gain values for the red, green, and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register. The rising edge of CDSCLK2 always resets the multiplexer.

### 3-Channel SHA Mode

In 3-channel SHA mode, the AD9816 simultaneously samples the red, green, and blue input voltages. The sample-and-hold amplifier's sampling point is controlled by CDSCLK2. CDSCLK2's falling edge samples the input waveforms on each channel. The output voltages from the three SHAs are modified by the offset DACs and then scaled by the three PGAs. The outputs of the PGAs are then multiplexed through the 12-bit ADC. The ADC sequentially samples the PGA outputs on the falling edges of ADCCLK.

The input signal is sampled with respect to the voltage applied to the OFFSET pin. With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero scale output. The input clamp is disabled in this mode. However, the OFFSET pin may be used as a coarse offset adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the red, green and blue inputs in the first amplifier stage of the AD9816. For more information, see the Circuit Descriptions section.

Timing for this mode is shown in Figure 2, using a 1× master clock. CDSCLK1 should be grounded in this mode. Although it is not required, it is recommended that the falling edge of CDSCLK2 be aligned with the rising edge of ADCCLK. The rising edge of CDSCLK2 should not occur before the previous falling edge of ADCCLK, as shown by  $t_{ADC2}$ . The maximum allowable width of CDSCLK2 will be dependent on the ADCCLK



period, and equal to one ADCCLK period minus 30 ns. The output data latency is three ADCCLK cycles.

The offset and gain values for the red, green and blue channels are programmed using the serial interface. The order in which the channels are switched through the multiplexer is selected by programming the MUX register. The rising edge of CDSCLK2 always resets the multiplexer.

## 1-Channel CDS Mode

This mode operates in the same way as the 3-channel CDS mode. The difference is that the multiplexer remains fixed in this mode, so only the channel specified in the MUX register is processed. Because the AD9816 is still sampling all three channels, the unused inputs should be grounded through 1200 pF capacitors.

Timing for this mode is shown in Figure 3, using a 3× master clock. Although it is not required, it is recommended that the falling edge of CDSCLK2 be aligned with the rising edge of ADCCLK.

## 1-Channel SHA Mode

This mode operates the same way as the 3-channel SHA mode, except that the multiplexer remains stationary. Only the channel specified in the MUX register is processed. Because the AD9816 is still sampling all three channels, the unused inputs should be grounded.

The input signal is sampled with respect to the voltage applied to the OFFSET pin. With the OFFSET pin grounded, a zero volt input corresponds to the ADC's zero scale output. The input clamp is disabled in this mode. However, the OFFSET pin may be used as a coarse offset adjust pin. A voltage applied to this pin will be subtracted from the voltages applied to the red, green and blue inputs in the first amplifier stage of the AD9816. For more information, see the Circuit Descriptions section.

Timing for this mode is shown in Figure 4, using a 1× master clock. CDSCLK1 should be grounded in this mode of operation. Although it is not required, it is recommended that the falling edge of CDSCLK2 be aligned with the rising edge of ADCCLK.

## REGISTER OVERVIEW

The serial interface is used to program the eight internal registers of the AD9816. The address bits A2–A0 determine the register in the AD9816 where serial data D7–D0 is written to or read from.

The Configuration Register controls the operating mode of the AD9816. Bits 7 (MSB), 6 and 0 are test mode bits and should always be set to zero. Bit 5 is set high to enable the CDS mode. Setting this bit low enables the SHA mode. Set Bit 4 high to enable the 3 V input span. Set Bit 3 high to enable the 1.5 V span. Bits 2 and 1 set the channel mode. Bit 2 enables 3-channel simultaneous sampling. Bit 1 enables single channel mode, with the appropriate channel set in the MUX Register. At power-on, this register defaults to 3-channel CDS mode with a 3 V input span, as shown in Table I.

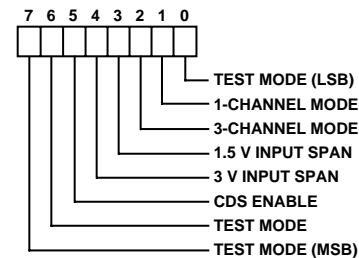


Figure 7. Configuration Register

The MUX Register determines the order of channels that the multiplexer will switch to in the different modes of operation. Bit 7 and Bit 1 are test modes and should be set to zero. Bit 0 is a test mode bit and should be set high. In 3-channel mode, Table II shows how to set the order in which the channels are converted. The multiplexer is always reset on the rising edge of CDSCLK2. In 1-channel mode, the multiplexer is stationary, and only converts the channel selected in Table III. At power-on, this register defaults to 3-channel RGB mode.

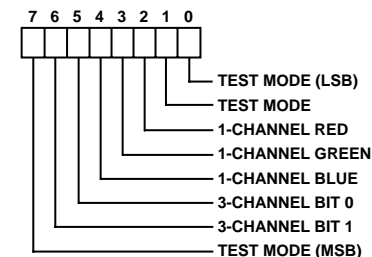


Figure 8. MUX Register

Table I. Register Map

A2	A1	A0	Register	Power-On Default Value
0	0	0	Configuration Register	0 0 1 1 0 1 0 0 (LSB)
0	0	1	MUX Register	0 0 1 0 0 0 0 1 (LSB)
0	1	0	Red PGA Register	Undetermined
0	1	1	Green PGA Register	Undetermined
1	0	0	Blue PGA Register	Undetermined
1	0	1	Red Offset Register	Undetermined
1	1	0	Green Offset Register	Undetermined
1	1	1	Blue Offset Register	Undetermined

# AD9816

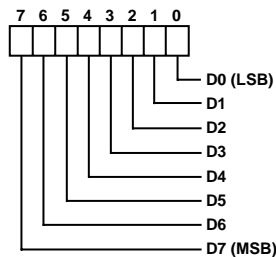
**Table II. 3-Channel Selection**

MUX Register Bits		Channel Sequence
6	5	
0	1	Red, Green, Blue
1	0	Blue, Green, Red

**Table III. 1-Channel Selection**

MUX Register Bits			Channel
4	3	2	
0	0	1	Red
0	1	0	Green
1	0	0	Blue

The offset is variable from  $-100\text{ mV}$  to  $+100\text{ mV}$ , and is applied at the output of the CDS, before the PGA. The resolution is 8 bits, and a sign magnitude coding scheme is used. Table IV shows the offset voltage that corresponds to the register value.



**Figure 9. Offset Registers for Red, Green and Blue Channels**

**Table IV. Offset Adjustment**

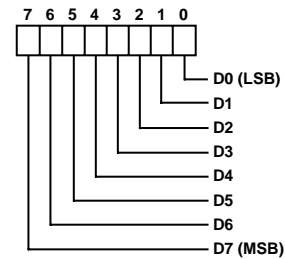
Offset Register	Offset Voltage
0111 1111 (LSB)	+100 mV
.	.
.	.
.	.
0000 0001	+0.8 mV
0000 0000	0.0 mV
1000 0000	0.0 mV
1000 0001	-0.8 mV
.	.
.	.
.	.
1111 1111	-100 mV

The PGA is used for correcting color imbalance and for fine adjustment of the input span before the ADC. Gain is variable from  $1\times$  to  $6\times$  (0 dB to 15.5 dB) with 8-bit resolution. An all “zeros” word (00 . . . 0) corresponds to the minimum gain, and an all “ones” word (11 . . . 1) corresponds to the maximum

gain. The gain of the PGA increases linearly as the gain word increases, and can be calculated by the following equation:

$$PGA\text{ Gain} = 1 + (\text{Gain Code}/51.2)$$

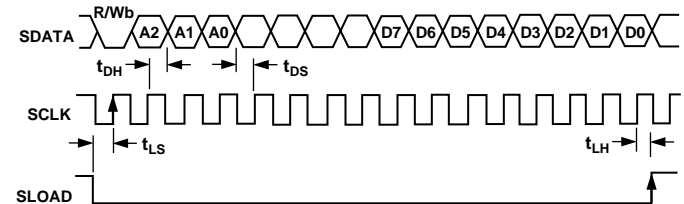
where *Gain Code* varies from 0 to 255. For more information, refer to the Circuit Descriptions section.



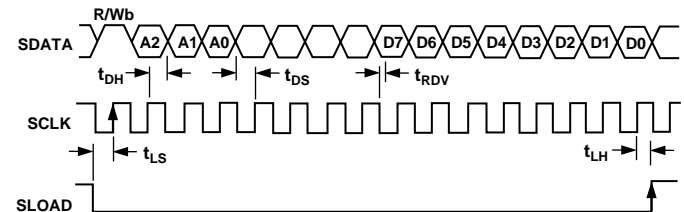
**Figure 10. PGA Registers for Red, Green and Blue Channels**

## SERIAL TIMING

The 3-wire serial interface timing is shown below. To write to the AD9816, SLOAD is first taken low. Next, a total of 16 bits are sent to SDATA, which get latched into the AD9816 on the rising edges of SCLK. Additional SCLK pulses will be ignored. The first bit,  $R/\overline{W}$ , should be low to specify a write operation. The next three bits, A2–A0, are the address bits to specify the destination register for the data word D7–D0. After all 16 bits have been clocked, SLOAD is taken high, which internally latches the data to the appropriate register. The read operation also starts by taking SLOAD low. First, a one is written to  $R/\overline{W}$ , to specify a read operation. Next, the three Address Bits A2–A0 are written to specify the register that will be read. On the 8th SCLK falling edge, SDATA will begin to output the information from the desired register. After all eight data bits have been read, SLOAD is taken back high.



**Figure 11. Write Operation Timing**



**Figure 12. Read Operation Timing**

## CIRCUIT DESCRIPTIONS

### Analog Input Configuration for CDS and SHA Mode

#### CDS Mode Operation

Figure 13 shows the equivalent input circuit for the CDS mode of operation. The CCD signal is connected to the AD9816's analog inputs through a coupling capacitor  $C_{IN}$ . The CCD reference level is clamped during the CDSCLK1 pulse, when the clamp switch closes and connects the externally-generated 3 V bias to the analog input. After the clamp switch opens (CDSCLK1 low), the CCD data level will be level shifted by the voltage held across  $C_{IN}$ , and the SHA will sample the input signal when the CDSCLK2 pulse goes low (see Figures 1 and 3 for CDS mode timing). In this sampling technique, the CDS function is effectively performed across the input capacitor,  $C_{IN}$ .

This CDS method has two additional considerations. First, the CCD signal cannot be dc-coupled into the AD9816, because the input capacitor is required. Second, the input clamp of the AD9816 is operating as a pixel clamp, and must be asserted on every pixel for true CDS operation. If line clamp operation is desired, CDSCLK1 may be used at the start of each line to set the proper dc voltage on  $C_{IN}$ . Then, during the effective pixels of each line, CDSCLK1 can be held low while CDSCLK2 samples the data levels of each pixel. Figure 5 shows the timing for line clamp operation.

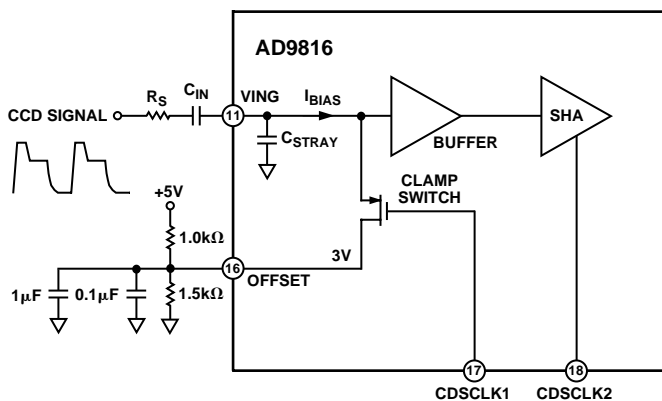


Figure 13. CDS Mode Input Circuit (All Channels Identical)

#### Input Signal Range for CDS Mode

An input dc bias level of 3 V allows a maximum 3 V p-p signal swing from the CCD. Figure 14 shows a typical full-scale input waveform to the AD9816, illustrating the allowable input range. With a reference level of 3 V, the AD9816 can tolerate up to 2 V of reset feedthrough above the reference level. The inputs

of the AD9816 can also handle an input signal down to  $AVSS - 0.3$  V without any saturation recovery issues. Although an input level below zero volts will be clipped to the ADC's full-scale output code, the input stage can respond quickly enough to accurately process the next pixel that falls into the linear input range. Any signals below  $AVSS - 0.3$  V will turn on the input protection diodes, and recovery from the saturated condition may take up to several milliseconds.

#### Input Capacitor $C_{IN}$

The recommended value for  $C_{IN}$  is 1200 pF. This value has been selected to provide the best overall performance when considering three factors: input attenuation, linearity and signal droop. The value of  $C_{IN}$  may be optimized for a particular application if these three factors are understood.

##### 1. Attenuation (Gain Error)

The input voltage will be attenuated by the interaction of  $C_{IN}$  and  $C_{STRAY}$ .  $C_{STRAY}$  is less than 10 pF, which results in an attenuation of about 0.8% when  $C_{IN}$  is 1200 pF. The gain error will increase accordingly as the value of  $C_{IN}$  is decreased.

##### 2. Linearity

The input capacitance of the AD9816 is shown in Figure 8 as  $C_{STRAY}$ . A small portion of this capacitance is junction capacitance, which will vary nonlinearly as the input voltage to the AD9816 changes. When the input voltage is attenuated by the combination of  $C_{IN}$  and  $C_{STRAY}$ , there will be a small nonlinear component caused by the input junction capacitance. The magnitude of the junction capacitance will cause a 1 LSB (0.024%) nonlinearity over the 3 V input range when a 1200 pF  $C_{IN}$  is used. This nonlinearity will increase if a smaller  $C_{IN}$  is used.

##### 3. Droop

The input bias current of the AD9816 is typically 10 nA and is constant regardless of the AD9816's input voltage. The droop of the voltage across  $C_{IN}$  can be calculated with the following equation:

$$dV = \frac{i_{BIAS}}{C_{IN}} \times (t)$$

where  $t$  is the time between clamp intervals. Between the adjacent pixels of a scanned line, this droop will be insignificant. Between scanned lines, a 1 ms delay will produce a droop of about 10 mV, which can be easily clamped on the first pixel of the next line. If the value of  $C_{IN}$  is reduced, the droop will increase accordingly.

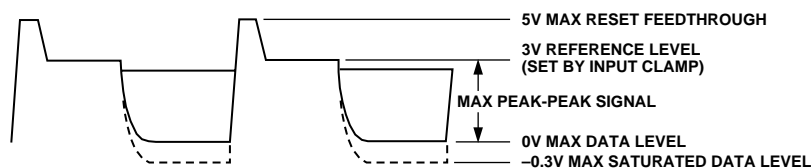


Figure 14. CCD Input Signal Clamped to 3 V

# AD9816

## Line Clamp

If a line clamp technique is implemented (see Figure 5 for timing), the value of  $C_{IN}$  should be increased to more than 1200 pF. The main requirement for line clamp is to keep the signal droop below 1 LSB across a scanned line. For example, if a CCD with 5400 effective pixels is clocked at 2 MHz, then  $t = 2.7$  ms. One LSB at 12 bits with a 3 V full scale is 732  $\mu$ V. Rearranging the above droop equation:

$$C_{MIN} = \frac{i_{BIAS}}{dV} \times t$$

In this case,  $C_{MIN} = 37$  nF, and a convenient standard value of 0.047  $\mu$ F will be adequate.

## SHA Mode Operation

When the AD9816 is configured for SHA mode operation, the OFFSET pin functions as an offset adjustment input. Figure 15 shows a simplified diagram of the AD9816's inputs when SHA mode is selected. A positive dc voltage may be applied to OFFSET which will be subtracted from all three input channels in the input stage of the AD9816. The maximum input voltage to the analog input pins or the OFFSET pin in SHA mode is 3 V.

The OFFSET feature is provided to allow coarse offset adjustment of the input signal. If the signal is sampled with respect to ground, any positive offset on the input signal will subtract from the dynamic range of the ADC. For example, an input signal that spans from 1.5 V to 2.5 V cannot utilize all of the available dynamic range, using either the 1.5 V or 3 V span. However, by applying a dc value of 1.5 V to the OFFSET pin, the input signal will be level-shifted down to 0 V to 1 V. This would allow the use of the 3 V span and a PGA gain of three to use the entire ADC dynamic range.

If no dc offset adjustment is desired, the OFFSET pin should be grounded. The input signal will be sampled with respect to ground.

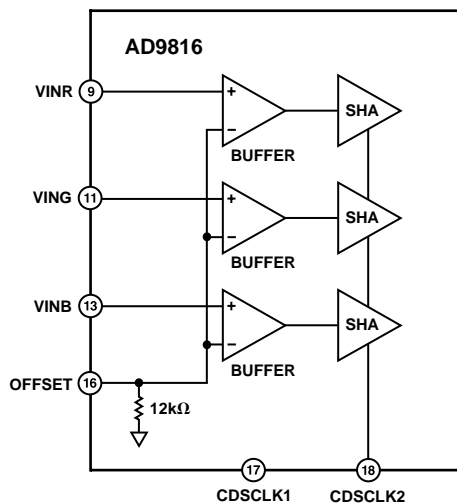


Figure 15. SHA Mode Input Circuit

## Programmable Gain Amplifiers

The AD9816 has three programmable amplifiers, one for each channel. The gain is variable from 1 V/V (0 dB) to 5.98 V/V (15.5 dB) in 256 increments. Figure 16 shows the PGA gain transfer function. The gain of the PGA can be calculated according to the equation:

$$PGA\ Gain = 1 + \left( \frac{Gain\ Code}{51.2} \right)$$

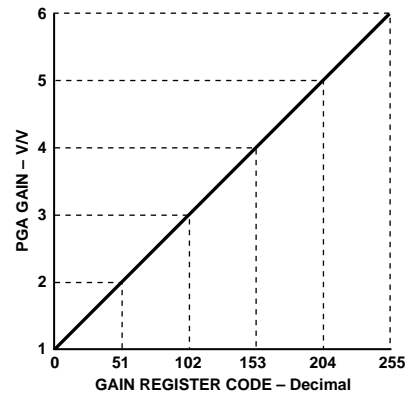


Figure 16. PGA Gain Transfer Function

The analog outputs of the three PGAs are multiplexed to the input of the 12-bit ADC. The differential output of the MUX is also buffered and externally available at Pins 43 and 44 (PGAOUT\_C and PGAOUT\_T, respectively). The timing diagrams, Figures 1 through 4, show the timing relationships between the analog inputs, CDSCLK2, ADCCLK, and PGAOUT\_T and PGAOUT\_C. The CDSCLK2 pulse resets the outputs of all three PGAs to an internal bias level. The first rising edge of ADCCLK after the rising edge of CDSCLK2 will switch the MUX to the red PGA output. The second ADCCLK rising edge switches the MUX to the green PGA output, and the third rising edge switches the MUX to the blue PGA output.

## PGA Outputs

The PGAOUT\_T and PGAOUT\_C signals represent the differential input to the ADC, and are complementary. Both signals will reset to 3.5 V while CDSCLK2 is high. The voltage swing of each output is equal to one-half of the ADC's full-scale voltage, centered at 3.5 V. Table V shows the relationship between the analog input voltage, the PGA output voltage and the ADC input voltage.

Figure 18 shows the PGA output voltages for three different color pixel amplitudes. In this example, the red pixel has the largest amplitude, and the blue pixel has the smallest amplitude. Because the PGAOUT\_T and PGAOUT\_C outputs are internally buffered by source followers, they are not an exact representation of the differential ADC input signal. PGAOUT\_T and PGAOUT\_C should only be used during evaluation; performance of the AD9816 is only guaranteed with these two pins unconnected.

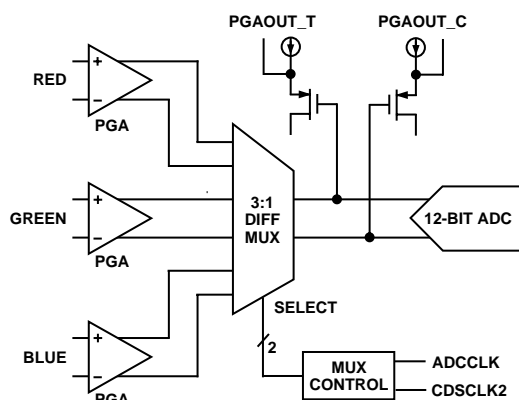


Figure 17. PGA/MUX Circuit Configuration

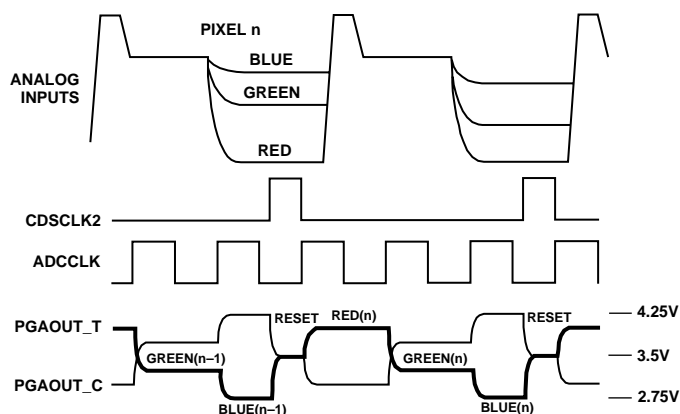


Figure 18. PGA Output Voltages (ADC Input Range = 3 V)

Table V. Voltage Swing of PGA Outputs

Analog Input Voltage <sup>1</sup>	PGAOUT_T	PGAOUT_C	Differential ADC Input
0.00 <sup>2</sup>	2.75	4.25	1.5
1.50 <sup>2</sup>	3.50	3.50	0.0
3.00 <sup>2</sup>	4.25	2.75	+1.5
0.00 <sup>3</sup>	3.125	3.875	0.75
0.75 <sup>3</sup>	3.50	3.50	0.0
1.50 <sup>3</sup>	3.875	3.125	+0.75

## NOTES

<sup>1</sup>Analog input voltage in CDS mode is the difference between the CCD's reference and data levels.

<sup>2</sup>3.0 V Input Range.

<sup>3</sup>1.5 V Input Range.

## Analog-to-Digital Converter

The AD9816 uses a high speed 12-bit ADC core. This CMOS converter is designed to run at 6 MSPS with good linearity and noise performance. Figure 19 shows the INL and DNL performance of a typical AD9816 device, running at 6 MHz in 3-channel CDS mode using the timing shown in Figure 1. The following timing parameters were used:  $t_{CRA} = 500$  ns,  $t_{ADCLK} = 83$  ns,  $t_{C1} = 20$  ns,  $t_{C1C2} = 170$  ns,  $t_{C1} = 80$  ns,  $t_{ADC2} = 3$  ns,  $t_{C2AD} = 83$  ns, and  $t_{C2C1} = 230$  ns.

The digital outputs of the AD9816 follow a straight binary coding scheme. Table VI shows the digital output coding for the 3 V input span.

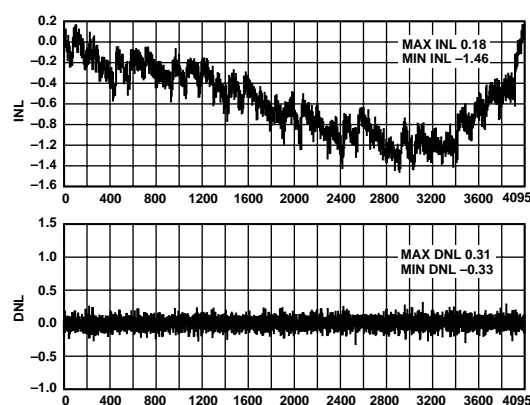


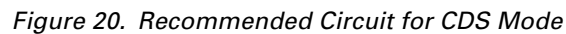
Figure 19. Typical Linearity Performance

Table VI. Digital Output Format

Input Voltage <sup>1</sup>	Digital Outputs
3.0 – 1 LSB	1111 1111 1111
3.0 – 2 LSB	1111 1111 1110
0.0 + 1 LSB	0000 0000 0001
0.0	0000 0000 0000

## NOTE

<sup>1</sup>Analog input voltage in CDS mode is the difference between the CCD's reference and data levels.



## SHA Mode Circuit

The circuit configuration for SHA mode is identical to CDS mode except for two differences: the analog inputs should be dc-coupled, and the OFFSET pin is tied to ground or a desired dc voltage (see Circuit Descriptions). In CIS applications, the

reference black level of the CIS can be connected to the OFFSET pin, to remove the dc offset. Removing the coarse offset of the CIS signal will allow the dynamic range of the AD9816 to be maximized.

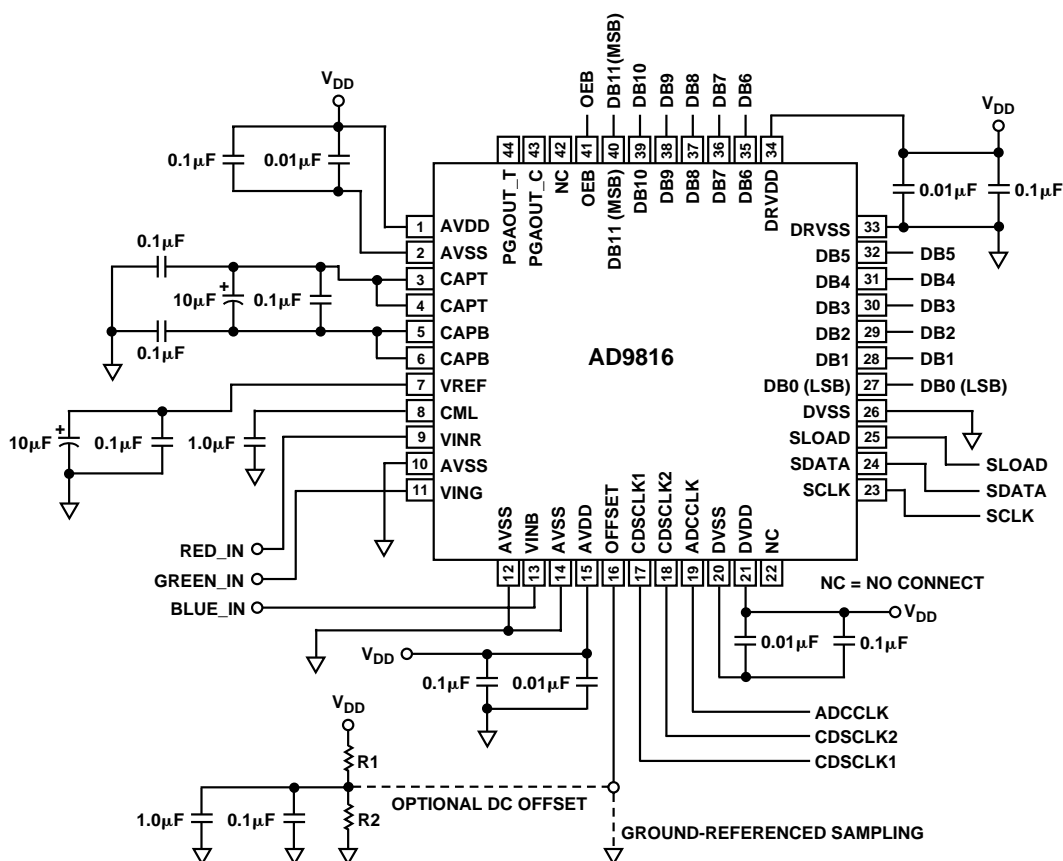


Figure 21. Recommended Circuit for SHA Mode

OUTLINE DIMENSIONS  
Dimensions shown in inches and (mm).

44-Lead MQFP  
(S-44)

