100/140/170/205 MSPS Analog Flat Panel Interface

AD9888

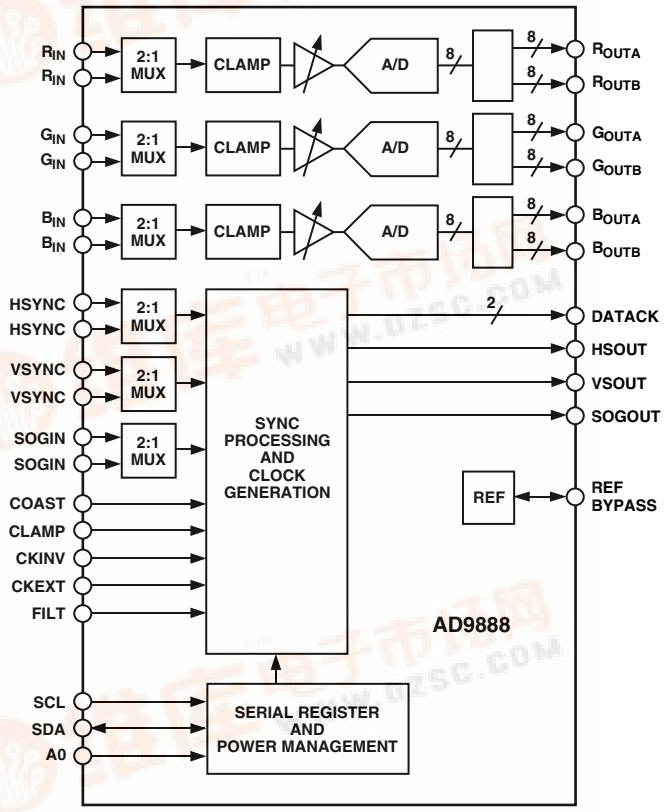
FEATURES

205 MSPS Maximum Conversion Rate
500 MHz Programmable Analog Bandwidth
0.5 V to 1.0 V Analog Input Range
Less than 450 ps p-p PLL Clock Jitter @ 205 MSPS
3.3 V Power Supply
Full Sync Processing
Sync Detect for "Hot Plugging"
2:1 Analog Input Mux
4:2:2 Output Format Mode
Midscale Clamping
Power-Down Mode
Low Power: <1 W Typical @ 205 MSPS

APPLICATIONS

RGB Graphics Processing
LCD Monitors and Projectors
Plasma Display Panels
Scan Converters
Microdisplays
Digital TV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9888 is a complete 8-bit, 205 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 205 MSPS encode rate capability and full-power analog bandwidth of 500 MHz supports resolutions up to UXGA (1600 × 1200 at 75 Hz).

For ease of design and to minimize cost, the AD9888 is a fully integrated interface solution for flat panel displays. The AD9888 includes an analog interface with a 205 MHz triple ADC with internal 1.25 V reference, PLL to generate a pixel clock from HSYNC and COAST, midscale clamping, and programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and HSYNC and COAST signals. Three-state CMOS outputs may be powered from 2.5 V to 3.3 V.

The AD9888's on-chip PLL generates a pixel clock from HSYNC and COAST inputs. Pixel clock output frequencies range from 10 MHz to 205 MHz. PLL clock jitter is less than 450 ps p-p typical at 205 MSPS. When the COAST signal is presented, the PLL maintains its output frequency in the absence of HSYNC. A sampling phase adjustment is provided. Data, HSYNC, and Clock output phase relationships are maintained. The PLL can be disabled and an external clock input provided as the pixel clock. The AD9888 also offers full sync processing for composite sync and Sync-on-Green applications.

A clamp signal is generated internally or may be provided by the user through the CLAMP input pin. This interface is fully programmable via a 2-wire serial interface.

Fabricated in an advanced CMOS process, the AD9888 is provided in a space-saving 128-lead MQFP surface mount plastic package and is specified over the 0°C to 70°C temperature range.

REV. A

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AD9888–SPECIFICATIONS (V_D = 3.3 V, V_{DD} = 3.3 V, ADC Clock = Maximum Conversion Rate)

Parameter	Temp	Test Level	AD9888KS-100/-140[1] Min	Typ	Max	AD9888KS-170 Min	Typ	Max	AD9888KS-205 Min	Typ	Max	Unit
RESOLUTION				8			8			8		Bits
DC ACCURACY												
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.6	+1.25/–1.0		±0.8	+1.50/–1.0	LSB
	Full	VI			+1.35/–1.0			+1.50/–1.0			+1.80/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±2.0		±0.75	±2.25		±1.0	±3.75	LSB
	Full	VI			±2.5			±2.75			±4.25	LSB
No Missing Codes	25°C	I		Guaranteed			Guaranteed			Guaranteed		
ANALOG INPUT												
Input Voltage Range												
Minimum	25°C	I			0.5			0.5			0.5	V p-p
Maximum	25°C	I	1.0			1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100			100		ppm/°C
Input Bias Current	25°C	IV			1			1			1	µA
	Full	IV			2			2			2	µA
Input Capacitance	Full	V		3			3			3		pF
Input Resistance	Full	IV	1			1			1			MΩ
Input Offset Voltage	Full	VI		7	90		7	90		7	90	mV
Input Full-Scale Matching	Full	VI		2.5	9.0		2.5	9.0		2.5	9.0	% FS
Offset Adjustment Range	Full	VI	44	49	53	44	49	53	44	49	53	% FS
REFERENCE OUTPUT												
Output Voltage	Full	VI	1.20	1.25	1.30	1.20	1.25	1.30	1.20	1.25	1.30	V
Temperature Coefficient	Full	V		±50			±50			±50		ppm/°C
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	100/140			170			205			MSPS
Minimum Conversion Rate	Full	IV			10			10			10	MSPS
Data to Clock Skew	Full	IV	–1.25		+1.25	–1.25		+1.25	–1.25		+1.25	ns
t_{BUFF}[2]	Full	VI	4.7			4.7			4.7			µs
t_{STAH}[2]	Full	VI	4.0			4.0			4.0			µs
t_{DHO}[2]	Full	VI	0			0			0			µs
t_{DAL}[2]	Full	VI	4.7			4.7			4.7			µs
t_{DAH}[2]	Full	VI	4.0			4.0			4.0			µs
t_{DSU}[2]	Full	VI	250			250			250			ns
t_{STASU}[2]	Full	VI	4.7			4.7			4.7			µs
t_{STOSU}[2]	Full	VI	4.0			4.0			4.0			µs
HSYNC Input Frequency	Full	IV	15		110	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	100/140			170			205			MHz
Minimum PLL Clock Rate	Full	IV			10			10			10	MHz
PLL Jitter	25°C	IV		470	700[3]		450	700[4]		440	700[4]	ps p-p
	Full	IV			1000[3]			1000[4]			1000[4]	ps p-p
Sampling Phase Tempco	Full	IV		15			15			15		ps/°C
DIGITAL INPUTS												
Input Voltage, High (V_{IH})	Full	VI	2.5			2.5			2.5			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8			0.8	V
Input Current, High (I_{IH})	Full	IV			–1.0			–1.0			–1.0	µA
Input Current, Low (I_{IL})	Full	IV			+1.0			+1.0			+1.0	µA
Input Capacitance	25°C	V		3			3			3		pF
DIGITAL OUTPUTS												
Output Voltage, High (V_{OH})	Full	VI	V_D – 0.1			V_D – 0.1			V_D – 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1		0	.1			0.1	V
Duty Cycle												
DATACK, $\overline{\text{DATACK}}$	Full	IV	44	49	55	44	49	55	44	49	55	%
Output Coding				Binary			Binary			Binary		
POWER SUPPLY												
V_D Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.6	2.2	3.3	3.6	2.2	3.3	3.6	V
P_{VD} Supply Voltage	Full	IV	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V
I_D Supply Current (V_D)	25°C	V		200			215			230		mA
I_{DD} Supply Current (V_{DD})[5]	25°C	V		50			55			60		mA
IP_{VD} Supply Current (P_{VD})	25°C	V		8			9			10		mA
Total Power Dissipation	Full	VI		850	1050		920	1150		990	1250	mW
Power-Down Supply Current	Full	VI		12	20		12	20		12	20	mA
Power-Down Dissipation	Full	VI		40	66		40	66		40	66	mW

Parameter	Temp	Test Level	AD9888KS-100/-140[1] Min	Typ	Max	AD9888KS-170 Min	Typ	Max	AD9888KS-205 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE												
Analog Bandwidth, Full Power[6]	25°C	V		500			500			500		MHz
Transient Response	25°C	V		2			2			2		ns
Overvoltage Recovery Time	25°C	V		1.5			1.5			1.5		ns
Signal-to-Noise Ratio (SNR)[7]	25°C	IV	42	45		41	44		40	42		dB
(Without Harmonics)	Full	V		44			43			41		dB
f_{IN} = 40.7 MHz												
Crosstalk	Full	V		50			50			50		dBc
THERMAL CHARACTERISTICS												
θ_{JC}–Junction-to-Case Thermal Resistance		V		8.4			8.4			8.4		°C/W
θ_{JA}–Junction-to-Ambient Thermal Resistance		V		35			35			35		°C/W

NOTES
[1]AD9888KS-100 specifications are tested at 100 MHz. AD9888KS-140 specifications are tested at 140 MHz.
[2]See Figure 23.
[3]VCO Range = 10, Charge Pump Current = 100, PLL Divider = 1693.
[4]VCO Range = 11, Charge Pump Current = 100, PLL Divider = 2159.
[5]DEMUX = 1, DATACK and $\overline{\text{DATACK}}$ Load = 15 pF, Data Load = 5 pF.
[6]Maximum bandwidth setting. Bandwidth can also be programmed to 300 MHz, 150 MHz, and 75 MHz.
[7]Using External Pixel Clock.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_D . . . . . 3.6 V
V_{DD} . . . . . 3.6 V
Analog Inputs . . . . . V_D to 0.0 V
VREF IN . . . . . V_D to 0.0 V
Digital Inputs . . . . . 5 V to 0.0 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –25°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . 150°C
Maximum Case Temperature . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9888KS-100	0°C to 70°C	S-128A
AD9888KS-140	0°C to 70°C	S-128A
AD9888KS-170	0°C to 70°C	S-128A
AD9888KS-205	0°C to 70°C	S-128A
AD9888/PCB	25°C	Evaluation Board

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9888 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

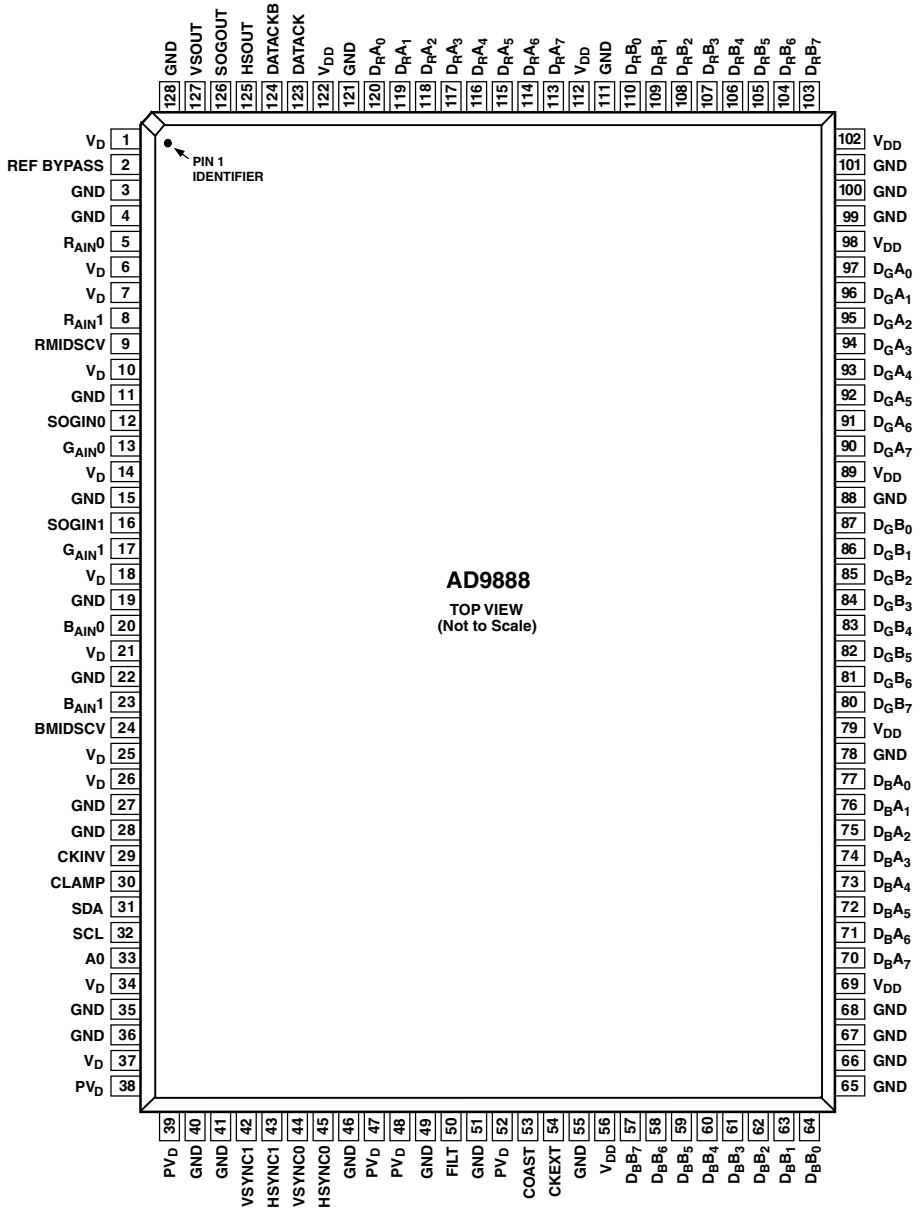


Table I. Complete Pinout List

Pin Type	Mnemonic	Function	Value	Pin Number
Analog Video Inputs	$R_{AIN}0$	Channel 0 Analog Input for Converter R	0.0 V to 1.0 V	5
	$G_{AIN}0$	Channel 0 Analog Input for Converter G	0.0 V to 1.0 V	13
	$B_{AIN}0$	Channel 0 Analog Input for Converter B	0.0 V to 1.0 V	20
	$R_{AIN}1$	Channel 1 Analog Input for Converter R	0.0 V to 1.0 V	8
	$G_{AIN}1$	Channel 1 Analog Input for Converter G	0.0 V to 1.0 V	17
	$B_{AIN}1$	Channel 1 Analog Input for Converter B	0.0 V to 1.0 V	23
Sync/Clock Inputs	HSYNC0	Channel 0 Horizontal SYNC Input	3.3 V CMOS	45
	VSYNC0	Channel 0 Vertical SYNC Input	3.3 V CMOS	44
	SOGIN0	Channel 0 Input for Sync-on-Green	0.0 V to 1.0 V	12
	HSYNC1	Channel 1 Horizontal SYNC Input	3.3 V CMOS	43
	VSYNC1	Channel 1 Vertical SYNC Input	3.3 V CMOS	42
	SOGIN1	Channel 1 Input for Sync-on-Green	0.0 V to 1.0 V	16
	CLAMP	Clamp Input (External CLAMP signal)	3.3 V CMOS	30
	COAST	PLL Coast Signal Input	3.3 V CMOS	53
	CKEXT	External Pixel Clock Input (to Bypass the PLL) or 10 kΩ to Ground	3.3 V CMOS	54
	CKINV	ADC Sampling Clock Invert	3.3 V CMOS	29
Sync Outputs	HSOUT	HSYNC Output Clock (Phase-Aligned with DATACK)	3.3 V CMOS	125
	VSOUT	VSYNC Output Clock (Phase-Aligned with DATACK)	3.3 V CMOS	127
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	126
Voltage	REF BYPASS	Internal Reference Bypass (Bypass with 0.1 µF to Ground)	1.25 V ± 10%	2
Clamp Voltages	$R_{MIDSC}V$	Red Channel Midscale Clamp Voltage Bypass		9
	$B_{MIDSC}V$	Blue Channel Midscale Clamp Voltage Bypass		24
PLL Filter	FILT	Connection for External Filter Components for Internal PLL		50
Power Supply	V_D	Analog Power Supply	3.3 V ± 10%	
	V_{DD}	Output Power Supply	3.3 V ± 10%	
	PV_D	PLL Power Supply	3.3 V ± 10%	
	GND	Ground	0 V	
Serial Port (2-Wire Serial Interface)	SDA	Serial Port Data I/O	3.3 V CMOS	31
	SCL	Serial Port Data Clock	3.3 V CMOS	32
	A0	Serial Port Address Input 1	3.3 V CMOS	33
Data Outputs	Red A[7:0]	Port A Outputs of Converter "Red," Bit 7 is the MSB.	3.3 V CMOS	113–120
	Red B[7:0]	Port B Outputs of Converter "Red," Bit 7 is the MSB.	3.3 V CMOS	103–110
	Green A[7:0]	Port A Outputs of Converter "Green," Bit 7 is the MSB.	3.3 V CMOS	90–97
	Green B[7:0]	Port B Outputs of Converter "Green," Bit 7 is the MSB.	3.3 V CMOS	80–87
	Blue A[7:0]	Port A Outputs of Converter "Blue," Bit 7 is the MSB.	3.3 V CMOS	70–77
	Blue B[7:0]	Port B Outputs of Converter "Blue," Bit 7 is the MSB.	3.3 V CMOS	57–64
Data Clock Output	DATACK	Data Output Clock	3.3 V CMOS	123
	$\overline{\text{DATACK}}$	Data Output Clock Complement	3.3 V CMOS	124

PIN FUNCTION DESCRIPTIONS

Pin	Description
Inputs	
$R_{AIN}0$	Channel 0 Analog Input for RED
$G_{AIN}0$	Channel 0 Analog Input for GREEN
$B_{AIN}0$	Channel 0 Analog Input for BLUE
$R_{AIN}1$	Channel 1 Analog Input for RED
$G_{AIN}1$	Channel 1 Analog Input for GREEN
$B_{AIN}1$	Channel 1 Analog Input for BLUE High-impedance inputs that accept the RED, GREEN, and BLUE channel graphics signals, respectively. (The six channels are identical and can be used for any colors; colors are assigned for convenient reference.) They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.
HSYNC0 HSYNC1	Channel 0 Horizontal Sync Input Channel 1 Horizontal Sync Input These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by serial register 0Eh Bit 6 (Hsync Polarity). Only the leading edge of Hsync is used by the PLL. The trailing edge is used for clamp timing only. When HSPOL = 0, the falling edge of Hsync is used. When HSPOL = 1, the rising edge is active. The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.
VSYNC0 VSYNC1	Channel 0 Vertical Sync Input Channel 1 Vertical Sync Input These are the inputs for vertical sync.
SOGIN0 SOGIN1	Channel 0 Sync-on-Green Input Channel 1 Sync-on-Green Input This input is provided to assist with processing signals with embedded sync, typically on the GREEN channel. The pin is connected to a high-speed comparator with an internally generated, variable threshold level, which is nominally set to 0.15 V above the negative peak of the input signal. When connected to an ac-coupled graphics signal with embedded sync, it will produce a noninverting digital output on SOGOUT. (This is usually a composite sync signal, containing both vertical and horizontal sync information.) When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green section.
CLAMP	External Clamp Input This logic input may be used to define the time during which the input signal is clamped to the reference dc level (ground for RGB or midscale for YUV). It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting the external clamp control (register 0Fh, Bit 7) to 1 (default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the HSYNC input. The logic sense of this pin is controlled by the clamp polarity control (register 0Fh, Bit 6). When not used, this pin must be grounded and external clamp programmed to 0.
COAST	Clock Generator Coast Input (Optional) This input may be used to cause the pixel clock generator to stop synchronizing with HSYNC and continue producing a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce horizontal sync pulses when in the vertical interval or that include equalization pulses. The Coast signal is usually *not* required for PC-generated signals. The logic sense of this pin is controlled by 0FH Bit 3 (Coast Polarity). When not used, this pin may be grounded and Coast Polarity programmed to 1, or tied HIGH (to V_D through a 10 kΩ resistor) and Coast Polarity programmed to 0. The Coast Polarity register bit defaults to 1 at power-up.
CKEXT	External Clock Input (Optional) This pin may be used to provide an external clock to the AD9888, in place of the clock internally generated from HSYNC. It is enabled by programming the External clock register to 1 (15H, Bit 0). When an external clock is used, all other internal functions operate normally. When unused, this pin should be tied through a 10 kΩ resistor to GROUND, and the External Clock register programmed to 0. The clock phase adjustment still operates when an external clock source is used.

PIN FUNCTION DESCRIPTIONS (continued)

Pin	Description
CKINV	Sampling Clock Inversion (Optional) This pin may be used to invert the pixel sampling clock, which has the effect of shifting the sampling phase 180°. This is in support of Alternate Pixel Sampling mode, wherein higher-frequency input signals (up to 410 Mpps) may be captured by first sampling the odd pixels, then capturing the even pixels on the subsequent frame. This pin should be exercised only during blanking intervals (typically vertical blanking) as it may produce several samples of corrupted data during the phase shift. CKINV should be grounded when not used.
Outputs	
D_RA_{7-0} D_RB_{7-0} D_GA_{7-0} D_GB_{7-0} D_BA_{7-0} D_BB_{7-0}	Data Output, Red Channel, Port A Data Output, Red Channel, Port B Data Output, Green Channel, Port A Data Output, Green Channel, Port B Data Output, Blue Channel, Port A Data Output, Blue Channel, Port B These are the main data outputs. Bit 7 is the MSB. Each channel has two ports. When the part is operated in single-channel mode (Channel Mode bit (15H, Bit 7) = 0), all data are presented to Port A, and Port B is placed in a high-impedance state. Programming the Channel Mode bit to 1 establishes dual-channel mode, wherein alternate pixels are presented to Port A and Port B of each channel. These will appear simultaneously; two pixels are presented at the time of every second input pixel, when the Output Mode bit (15H, Bit 6) is set to 1 (parallel mode). When the Output Mode bit is set to 0, pixel data appear alternately on the two ports, one new sample with each incoming pixel (interleaved mode). In dual-channel mode, the first pixel after HSYNC is routed to Port A. The second pixel goes to Port B, the third to A, etc. This can be reversed by setting the A/B Invert bit to 1 (15H, Bit 5). The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The DATACK, $\overline{\text{DATACK}}$ and HSOUT outputs are also moved, so the timing relationship among the signals is maintained.
DATACK $\overline{\text{DATACK}}$	Data Output Clock Data Output Clock Complement Differential data clock output signals to be used to strobe the output data and HSOUT into external logic. They are produced by the internal clock generator and are synchronous with the internal pixel sampling clock. When the AD9888 is operated in single-channel mode, the output frequency is equal to the pixel sampling frequency. When operating in dual-channel mode, the clock frequency is one-half the pixel frequency, as is the output data frequency. When the sampling time is changed by adjusting the PHASE register, the output timing is shifted as well. The Data, DATACK, $\overline{\text{DATACK}}$ and HSOUT outputs are all moved, so the timing relationship among the signals is maintained. Either or both signals may be used, depending on the timing mode and interface design employed.
HSOUT	Horizontal Sync Output A reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK, $\overline{\text{DATACK}}$, and Data, data timing with respect to horizontal sync can always be determined.
SOGOUT	Sync-On-Green Slicer Output This pin can be programmed to output either the output from the Sync-On-Green slicer comparator or an unprocessed but delayed version of the Hsync input. See the Sync Processing Block Diagram (Figure 25) to view how this pin is connected. (Note: Besides slicing off SOG, the output from this pin gets no other additional processing on the AD9888. Vsync separation is performed via the sync separator.)
REF BYPASS	Internal Reference BYPASS Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1 µF capacitor. The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9888 applications. If higher accuracy is required, an external reference may be employed instead.
RMIDSCV BMIDSCV	RED Channel Midscale Voltage BYPASS BLUE Channel Midscale Voltage BYPASS Bypasses for the internal midscale voltage references. They should each be connected to ground through 0.1 µF capacitors. The exact voltage varies with the gain setting of the BLUE channel.

PIN FUNCTION DESCRIPTIONS (continued)

Pin	Description
FILT	External Filter Connection For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 6 to this pin. For optimal performance, minimize noise and parasitics on this node.
Power Supply	
V_D	Main Power Supply These pins supply power to the main elements of the circuit. It should be as quiet and filtered as possible.
V_{DD}	Digital Output Power Supply A large number of output pins (up to 52) switching at high speed (up to 110 MHz) generates a lot of power supply transients (noise). These supply pins are identified separately from the V_D pins, so special care can be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9888 is interfacing with lower voltage logic, V_{DD} may be connected to a lower supply voltage (as low as 2.5 V) for compatibility.
PV_D	Clock Generator Power Supply The most sensitive portion of the AD9888 is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide "quiet," noise-free power to these pins.
GND	Ground The ground return for all circuitry on chip. It is recommended that the AD9888 be assembled on a single solid ground plane, with careful attention to ground current paths.
Serial Port (2-Wire)	
SDA	Serial Port Data I/O
SCL	ISerial Port Data Clock
A0	Serial Port Address Input 1

For a full description of the 2-wire serial register and how it works, refer to the Control Register section.

DESIGN GUIDE

General Description

The AD9888 is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The circuit is ideal for providing a computer interface for HDTV monitors or as the front-end to high-performance video scan converters.

Implemented in a high-performance CMOS process, the interface can capture signals with pixel rates of up to 205 MHz, and with an Alternate Pixel Sampling mode, up to 340 MHz.

The AD9888 includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 650 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

Input Signal Handling

The AD9888 has six high-impedance analog input pins for the red, green, and blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or via BNC connectors. The AD9888 should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At that point, the signal should be resistively terminated (to the signal ground return) and capacitively coupled to the AD9888 inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The ultrawide bandwidth inputs of the AD9888 (500 MHz) can track the input signal continuously as it moves from one pixel level to the next, and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. The AD9888 can digitize graphics signals over a very wide range of frequencies (10 MHz to 205 MHz). Often characteristics that are beneficial at one frequency can be detrimental at another. Analog bandwidth is one such characteristic. For UXGA resolutions (up to 205 MHz), a very high analog bandwidth is desirable because of the fast input signal slew rates. For VGA and lower resolutions (down to 12.5 MHz), a very high bandwidth is not desirable, because it allows excess noise to pass through. To accommodate these varying needs, the AD9888 includes variable analog bandwidth control. Four settings are available (75 MHz, 150 MHz, 300 MHz, and 500 MHz), allowing the analog bandwidth to be matched with the resolution of the incoming graphics signal.

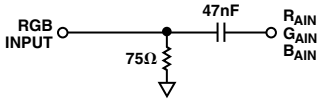


Figure 1. Analog Input Interface Circuit

Sync Processing
The AD9888 contains circuitry that enables it to accept composite sync inputs, such as Sync-on-Green or the trilevel syncs found in digital TV signals. A complete description of the sync processing functionality is found in the Sync Slicer and Sync Separator sections.

Hsync, Vsync Inputs
The interface also takes a horizontal sync signal, which is used to generate the pixel clock and clamp timing. It is possible to operate the AD9888 without applying Hsync (using an external clock, external clamp, and single port output mode) but a number of features of the chip will be unavailable, so it is recommended that Hsync be provided. This can be either a sync signal directly from the graphics source, or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires in the monitor cable. As such, no termination is required or desired.

Serial Control Port
The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

Output Signal Handling
The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

Clamping
RGB Clamping
To digitize the incoming signal properly, the dc offset of the input must be adjusted to fit the range of the on-board A/D converters.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground and black is at 300 mV. Then white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9888.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced which results in the A/D converters producing a black output (code 00h) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most graphics systems, black is transmitted between active video lines. Going back to CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is almost always a period following Hsync called the back porch where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time (with External Clamp = 1). The polarity of this signal is set by the Clamp Polarity (Register 0Fh, Bit 6).

A simpler method of clamp timing employs the AD9888 internal clamp timing generator. The Clamp Placement register is programmed with the number of pixel times that should pass after the trailing edge of HSYNC before clamping starts. A second register (Clamp Duration, Register 06h) sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync because, though Hsync duration can vary widely, the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 08h (providing 8 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 14h (giving the clamp 20 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there will be a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it will take excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovering from a step error of 100 mV to within 1/2 LSB in 10 lines with a clamp duration of 20 pixel periods on a 60 Hz SXGA signal.

YUV Clamping
YUV graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) can be at the midpoint of the video signal rather than the bottom. For these signals it can be necessary to clamp to the midscale range of the A/D converter range (80h) rather than bottom of the A/D converter range (00h).

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the series bus register. The red and blue channels each have their own selection bit so that they can be clamped to either midscale or ground independently. The clamp controls are located in register 10h and are Bits 1 and 2. The midscale reference voltage that each A/D converter clamps to is provided independently on the RMIDSCV and BMIDSCV pins. These two pins should be bypassed to ground with a 0.1 μF capacitor (even if midscale clamping is not required).

Gain and Offset Control
The AD9888 can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (Red Gain, Green Gain, and Blue Gain; Registers 08h, 09h, and 10h respectively).

Note that *increasing* the gain setting results in an image with *less* contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (Red Offset, Green Offset, Blue Offset; Registers 0Bh, 0Ch, and 0Dh respectively) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 2 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale *range* is not affected, but the full-scale *level* is shifted by the same amount as the zero-scale level.

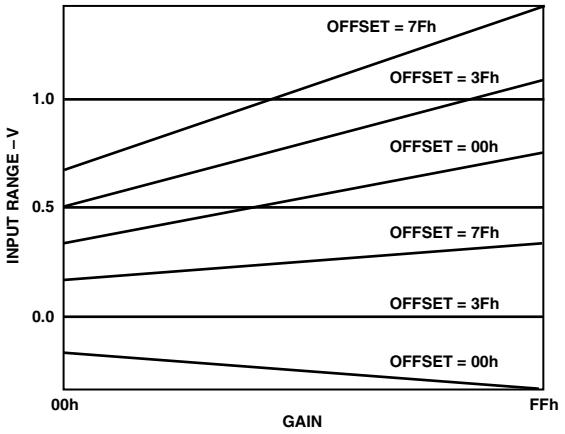


Figure 2. Gain and Offset Control

Sync-on-Green

The Sync-on-Green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via register 11H. The Sync-on-Green input must be ac-coupled to the green analog input through its own capacitor as shown in Figure 3. The value of the capacitor must be 1 nF ± 20%. If Sync-on-Green is not used, this connection is not required and the SOGIN pin should be left unconnected. (Note: the Sync-on-Green signal is always negative polarity.) For more details, see the Sync Processing section.

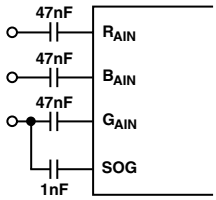


Figure 3. Typical Clamp Configuration for RGB/YUV Applications

Clock Generation

A Phase Locked Loop (PLL) is employed to generate the pixel clock. The Hsync input provides a reference frequency to the PLL. A Voltage Controlled Oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (registers 01H and 02H) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 4). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

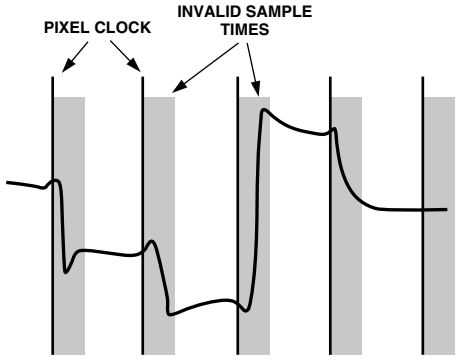


Figure 4. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined, and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9888's clock generation circuit to minimize jitter. As indicated in Figure 5, the clock jitter of the AD9888 is less than 9% of the total pixel time in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

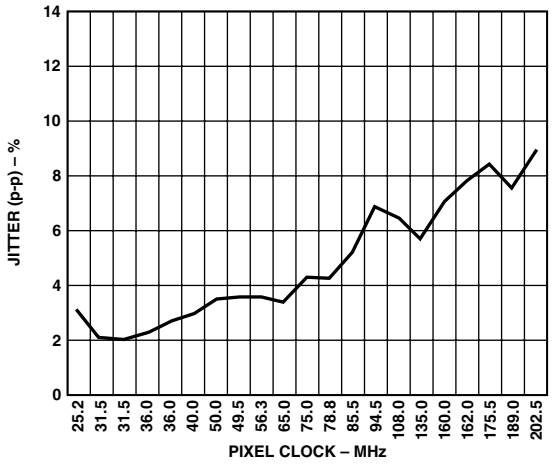


Figure 5. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, by the PLL Charge Pump Current and by the VCO range setting. The loop filter design is illustrated in Figure 6. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table IV.

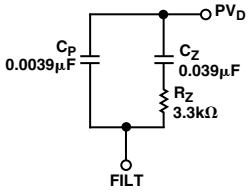


Figure 6. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are:

1. The 12-Bit Divisor Registers. The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 205 MHz. The Divisor Register controls the exact multiplication factor. This register may be set to any value between 221 and 4095. (The divide ratio that is actually used is the programmed divide ratio plus one.)
2. The 2-Bit VCO Range Register. To lower the sensitivity of the output frequency to noise on the control signal, the VCO operating frequency range is divided into four overlapping regions. The VCO Range register sets this operating range. Because there are only four possible regions, only the two least significant bits of the VCO Range register are used. The frequency ranges for the lowest and highest regions are shown in Table II.
3. The 3-Bit Charge Pump Current Register. This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table III.

Table II. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	K_{VCO} Gain (MHz/V)
0	0	10–45	22.5
0	1	45–90	45
1	0	90–150	90
1	1	150+	180

Table III. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

Table IV. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	VCORNGE	Current
VGA	640 × 480	60	31.5	25.175	00	010
		72	37.7	31.500	00	100
		75	37.5	31.500	00	100
		85	43.3	36.000	00	100
SVGA	800 × 600	56	35.1	36.000	00	100
		60	37.9	40.000	00	101
		72	48.1	50.000	01	011
		75	46.9	49.500	01	011
		85	53.7	56.250	01	011
XGA	1024 × 768	60	48.4	65.000	01	100
		70	56.5	75.000	01	100
		75	60.0	78.750	01	101
		80	64.0	85.500	01	101
		85	68.3	94.500	10	011
SXGA	1280 × 1024	60	64.0	108.000	10	011
		75	80.0	135.000	10	100
		85	91.1	157.500	11	100
UXGA	1600 × 1200	60	75.0	162.000	11	100
		65	81.3	175.500	11	100
		70	87.5	189.000	11	101
		75	93.8	202.500	11	101
		85	106.3	229.500*	10	110
QXGA	2048 × 1536	60		260.000*	11	100
	2048 × 1536	75		315.000*	11	100

*Graphics sampled at 1/2 the incoming pixel rate using Alternate Pixel Sampling mode.

4. The 5-Bit Phase Adjust Register. The phase of the generated sampling clock may be shifted to locate an optimum sampling point within a clock cycle. The Phase Adjust Register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjustment is still available if the pixel clock is being provided externally.

   The COAST pin is used to allow the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal. This may be used during the vertical sync period, or any other time that the Hsync signal is unavailable. The polarity of the COAST signal may be set through the COAST Polarity Register. Also, the polarity of the Hsync signal may be set through the Hsync Polarity Register.

Alternate Pixel Sampling Mode

A Logic 1 input on Clock Invert (CKINV, Pin 29) inverts the nominal ADC clock. CKINV can be switched between frames to implement the alternate pixel sampling mode. This allows higher effective image resolution to be achieved at lower pixel rates but with lower frame rates.

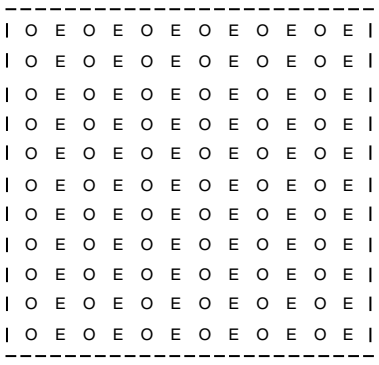


Figure 7. Odd and Even Pixels in a Frame

On one frame, only even pixels are digitized. On the subsequent frame, odd pixels are sampled. By reconstructing the entire frame in the graphics controller, a complete image can be reconstructed. This is similar to the interlacing process that is employed in broadcast television systems, but the interlacing is vertical instead of horizontal. The frame data is still presented to the display at the full desired refresh rate (usually 60 Hz) so there are no flicker artifacts added.

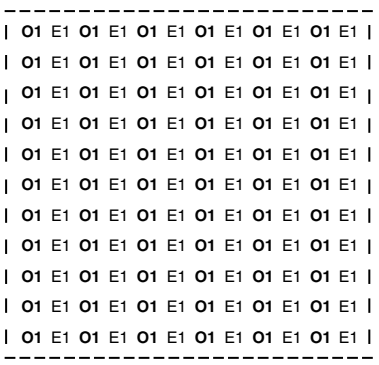


Figure 8. Odd Pixels from Frame 1

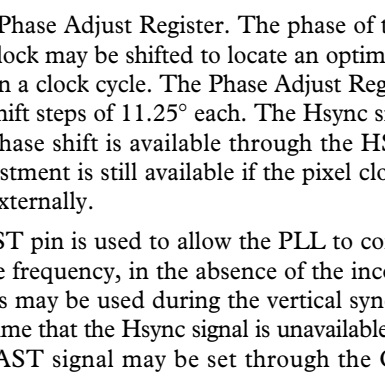


Figure 9. Even Pixels from Frame 2

Figure 10. Combined Frame Output from Graphics Controller

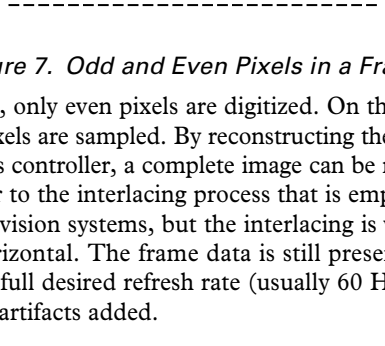


Figure 11. Subsequent Frame from Controller

TIMING

The following timing diagrams show the operation of the AD9888 analog interface in all clock modes. The part establishes timing by having the sample that corresponds to the pixel digitized when the leading edge of Hsync occurs sent to the "A" data port. In dual-channel mode, the next sample is sent to the "B" port. Future samples are alternated between the "A" and "B" data ports. In single-channel mode, data is only sent to the "A" data port, and the "B" port is placed in a high impedance state.

The Output Data Clock signal is created so that its rising edge always occurs between "A" data transitions, and can be used to latch the output data externally.

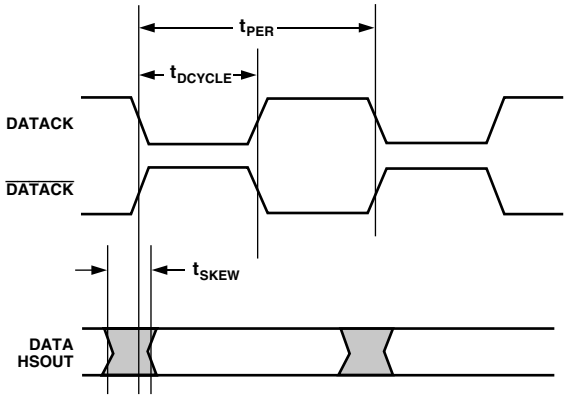


Figure 12. Output Timing

Hsync Timing

Horizontal sync is processed in the AD9888 to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the Phase Adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Horizontal Sync in the AD9888. First, the polarity of Hsync input is determined and will thus have a known output polarity. The known output polarity can be programmed either active high or active low (Register 0EH, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via register 07H. HSOUT is the sync signal that should be used to drive the rest of the display system.

COAST Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary, and should not be used.

In some systems, however, Hsync is disturbed during the Vertical Sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ Composite Sync (Csync) signals or embedded Sync-On-Green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it will attempt to lock to this new frequency, and will have changed frequency by the end of the Vsync period. It will then take a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a "tearing" of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

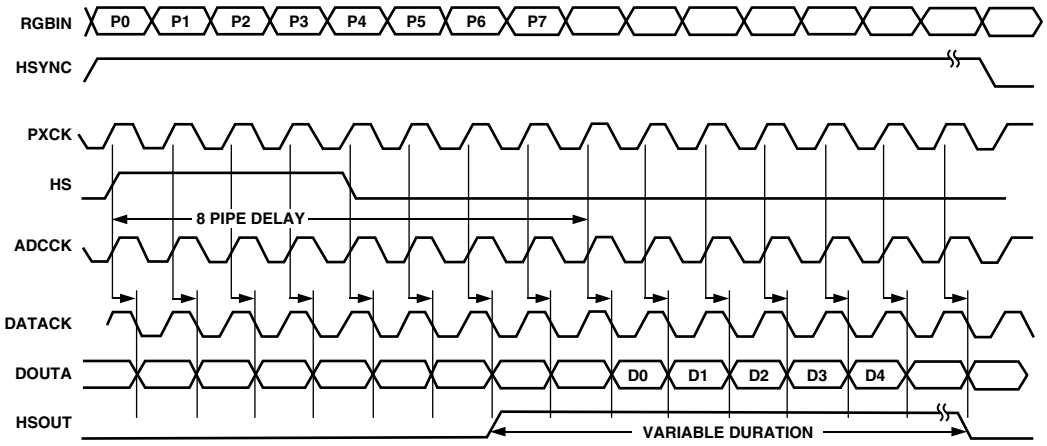


Figure 13. Single-Channel Mode

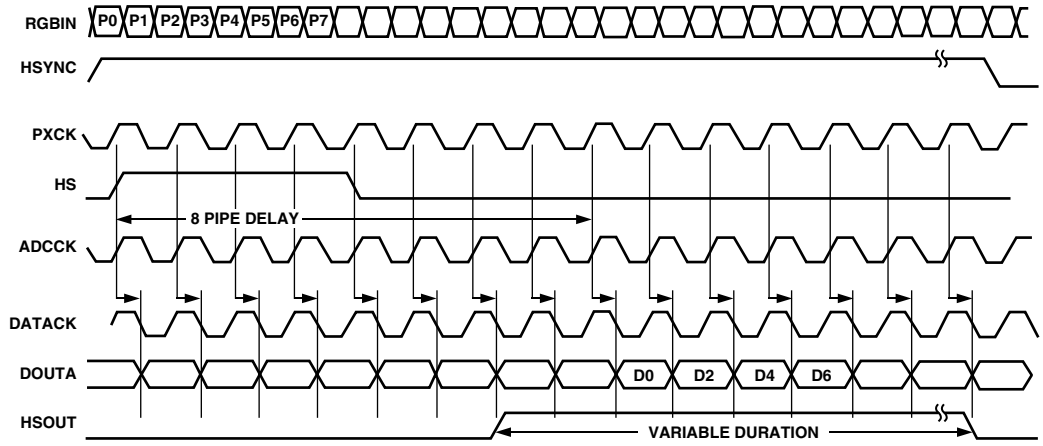


Figure 14. Single-Channel Mode, Two Pixels/Clock (Even Pixels)

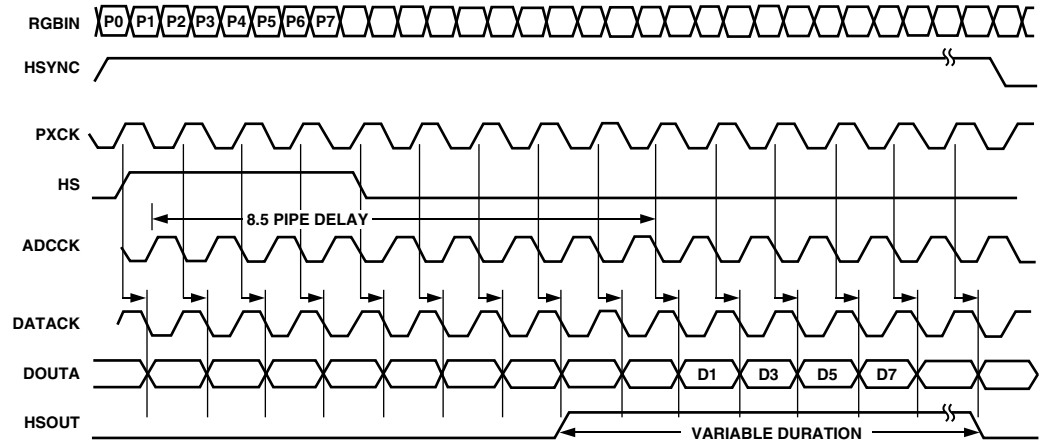


Figure 15. Single-Channel Mode, Two Pixels/Clock (Odd Pixels)

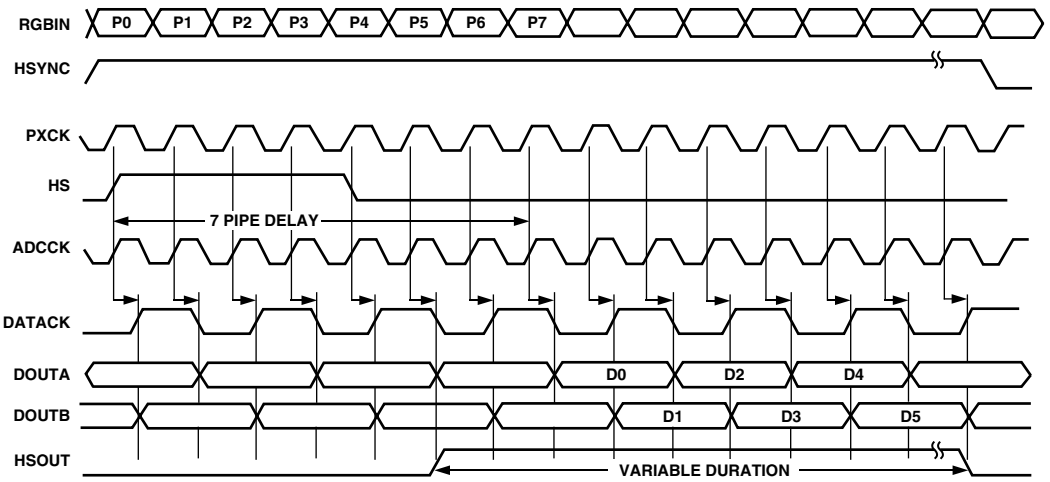


Figure 16. Dual-Channel Mode, Interleaved Outputs

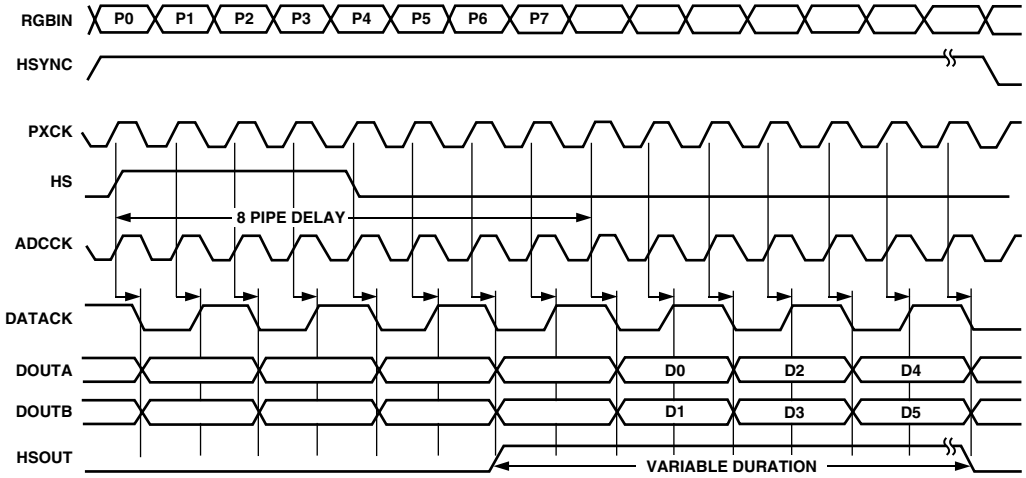


Figure 17. Dual-Channel Mode, Parallel Outputs

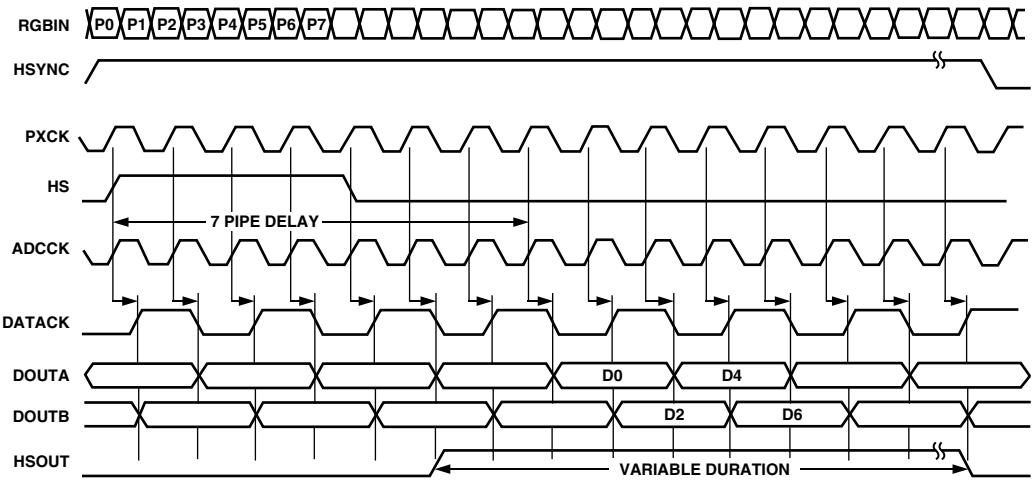


Figure 18. Dual-Channel Mode, Interleaved Outputs, Two Pixels/Clock (Even Pixels)

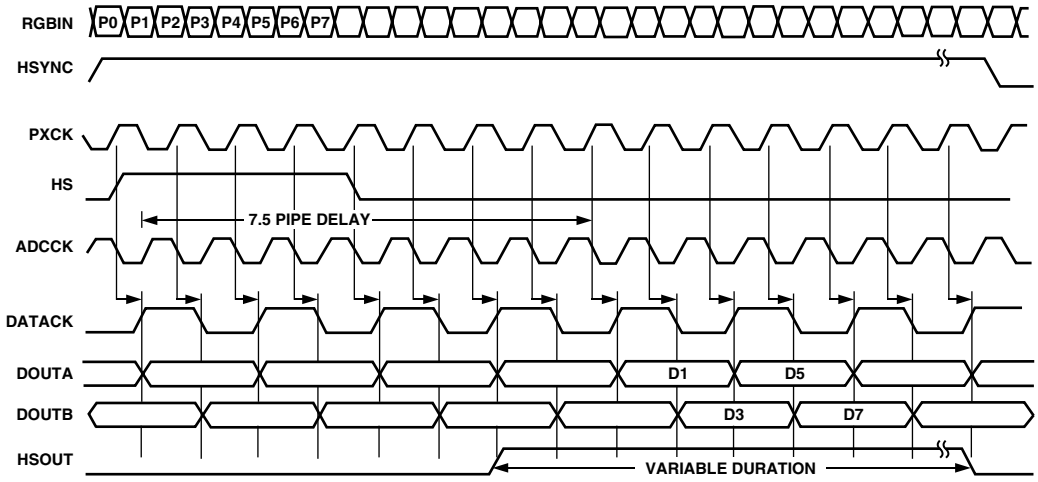


Figure 19. Dual-Channel Mode, Interleaved Outputs, Two Pixels/Clock (Odd Pixels)

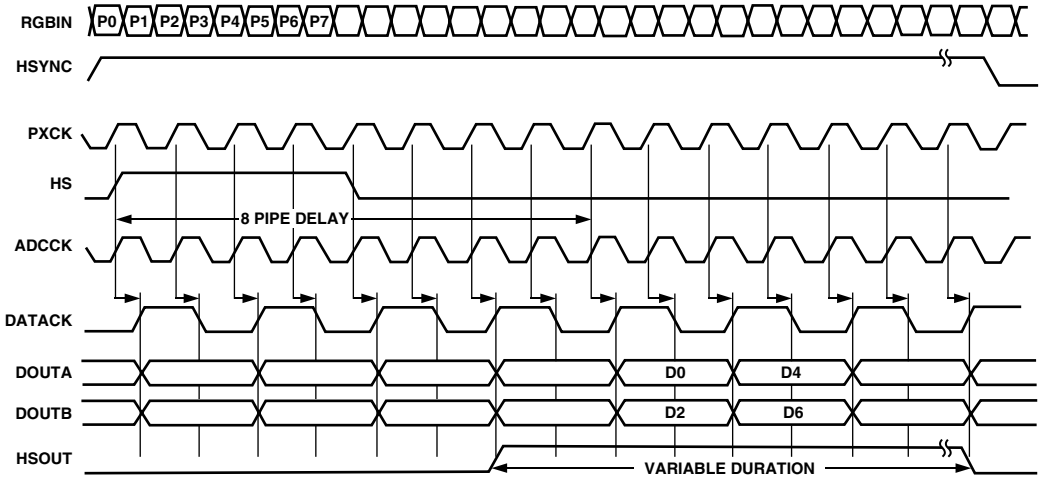


Figure 20. Dual-Channel Mode, Parallel Outputs, Two Pixels/Clock (Even Pixels)

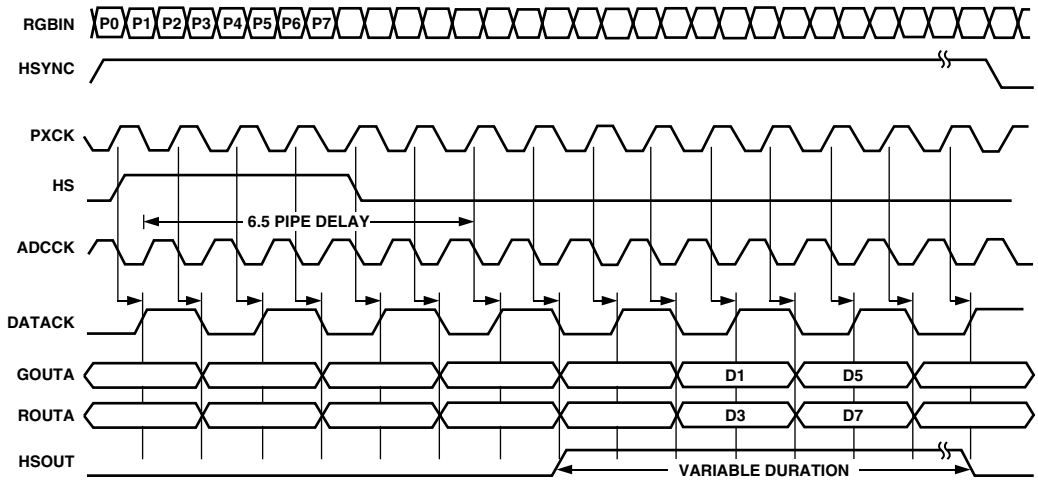


Figure 21. Dual-Channel Mode, Parallel Outputs, Two Pixels/Clock (Odd Pixels)

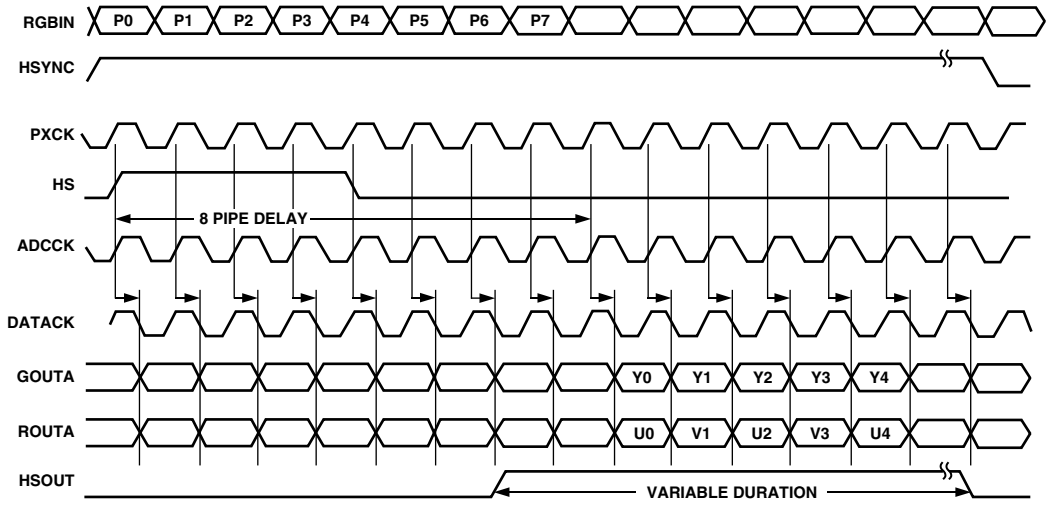


Figure 22. 4:2:2 Output Mode

2-WIRE SERIAL REGISTER MAP

The AD9888 is initialized and controlled by a set of registers, which determine the operating modes. An external controller is employed to write and read the Control Registers through the 2-line serial interface port.

Table V. Control Register Map

Hex Address	Read and Write or Read Only	Bits	Default Value	Register Name	Function
00H	RO	7:0		Chip Revision	An 8-bit register which represents the silicon revision level. Revision 0 = 0000 0000.
01H	R/$\overline{W}$	7:0	01101001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. (This will give the PLL more time to lock.) See Note 1.
02H	R/$\overline{W}$	7:4	1101****	PLL Div LSB	Bits [7:4] LSBs of the PLL divider word. See Note 1.
03H	R/$\overline{W}$	7:2	01******	VCO/CPMP	Bits [7:6] VCO Range. Selects VCO frequency range. (See PLL description.)
			001*		Bits [5:3] Charge Pump Current. Varies the current that drives the low-pass filter. (See PLL description.)
04H	R/$\overline{W}$	7:3	10000***	Phase Adjust	ADC Clock phase adjustment. Larger values mean more delay. (1 LSB = T/32)
05H	R/$\overline{W}$	7:0	00001000	Clamp Placement	Places the Clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
06H	R/$\overline{W}$	7:0	00010100	Clamp Duration	Number of clock periods that the Clamp signal is actively clamping.
07H	R/$\overline{W}$	7:0	00100000	Hsync Output Pulsewidth	Sets the number of pixel clocks that HSOUT will remain active.
08H	R/$\overline{W}$	7:0	10000000	Red Gain	Controls ADC input range (Contrast) of each respective channel. Bigger values give less contrast.
09H	R/$\overline{W}$	7:0	10000000	Green Gain	
0AH	R/$\overline{W}$	7:0	10000000	Blue Gain	
0BH	R/$\overline{W}$	7:1	1000000*	Red Offset	Controls dc offset (Brightness) of each respective channel. Bigger values decrease brightness.
0CH	R/$\overline{W}$	7:1	1000000*	Green Offset	
0DH	R/$\overline{W}$	7:1	1000000*	Blue Offset	

Table V. Control Register Map (continued)

Hex Address	Read and Write or Read Only	Bits	Default Value	Register Name	Function
0EH	R/$\overline{W}$	7:0	0*******	Sync Control	Bit 7—Hsync Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 6 in Register 0Eh.)
			*1******		Bit 6—Hsync Input Polarity. Indicates to the PLL the polarity of the incoming Hsync signal. (Logic 0 = active low, Logic 1 = active high.)
			0***		Bit 5—Hsync Output Polarity. (Logic 0 = Logic High Sync, Logic 1 = Logic Low Sync).
			0*		Bit 4—Active Hsync Override. If set to Logic 1, the user can select the Hsync to be used via Bit 3. If set to Logic 0, the active interface is selected via Bit 6 in Register 14H.
			****0***		Bit 3—Active Hsync select. Logic 0 selects Hsync as the active sync. Logic 1 selects Sync-on-Green as the active sync. Note: the indicated Hsync will be used only if Bit 4 is set to Logic 1 or if both syncs are active (Bits 1, 7 = Logic 1 in Register 14H).
			*****0**		Bit 2—Vsync Output Invert. (Logic 0 = No Invert, Logic 1 = Invert.)
			******0*		Bit 1—Active Vsync override. If set to Logic 1, the user can select the Vsync to be used via Bit 0. If set to Logic 0, the active interface is selected via Bit 3 in Register 14H.
			*******0		Bit 0—Active Vsync select. Logic 0 selects Raw Vsync as the output Vsync. Logic 1 selects Sync Separated Vsync as the output Vsync. Note: the indicated Vsync will be used only if Bit 1 is set to Logic 1.
0FH	R/$\overline{W}$	7:1	0*******		Bit 7—Clamp Function. Chooses between Hsync for Clamp signal or another external signal to be used for clamping. (Logic 0 = Hsync, Logic 1 = Clamp.)
			*1******		Bit 6—Clamp Polarity. Valid only with external Clamp signal. (Logic 0 = active high, Logic 1 selects active low.)
			0***		Bit 5—COAST select. Logic 0 selects the coast input pin to be used for the PLL coast. Logic 1 selects Vsync to be used for the PLL coast.
			0*		Bit 4—COAST Polarity Override. (Logic 0 = Polarity determined by chip, Logic 1 = Polarity set by Bit 3 in register 0Fh.)
			****1***		Bit 3—COAST Polarity. Changes polarity of external COAST signal. (Logic = 0 = active low, Logic 1 = active high.)
			*****1**		Bit 2—Seek Mode Override. (Logic 1 = allow low-power mode, Logic 0 = disallow low-power mode.)
			******1*		Bit 1—$\overline{PWRDN}$. Full Chip Power Down, active low. (Logic 0 = Full Chip Power Down, Logic 1 = normal.)
10H	R/$\overline{W}$	7:3	01111***	Sync-on-Green Threshold	Sync-on-Green Threshold – Sets the voltage level of the Sync-on-Green slicer's comparator.
			*****0**		Bit 2—Red Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 9).
			******0*		Bit 1—Blue Clamp Select – Logic 0 selects clamp to ground. Logic 1 selects clamp to midscale (voltage at Pin 24).
			*******0		Bit 0—Must be set to 1 for proper operation.
11H	R/$\overline{W}$	7:0	00100000	Sync Separator Threshold	Sync Separator Threshold – Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
12H	R/$\overline{W}$	7:0	00000000	Pre-COAST	Pre-COAST – Sets the number of Hsync periods that coast becomes active prior to Vsync.
13H	R/$\overline{W}$	7:0	00000000	Post-COAST	Post-COAST – Sets the number of Hsync periods that coast stays active following Vsync.

Table V. Control Register Map (continued)

Hex Address	Read and Write or Read Only	Bits	Default Value	Register Name	Function
14H	RO	7:0		Sync Detect	Bit 7—Hsync Detect. It is set to Logic 1 if Hsync is present on the analog interface, else it is set to Logic 0.
					Bit 6—AHS: Active Hsync. This bit indicates which analog Hsync is being used. (Logic 0 = Hsync input pin, Logic 1 = Hsync from sync-on-green.)
					Bit 5—Input Hsync Polarity Detect. (Logic 0 = active low, Logic 1 = active high.)
					Bit 4—Vsync detect. It is set to Logic 1 if Vsync is present on the analog interface, else it is set to Logic 0.
					Bit 3—AVS: Active Vsync. This bit indicates which analog Vsync is being used. (Logic 0 = Vsync input pin, Logic 1 = Vsync from sync separator.)
					Bit 2—Output Vsync Polarity Detect. (Logic 0 = active low, Logic 1 = active high.)
					Bit 1—Sync-on-Green Detect. It is set to Logic 1 if sync is present on the green video input, else it is set to 0.
					Bit 0—Input COAST Polarity Detect. (Logic 0 = active low, Logic 1 = active high.)
15H	R/$\overline{W}$	7:0	1*******		Bit 7—Channel Mode. Determines single-channel or dual-channel output mode. (Logic 0 = single-channel mode, Logic 1 = dual-channel mode.)
			*1******		Bit 6—Output Mode. Determine interleaved or parallel output mode. (Logic 0 = interleaved mode, Logic 1 = parallel mode.)
			0***		Bit 5—A/B Invert. Determines which port outputs the first data byte after Hsync. (Logic 0 = A port, Logic 1 = B port.)
			0*		Bit 4—4:2:2 Output Formatting Mode.
			****0***		Bit 3—Input Mux Control.
			*****11*		Bits [2:1]—Input Bandwidth.
			*******0		Bit 0—External Clock. Shuts down PLL and allows external clock to drive the part. (Logic 0 = use internal PLL, Logic 1 = bypassing of the internal PLL.)
16H	R/$\overline{W}$	7:0	11111111	Test Register	Must be set to 11111110 for proper operation.
17H	R/$\overline{W}$	7:3	00000000	Test Register	Must be set to default for proper operation.
18H	RO	7:0		Test Register	
19H	RO	7:0		Test Register	

NOTE
1. The AD9888 only updates the PLL divide ratio when the LSBs are written to (Register 02h).

2-WIRE SERIAL CONTROL REGISTER DETAIL CHIP IDENTIFICATION

00 7-0 Chip Revision

An 8-bit register that represents the silicon revision. Revision 0 = 0000 0000, Revision 1 = 0000 0001.

PLL DIVIDER CONTROL

01 7-0 PLL Divide Ratio MSBs

The eight most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a master clock from an incoming Hsync signal. The master clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established standard timing specifications, which will assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (Table IV).

However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV will usually produce one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9888 updates the full divide ratio only when the LSBs are changed. Writing to this register by itself will not trigger an update.

02 7-4 PLL Divide Ratio LSBs

The four least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 69h, PLLDIVL = Dxh).

The AD9888 updates the full divide ratio only when this register is written to.

CLOCK GENERATOR CONTROL

03 7-6 VCO Range Select

Two bits that establish the operating range of the clock generator.

VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL gives the best jitter performance at high frequencies. For this reason, in order to output low pixel rates and still get good jitter performance, the PLL actually operates at a higher frequency but then divides down the clock rate afterwards. Table VI shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table VI. VCO Ranges

VCORNGE	Pixel Rate Range
00	10–45
01	45–90
10	90–150
11	150+

The power-up default value is 01.

03 5-3 Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table VII. Charge Pump Currents

CURRENT	Current (μA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

CURRENT must be set to correspond with the desired operating frequency (incoming pixel rate).

The power-up default value is CURRENT = 001.

04 7-3 Clock Phase Adjust

A five-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default value is 16.

CLAMP TIMING

05 7-0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When the external clamp control bit is set to 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) pixel periods after the trailing edge of Hsync. The clamp placement may be programmed to any value up to 255, except 0.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When the external clamp control bit is set to 1, this register is ignored.

06 7-0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

When the external clamp control bit is set to 0, a clamp signal is generated internally, at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (Clamp Placement) pixel periods after the trailing edge of Hsync, and continues for (Clamp Duration) pixel periods. The clamp duration may

be programmed to any value between 1 and 255. A value of 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the Average Picture Level (APL), or brightness.

When the external clamp control bit is set to 1, this register is ignored.

Hsync PULSEWIDTH

07 7-0 Hsync Output Pulsewidth
An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9888 then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of the Hsync output, which is also phase-adjusted.

INPUT GAIN

08 7-0 Red Channel Gain Adjust
An 8-bit word that sets the gain of the RED channel. The AD9888 can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Set ting REDGAIN to 255 corresponds to an input range of 1.0 V. A REDGAIN of 0 establishes an input range of 0.5 V. Note that INCREASING REDGAIN results in the picture having LESS CONTRAST (the input signal uses fewer of the available converter codes). See Figure 2.

09 7-0 Green Channel Gain Adjust
An 8-bit word that sets the gain of the GREEN channel. See REDGAIN (08).

0A 7-0 Blue Channel Gain Adjust
An 8-bit word that sets the gain of the BLUE channel. See REDGAIN (08).

INPUT OFFSET

0B 7-1 Red Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the RED channel. One LSB of offset adjustment equals ap proximately one LSB change in the ADC offset. There fore, the absolute magnitude of the offset adjustment scales as the gain of the channel is changed. A nominal setting of 63 results in the channel nominally clamping the back porch (during the clamping interval) to code 00. An offset setting of 127 results in the channel clamping to code 64 of the ADC. An offset setting of 0 clamps to code –63 (off the bottom of the range). Increasing the value of Red Offset decreases the brightness of the channel.

0C 7-1 Green Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the GREEN channel. See REDOFST (0B).

0D 7-1 Blue Channel Offset Adjust
A 7-bit offset binary word that sets the dc offset of the BLUE channel. See REDOFST (0B).

0E 7 Hsync Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table VIII. Hsync Input Polarity Override Settings

Override Bit	Result
0	Hsync Polarity Determined by Chip
1	Hsync Polarity Determined by User

The default for Hsync polarity override is 0 (polarity determined by chip).

0E 6 HSPOL Hsync Input Polarity
A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table IX. Hsync Input Polarity Settings

HSPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means the leading edge of the Hsync pulse is negative-going. All timing is based on the leading edge of Hsync, which is the *falling* edge. The rising edge has no effect.

Active HIGH means the leading edge of the Hsync pulse is positive-going. This means that timing will be based on the leading edge of Hsync, which is now the *rising* edge.

The device will operate if this bit is set incorrectly, but the internally generated clamp position, as established by Clamp Placement (Register 05h), will not be placed as expected, which may generate clamping errors.

The power-up default value is HSPOL = 1.

0E 5 Hsync Output Polarity
One bit that determines the polarity of the Hsync output and the SOG output. Table X shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table X. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (Positive Polarity)
1	Logic 0 (Negative Polarity)

The default setting for this register is 0.

0E 4 Active Hsync Override
This bit is used to override the automatic Hsync selection. To override, set this bit to Logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

Table XI. Active Hsync Override Settings

Override	Result
0	Auto determines the active interface.
1	Override, Bit 3 determines the active interface.

The default for this register is 0.

0E 3 Active Hsync Select
This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternately, it is used to determine the active Hsync when not overriding but both Hsyncs are detected.

Table XII. Active Hsync Select Settings

Select	Result
0	Hsync Input
1	Sync-on-Green Input

The default for this register is 0.

0E 2 Vsync Output Invert
A bit that inverts the polarity of the Vsync output. Table XIII shows the effect of this option.

Table XIII. Vsync Output Polarity Settings

Setting	SYNC
1	Invert
0	Don't Invert

The default setting for this register is 0.

0E 1 Active Vsync Override
This bit is used to override the automatic Vsync selection. To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 0 in this register.

Table XIV. Active Vsync Override Settings

Override	Result
0	Auto determines the active Vsync.
1	Override, Bit 0 determines the active Vsync.

The default for this register is 0.

0E 0 Active Vsync Select
This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table XV. Active Vsync Select Settings

Select	Result
0	Vsync Input
1	Sync Separator Output

The default for this register is 0.

0F 7 Clamp Input Signal Source
A bit that determines the source of clamp timing.

Table XVI. Clamp Input Signal Source Settings

External Clamp	Function
0	Internally Generated Clamp
1	Externally Provided Clamp Signal

A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync.

A 1 enables the external CLAMP input pin. The three channels are clamped when the CLAMP signal is active. The polarity of CLAMP is determined by the Clamp Polarity bit (Register 0Fh, Bit 6).

The power-up default value is External Clamp = 0.

0F 6 Clamp Input Signal Polarity
A bit that determines the polarity of the externally provided CLAMP signal.

Table XVII. Clamp Input Signal Polarity Settings

Clamp Polarity	Function
1	Active LOW
0	Active HIGH

A Logic 1 means that the circuit will clamp when CLAMP is LOW, and it will pass the signal to the ADC when CLAMP is HIGH.

A Logic 0 means that the circuit will clamp when CLAMP is HIGH, and it will pass the signal to the ADC when CLAMP is LOW.

The power-up default value is Clamp Polarity = 1.

0F 5 COAST Select
This bit is used to select the active coast source. The choices are the coast input pin or Vsync. If Vsync is selected, the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 0E, Bits 1, 0).

Table XVIII. COAST Source Selection Settings

Select	Result
0	COAST Input Pin
1	Vsync (See above text.)

The default for this register is 0.

0F 4 COAST Input Polarity Override
This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL.

Table XIX. COAST Input Polarity Override Settings

Override Bit	Result
0	COAST Polarity Determined by Chip
1	COAST Polarity Determined by User

The default for coast polarity override is 0.

0F 3 COAST Input Polarity
A bit to indicate the polarity of the COAST signal that is applied to the PLL COAST input.

Table XX. COAST Input Polarity Settings

CSTPOL	Function
0	Active LOW
1	Active HIGH

Active LOW means that the clock generator will ignore Hsync inputs when COAST is LOW, and continue operating at the same nominal frequency until COAST goes HIGH.

Active HIGH means that the clock generator will ignore Hsync inputs when COAST is HIGH, and continue operating at the same nominal frequency until COAST goes LOW.

This function needs to be used along with the COAST polarity override bit (Bit 4).

The power-up default value is CSTPOL = 1.

0F 2 Seek Mode Override
This bit is used to either allow or disallow the low-power mode. The low-power mode (seek mode) occurs when there are no signals on any of the Sync inputs.

Table XXI. Seek Mode Override Settings

Select	Result
1	Allow Seek Mode
0	Disallow Seek Mode

The default for this register is 1.

0F 1 $\overline{\text{PWRDN}}$
This bit is used to put the chip in power-down mode. In this mode the chip's power dissipation is reduced to a fraction of the typical power (see the Electrical Characteristics table for exact power dissipation). When in power-down, the HSOUT, VSOUT, DATACK, $\overline{\text{DATACK}}$, and all 48 of the data outputs are put into a high impedance state. (Note: the SOGOUT output is not put into high impedance.) Circuit blocks that continue to be active during power-down include the voltage references, sync processing, sync detection, and the serial register. These blocks facilitate a fast start-up from power-down.

Table XXII. Power-Down Settings

Select	Result
0	Power-Down
1	Normal Operation

The default for this register is 1.

10 7-3 Sync-on-Green Slicer Threshold
This register allows the comparator threshold of the Sync-on-Green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV and the maximum setting equaling 330 mV.

The default setting is 15 and corresponds to a threshold value of 0.16 V.

10 2 Red Clamp Select
A bit that determines whether the red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YcbCr (or YUV), the Y channel is referenced to ground, but the CbCr channels are referenced to midscale. Clamping to midscale actually clamps to Pin 9.

Table XXIII. Red Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 9)

The default setting for this register is 0.

10 1 Blue Clamp Select
A bit that determines whether the blue channel is clamped to ground or to midscale. Clamping to midscale actually clamps to Pin 24.

Table XXIV. Blue Clamp Select Settings

Clamp	Function
0	Clamp to Ground
1	Clamp to Midscale (Pin 24)

The default setting for this register is 0.

11 7:0 Sync Separator Threshold
This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulsewidth. Note: the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 32.

12 7-0 Pre-COAST
This register allows the COAST signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

13 7-0 Post-COAST
This register allows the COAST signal to be applied following to the Vsync signal. This is necessary in cases where post-equalization pulses are present. The step size for this control is one Hsync period.

The default is 0.

14 7 Hsync Detect

This bit is used to indicate when activity is detected on the selected Hsync input pin. If HSYNC is held high or low, activity will not be detected.

Table XXV. Hsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram shows where this function is implemented.

14 6 AHS – Active Hsync

This bit indicates which Hsync input source is being used by the PLL (Hsync input or Sync-on-Green). Bits 7 and 1 in this register are what determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in Register 0EH. The user can override this function via Bit 4 in Register 0EH. If the override bit is set to Logic 1, then this bit will be forced to whatever the state of Bit 3 in register 0EH is set to.

Table XXVI. Active Hsync Results

Bit 7 (Hsync Detect)	Bit 1 (SOG Detect)	Bit 4, Reg OEH (Override)	AHS
0	0	0	Bit 3 in 0EH
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0EH
X	X	1	Bit 3 in 0EH

AHS = 0 means use the HSYNC pin input for HSYNC.

AHS = 1 means use the SOG pin input for HSYNC.

The override bit is in Register 0EH, Bit 4.

14 5 Detected Hsync Input Polarity Status

This bit reports the status of the HSYNC input polarity detection circuit. It can be used to determine the polarity of the HSYNC input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 25).

Table XXVII. Detected Hsync Input Polarity Status

HSYNC Polarity Status	Result
0	Hsync Polarity is Negative.
1	Hsync Polarity is Positive.

14 4 Vsync Detect

This bit is used to indicate when activity is detected on the selected Vsync input pin. If Vsync is held high or low, activity will not be detected.

Table XXVIII. Vsync Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The sync processing block diagram (Figure 25) shows where this function is implemented.

14 3 AVS – Active Vsync

This bit indicates which Vsync source is being used; the Vsync input or the output from the sync separator. Bit 4 in this register is what determines which is active. If both Vsync and SOG are detected, the user can determine which has priority via Bit 0 in Register 0EH. The user can override this function via Bit 1 in Register 0EH. If the override bit is set to Logic 1, this bit will be forced to whatever the state of Bit 0 in Register 0EH is set to.

Table XXIX. Active Vsync Results

Bit 5 (Vsync Detect)	Override	AVS
0	0	1
1	0	0
X	1	Bit 0 in 0EH

AVS = 1 means Sync separator.

AVS = 0 means Vsync input.

The override bit is in Register 0EH, Bit 1.

14 2 Detected Vsync Output Polarity Status

This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync input. The detection circuit's location is shown in the Sync Processing Block Diagram (Figure 25).

Table XXX. Detected Vsync Input Polarity Status

Vsync Polarity Status	Result
0	Vsync Polarity is Active Low
1	Vsync Polarity is Active High

14 1 Sync-on-Green Detect

This bit is used to indicate when Sync activity is detected on the selected Sync-on-Green input pin.

Table XXXI. Sync-on-Green Detection Results

Detect	Function
0	No Activity Detected
1	Activity Detected

The Sync Processing Block Diagram (Figure 25) shows where this function is implemented.

14 0 Detected COAST Polarity Status

This bit reports the status of the coast input polarity detection circuit. It can be used to determine the polarity of the COAST input. The detection circuit's location is shown in Figure 25.

Table XXXII. Detected COAST Input Polarity Status

HSYNC Polarity Status	Result
0	COAST Polarity is Negative.
1	COAST Polarity is Positive.

MODE CONTROL 1

15 7 Channel Mode

A bit that determines whether all pixels are presented to a single port (A), or alternating pixels are demultiplexed to Ports A and B.

Table XXXIII. Channel Mode Settings

DEMUX	Function
0	All data goes to Port A.
1	Alternate pixels go to Port A and Port B.

When DEMUX = 0, Port B outputs are in a high-impedance state. The maximum data rate for single-port mode is 110 MHz. The timing diagrams starting with Figure 13 show the effects of this option.

The power-up default value is 1.

15 6 Output Mode

A bit that determines whether all pixels are presented to Port A and Port B simultaneously on every second DATACK rising edge, or alternately on Port A and Port B on successive DATACK rising edges.

Table XXXIV. Output Mode Settings

PARALLEL	Function
0	Data is interleaved.
1	Data is simultaneous on every other data clock.

When in single port mode (DEMUX = 0), this bit is ignored. The timing diagrams (Figure 17) show the effects of this option.

The power-up default value is PARALLEL = 1.

15 5 Output Port Phase

One bit that determines whether even pixels or odd pixels go to Port A.

Table XXXV. Output Port Phase Settings

OUTPHASE	First Pixel after Hsync
0	Port A
1	Port B

In normal operation (OUTPHASE = 0), when operating in dual-port output mode (DEMUX = 1), the first sample after the Hsync leading edge is presented at Port A. Every subsequent ODD sample appears at Port A. All EVEN samples go to Port B.

When OUTPHASE = 1, these ports are reversed and the first sample goes to Port B.

When DEMUX = 0, this bit is ignored as data always comes out of only Port A.

15 4 4:2:2 Output Mode Select

A bit that configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 down to 16 for applications using YUV, YCbCr, or YPbPr graphics signals. A timing diagram for this mode is shown in Figure 12. Recommended input and output configurations are shown in Table XXXVII. In 4:2:2 mode, the red and blue channels can be interchanged to help satisfy board layout or timing requirements, but the green channel must be configured for Y.

Table XXXVI. 4:2:2 Output Mode Select

Select	Output Mode
0	4:4:4
1	4:2:2

Table XXXVII. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	V	U/V
Green	Y	Y
Blue	U	High Impedance

15 3 Input Mux Control

A bit that selects either analog inputs from Channel 0 or the analog inputs from Channel 1.

Table XXXVIII. Input Mux Control

Control	Channel Selected
0	Channel 0
1	Channel 1

15 2-1 Analog Bandwidth Control

Two bits that select the analog bandwidth.

Table XXXIX. Analog Bandwidth Control

Bit 2	Bit 1	Analog Bandwidth
1	1	500 MHz
1	0	300 MHz
0	1	150 MHz
0	0	75 MHz

15 0 External Clock Select

A bit that determines the source of the pixel clock.

Table XL. External Clock Select Settings

EXTCLK	Function
0	Internally Generated Clock
1	Externally Provided Clock Signal

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided HSYNC.

A Logic 1 enables the external CKEXT input pin. In this mode, the PLL Divide Ratio (PLLDIV) is ignored. The clock phase adjust (PHASE) is still functional.

The power-up default value is EXTCLK = 0.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial interface control interface is provided. Up to two AD9888 devices may be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The AD9888 acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled HIGH by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is LOW. If SDA changes state while SCL is HIGH, the serial interface interprets that action as a start or stop sequence.

There are six components to serial bus operation:

Start signal
Slave address byte
Base register address byte
Data byte to read or write
Stop signal

When the serial interface is inactive (SCL and SDA are HIGH), communications are initiated by sending a start signal. The start signal is a HIGH-to-LOW transition on SDA while SCL is HIGH. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer, read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the A_0 input pin in Table XLI), the AD9888 acknowledges by bringing SDA LOW on the ninth SCL pulse. If the addresses do not match, the AD9888 does not acknowledge

Table XLI. Serial Port Addresses

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A_6	A_5	A_4	A_3	A_2	A_1	A_0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence.

If the AD9888 does not acknowledge the master device during a write sequence, the SDA remains HIGH so the master can generate a stop signal. If the master device does not acknowledge the AD9888 during a read sequence, the AD9888 interprets this as "end of data." The SDA remains HIGH so the master can generate a stop signal.

Writing data to specific control registers of the AD9888 requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If more bytes are transferred than there are available addresses, the address will not increment and remain at its maximum value of 19h. Any base address higher than 19h will not produce an ACKnowledge signal.

Data are read from the control registers of the AD9888 in a similar manner. Reading requires two data transfer operations.

The base address must be written with the R/$\overline{W}$ bit of the slave address byte LOW to set up a sequential read operation.

Reading (the R/$\overline{W}$ bit of the slave address byte HIGH) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9888, a stop signal must be sent. A stop signal comprises a LOW-to-HIGH transition of SDA while SCL is HIGH.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

Serial Interface Read/Write Examples

Write to One Control Register

Start Signal
Slave Address Byte (R/$\overline{W}$ Bit = LOW)
Base Address Byte
Data Byte to Base Address
Stop Signal

Write to Four Consecutive Control Registers

Start Signal
Slave Address Byte (R/$\overline{W}$ Bit = LOW)
Base Address Byte
Data Byte to Base Address
Data Byte to (Base Address + 1)
Data Byte to (Base Address + 2)
Data Byte to (Base Address + 3)
Stop Signal

Read from One Control Register

Start Signal
Slave Address Byte (R/$\overline{W}$ Bit = LOW)
Base Address Byte
Start Signal
Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
Data Byte from Base Address
Stop Signal

Read from Four Consecutive Control Registers

Start Signal
Slave Address Byte (R/$\overline{W}$ bit = LOW)
Base Address Byte
Start Signal
Slave Address Byte (R/$\overline{W}$ Bit = HIGH)
Data Byte from Base Address
Data Byte from (Base Address + 1)
Data Byte from (Base Address + 2)
Data Byte from (Base Address + 3)
Stop Signal

Sync Processing

Table XLII. Control of the Sync Block Muxes via the Serial Register

Mux Number(s)	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0EH: Bit 3	0 1	Pass HSYNC Pass Sync-on-Green
3	0FH: Bit 5	0 1	Pass COAST Pass Vsync
4	0EH: Bit 0	0 1	Pass Vsync Pass Sync Separator Signal
5	15H: Bit 3	0 1	Pass Channel 0 Inputs Pass Channel 1 Inputs

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics systems, only those with Sync-on-Green. The sync signal is extracted from the green channel in a two-step process. First, the SOG input is clamped to its negative peak (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The "sliced" sync is typically a composite sync signal containing both Hsync and Vsync.

Sync Separator

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. So, it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulsewidth and a Vsync pulsewidth.

The sync separator on the AD9888 is an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. (Polarities are determined elsewhere on the chip.) The basic idea is that the counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter only reaches a value of N before the pulse ends. It then starts counting down eventually reaching 0 before the next Hsync pulse arrives. The specific value of N will vary for different video modes, but will always be less than 255. For example, with a 1 µs width Hsync, the counter will only reach 5 (1 µs/200 ns = 5). Now, when Vsync is present on the composite sync, the counter will also count up. However, since the Vsync signal is much longer, it will count to a higher number M. For most video modes, M will be at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (T) can be programmed through the serial register (0fh).

Once Vsync has been detected, there is a similar process to detect when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. Similar to the previous case, it will detect the absence of Vsync when the counter reaches the threshold count (T). In this way, it will reject noise and/or serration pulses. Once Vsync is detected to be absent, the counter resets to 0 and begins the cycle again.

PCB LAYOUT RECOMMENDATIONS

The AD9888 is a high-precision, high-speed analog device. To get the maximum performance out of the part, it is important to have a well laid-out board. The following is a guide for designing a board using the AD9888.

Analog Interface Inputs

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9888 as close as possible to the graphics (VGA) connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 1) as close to the AD9888 chip as possible. Any additional trace length between the termination resistors and the input of the AD9888 increases the magnitude of reflections, which will corrupt the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω will also increase the chance of reflections.

The AD9888 has very high input bandwidth (500 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it will also capture any high-frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

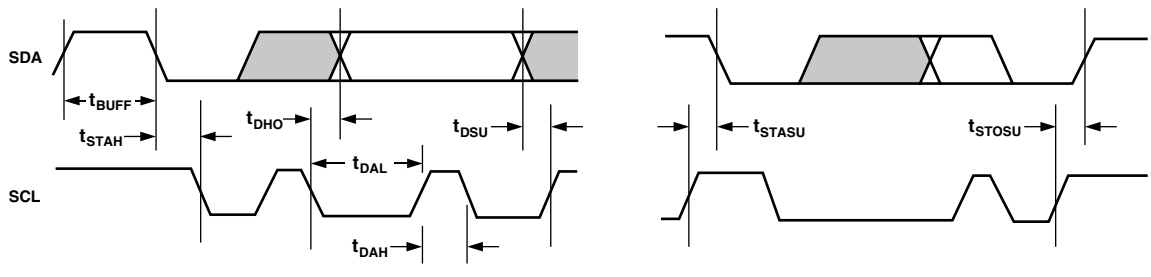


Figure 23. Serial Port Read/Write Timing

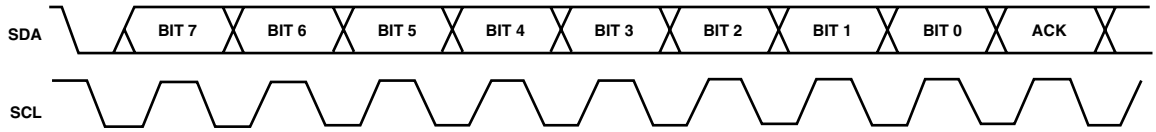


Figure 24. Serial Interface—Typical Byte Transfer

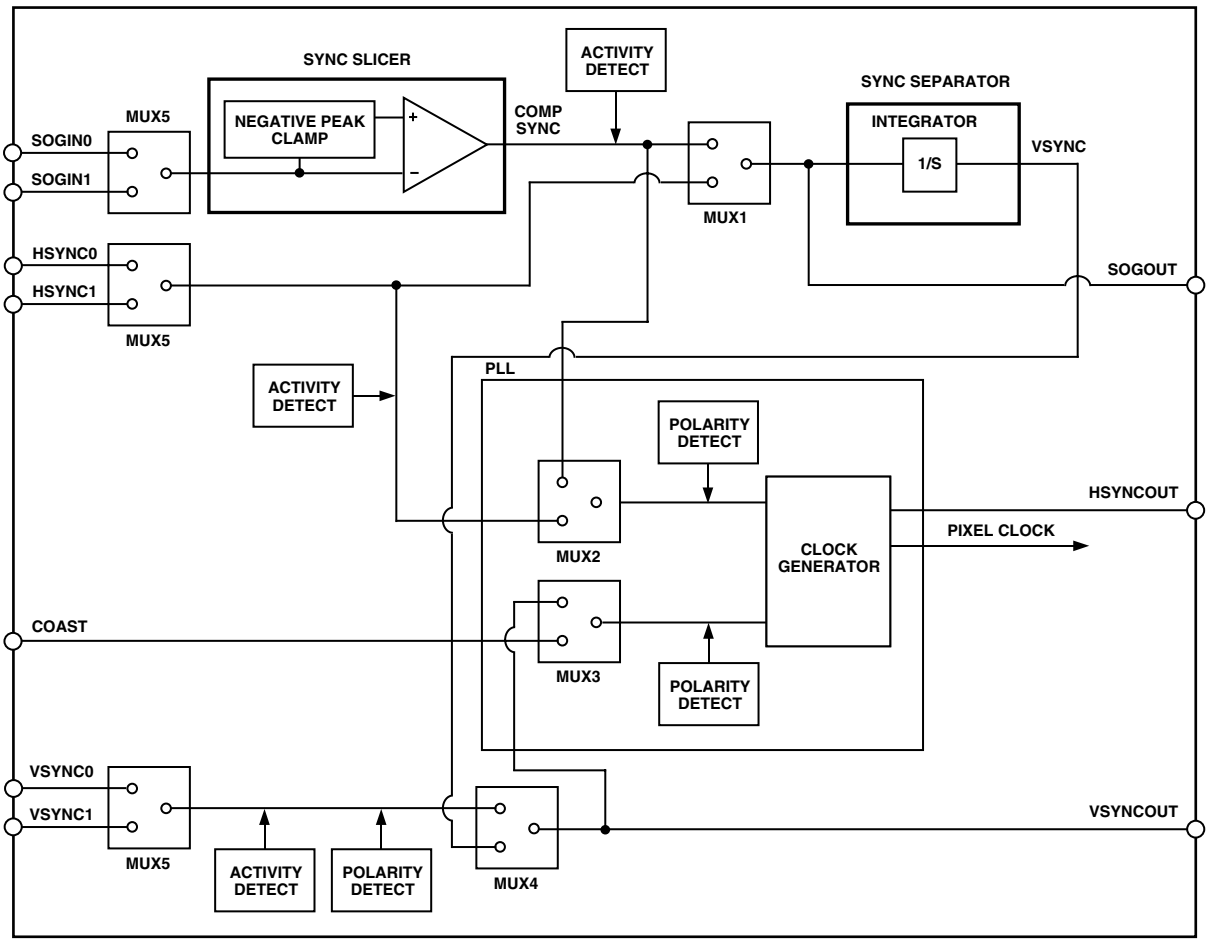


Figure 25. Sync Processing Block Diagram

The AD9888 can digitize graphics signals over a very wide range of frequencies (10 MHz to 205 MHz). Often characteristics that are beneficial at one frequency can be detrimental at another. Analog bandwidth is one such characteristic. For UXGA resolutions (up to 205 MHz), a very high analog bandwidth is desirable because of the fast input signal slew rates. For VGA and lower resolutions (down to 12.5 MHz), a very high bandwidth is not desirable, because it allows excess noise to pass through. To accommodate these varying needs, the AD9888 includes variable analog bandwidth control. Four settings are available (75 MHz, 150 MHz, 300 MHz, and 500 MHz), allowing the analog bandwidth to be matched with the resolution of the incoming graphics signal.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 µF capacitor. The exception is in the case where two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9888, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane => capacitor => power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PVd (the clock generator supply). Abrupt changes in PVd can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (Vd and PVd).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated

analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVd, from a different, cleaner, power source (for example, from a 12 V supply).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to at least place a single ground plane under the AD9888. The location of the split should be at the receiver of the digital outputs. For this case it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop: power plane => AD9888 => digital output trace => digital data receiver => digital ground plane => analog ground plane.

PLL

Place the PLL loop filter components as close to the FILT pin as possible.

Do not place any digital or other high-frequency traces near these components.

Use the values suggested in the data sheet with 10% tolerances or less.

Outputs (Both Data and Clocks)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, requiring more current and causing more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor of value 50 Ω–200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the AD9888. If series resistors are used, place them as close to the AD9888 pins as possible (although try not to add vias or extra length to the output trace in order to get the resistors closer).

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance will increase the current transients inside of the AD9888 creating more digital noise on its power supplies.

Digital Inputs

The digital inputs on the AD9888 were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. So, no extra components need to be added if using 5.0 V logic.

Any noise that gets onto the Hsync input trace will add jitter to the system. Therefore, minimize the trace length and do not run any digital or other high-frequency traces near it.

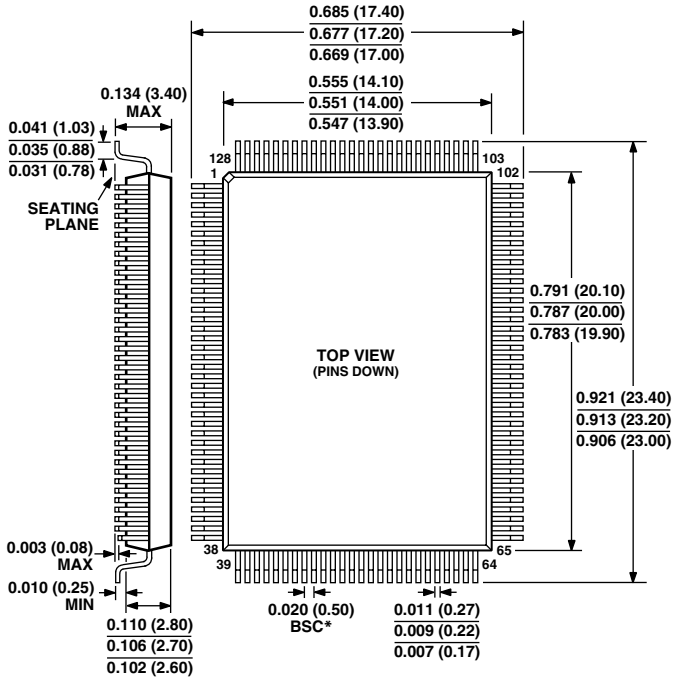
Voltage Reference

Bypass with a 0.1 µF capacitor. Place as close to the AD9888 pin as possible. Make the ground connection as short as possible.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

128-Lead Plastic Quad Flatpack (MQFP)
(S-128A)



* THE ACTUAL POSITION OF EACH LEAD IS WITHIN 0.00315 (0.08) FROM ITS IDEAL POSITION WHEN MEASURED IN THE LATERAL DIRECTION. CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED.

THE CONTROLLING DIMENSIONS ARE IN MM.

Revision History

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