NID9N05CL

Power MOSFET

9.0 A, 52 V, N−Channel, Logic Level, Clamped MOSFET w/ ESD Protection in a DPAK Package

Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

Features

- Diode Clamp Between Gate and Source
- ESD Protection − HBM 5000 V
- Active Over−Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance

Applications

- Automotive and Industrial Markets: Solenoid Drivers, Lamp Drivers, Small Motor Drivers

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	52−59	V
Gate−to−Source Voltage − Continuous	V_{GS}	±15	V
Drain Current − Continuous @ T_A = 25°C − Single Pulse (t_p = 10 μs)	I_D I_{DM}	9.0 35	A
Total Power Dissipation @ T_A = 25°C	P_D	28.8	W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 125°C (V_{DD} = 50 V, $I_{D(pk)}$ = 1.5 A, V_{GS} = 10 V, R_G = 25 Ω)	E_{AS}	160	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1) − Junction−to−Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	5.2 72 100	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 s	T_L	260	°C

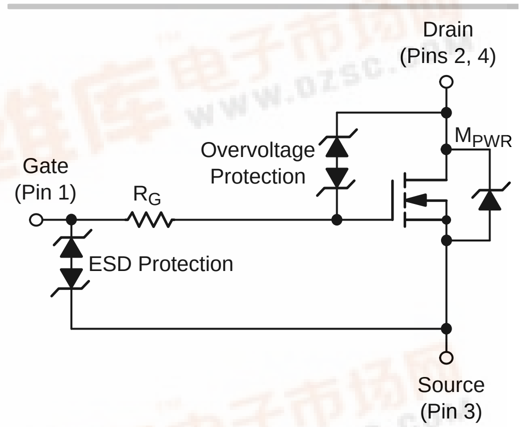
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using 1″ pad size, (Cu area 1.127 in^2)
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu area 0.412 in^2)

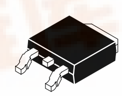
ON Semiconductor®

http://onsemi.com

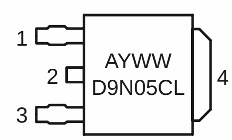
V_{DSS} (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX (Limited)
52 V	90 mΩ	9.0 A



MARKING DIAGRAM



DPAK
CASE 369C
STYLE 2



D9N05CL	= Device Code	1	= Gate
A	= Assembly Location	2	= Drain
Y	= Year	3	= Source
WW	= Work Week	4	= Drain

ORDERING INFORMATION

Device	Package	Shipping†
NID9N05CLT4	DPAK	2500/Tape & Reel
NID9N05CL	DPAK	75 Units/Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 V, I_D = 1.0 mA, T_J = 25°C) (V_{GS} = 0 V, I_D = 1.0 mA, T_J = −40°C to 125°C) Temperature Coefficient (Negative)	$V_{(BR)DSS}$	 52 50.8 −	 55 54 −10	 59 59.5 −	 V V mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 40 V, V_{GS} = 0 V) (V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125°C)	I_{DSS}	 − −	 − −	 10 25	μA
Gate−Body Leakage Current (V_{GS} = ±8 V, V_{DS} = 0 V) (V_{GS} = ±14 V, V_{DS} = 0 V)	I_{GSS}	 − −	 − ±22	 ±10 −	μA
ON CHARACTERISTICS (Note 3)					
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 100 μA) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 1.3 −	 1.75 −4.5	 2.5 −	 V mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 4.0 V, I_D = 1.5 A) (V_{GS} = 3.5 V, I_D = 0.6 A) (V_{GS} = 3.0 V, I_D = 0.2 A) (V_{GS} = 12 V, I_D = 9.0 A) (V_{GS} = 12 V, I_D = 12 A)	$R_{DS(on)}$	 − − − 70 67	 153 175 − 90 95	 181 364 1210 − −	mΩ
Forward Transconductance (Note 3) (V_{DS} = 15 V, I_D = 9.0 A)	g_{FS}	−	24	−	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 40 V, V_{GS} = 0 V, f = 10 kHz)	C_{iss}	−	155	250	pF
Output Capacitance (V_{DS} = 40 V, V_{GS} = 0 V, f = 10 kHz)	C_{oss}	−	60	100	
Transfer Capacitance (V_{DS} = 40 V, V_{GS} = 0 V, f = 10 kHz)	C_{rss}	−	25	40	
Input Capacitance (V_{DS} = 25 V, V_{GS} = 0 V, f = 10 kHz)	C_{iss}	−	175	−	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0 V, f = 10 kHz)	C_{oss}	−	70	−	
Transfer Capacitance (V_{DS} = 25 V, V_{GS} = 0 V, f = 10 kHz)	C_{rss}	−	30	−	

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{GS} = 10 V, V_{DD} = 40 V, I_D = 9.0 A, R_G = 9.0 Ω)	$t_{d(on)}$	−	130	200	ns
Rise Time		t_r	−	500	750	
Turn−Off Delay Time		$t_{d(off)}$	−	1300	2000	
Fall Time		t_f	−	1150	1850	
Turn−On Delay Time	(V_{GS} = 10 V, V_{DD} = 15 V, I_D = 1.5 A, R_G = 2 kΩ)	$t_{d(on)}$	−	200	−	ns
Rise Time		t_r	−	500	−	
Turn−Off Delay Time		$t_{d(off)}$	−	2500	−	
Fall Time		t_f	−	1800	−	
Turn−On Delay Time	(V_{GS} = 10 V, V_{DD} = 15 V, I_D = 1.5 A, R_G = 50 Ω)	$t_{d(on)}$	−	120	−	ns
Rise Time		t_r	−	275	−	
Turn−Off Delay Time		$t_{d(off)}$	−	1600	−	
Fall Time		t_f	−	1100	−	
Gate Charge	(V_{GS} = 4.5 V, V_{DS} = 40 V, I_D = 9.0 A) (Note 3)	Q_T	−	4.5	7.0	nC
		Q_1	−	1.2	−	
		Q_2	−	2.7	−	
Gate Charge	(V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 1.5 A) (Note 3)	Q_T	−	3.6	−	nC
		Q_1	−	1.0	−	
		Q_2	−	2.0	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 4.5 A, V_{GS} = 0 V) (Note 3) (I_S = 4.0 A, V_{GS} = 0 V) (I_S = 4.5 A, V_{GS} = 0 V, T_J = 125°C)	V_{SD}	− − −	0.86 0.845 0.725	1.2 − −	V
Reverse Recovery Time	(I_S = 4.5 A, V_{GS} = 0 V, dI_S/dt = 100 A/µs) (Note 3)	t_{rr}	−	700	−	ns
		t_a	−	200	−	
		t_b	−	500	−	
Reverse Recovery Stored Charge		Q_{RR}	−	6.5	−	µC
ESD CHARACTERISTICS						
Electro−Static Discharge Capability	Human Body Model (HBM)	ESD	5000	−	−	V
	Machine Model (MM)		500	−	−	

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

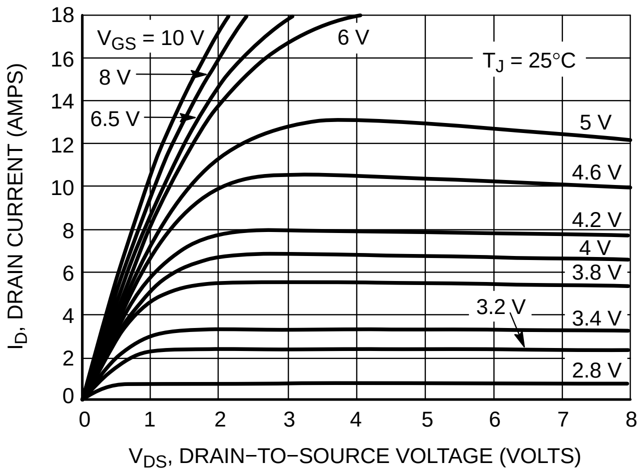


Figure 1. On−Region Characteristics

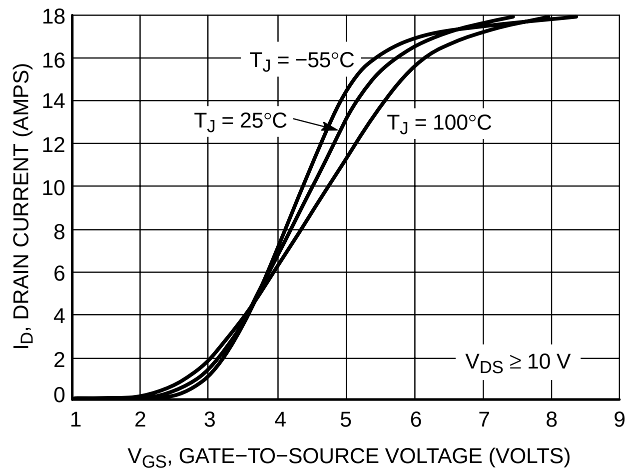


Figure 2. Transfer Characteristics

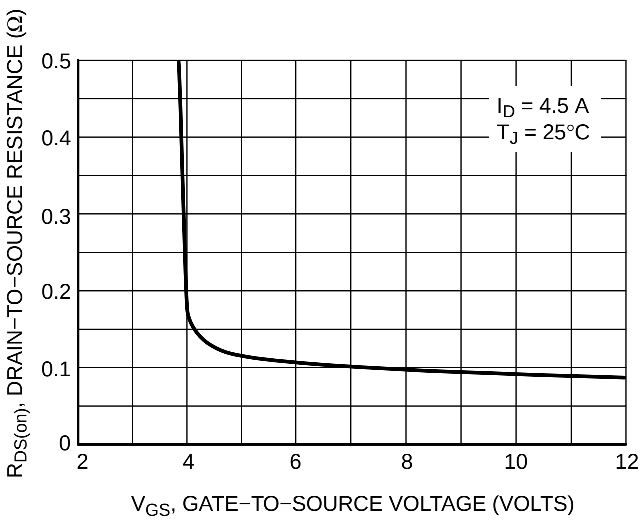


Figure 3. On−Resistance versus Gate−to−Source Voltage

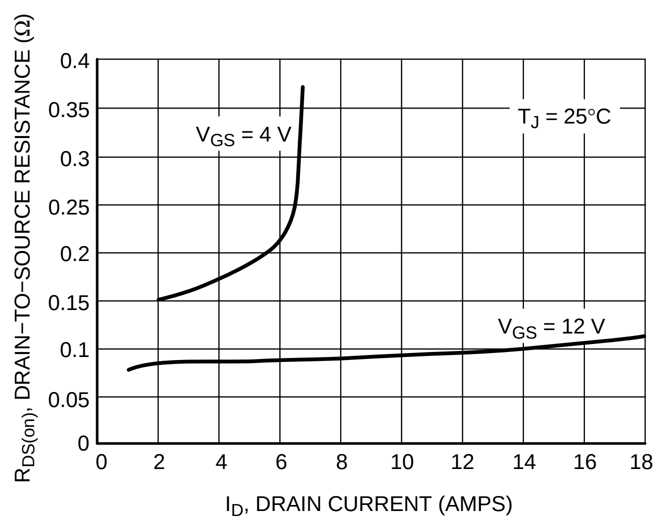


Figure 4. On−Resistance versus Drain Current and Gate Voltage

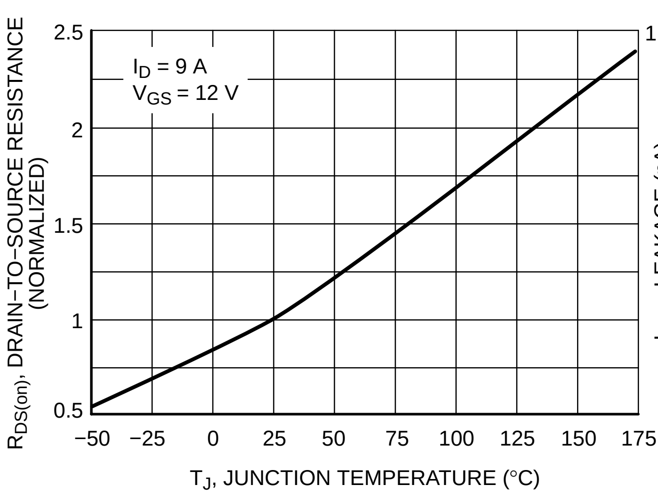


Figure 5. On−Resistance Variation with Temperature

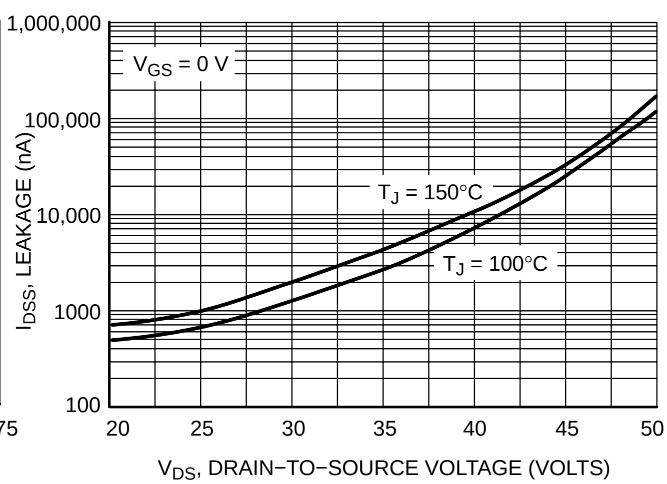


Figure 6. Drain−to−Source Leakage Current versus Voltage

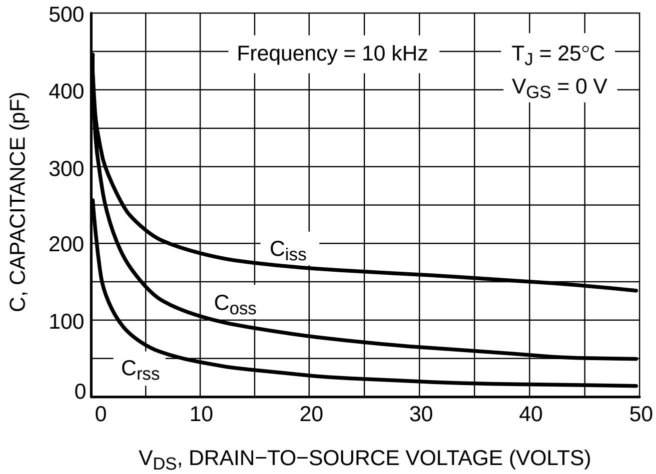


Figure 7. Capacitance Variation

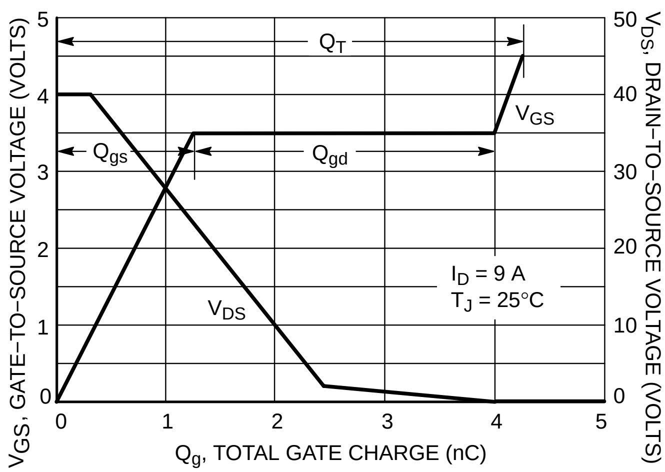


Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge

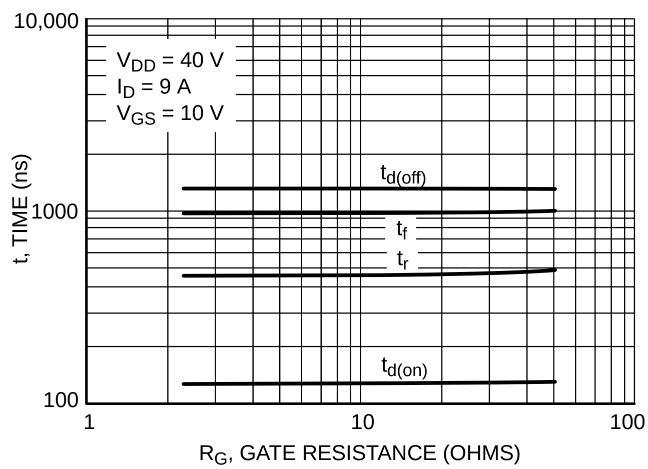


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN−TO−SOURCE DIODE CHARACTERISTICS

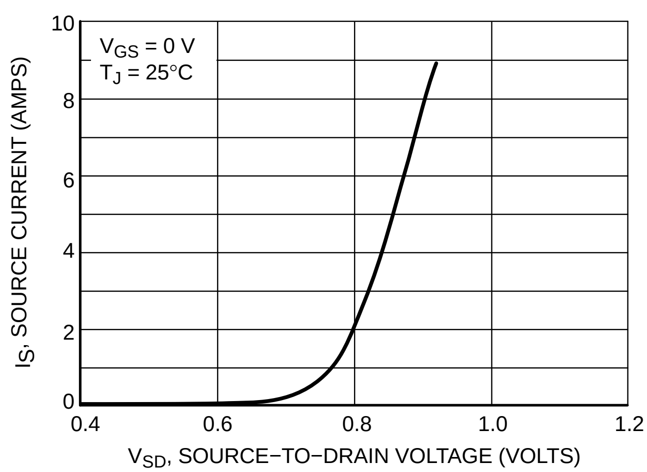


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain−to−source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance − General Data and Its Use."

Switching between the off−state and the on−state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E−FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non−linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E−FETs can withstand the stress of drain−to−source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

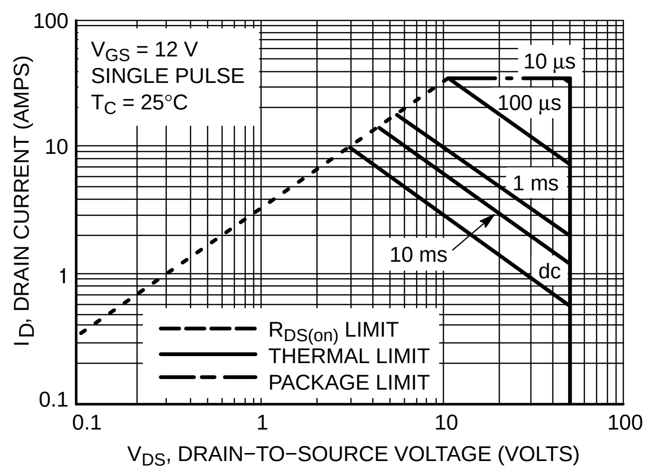


Figure 11. Maximum Rated Forward Biased Safe Operating Area

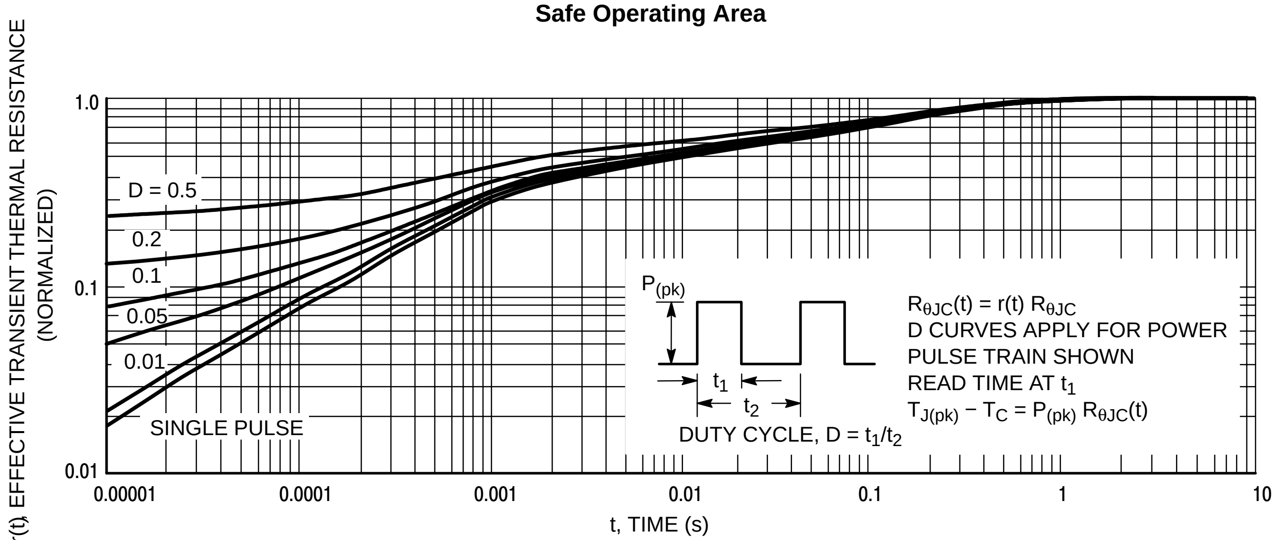
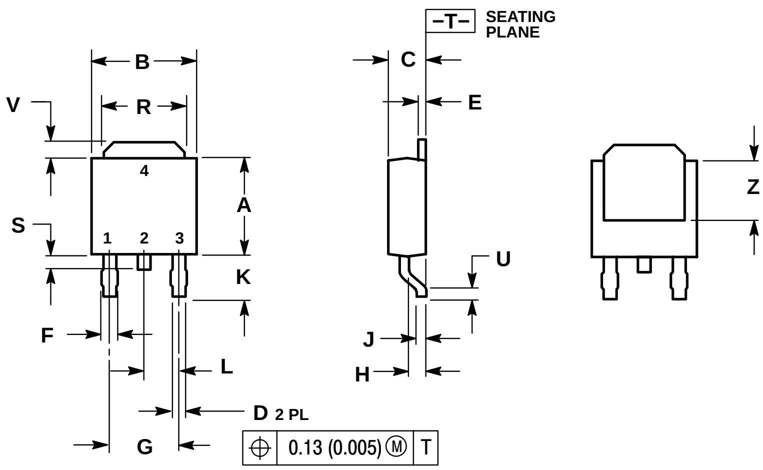


Figure 12. Thermal Response

NID9N05CL

PACKAGE DIMENSIONS

DPAK
CASE 369C−01
ISSUE O

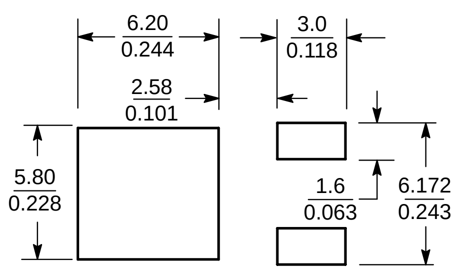


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



SCALE 3:1 (mm / inches)

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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