High speed Driver with bootstrapping for dual Power MOSFETs

P-DSO-14-3

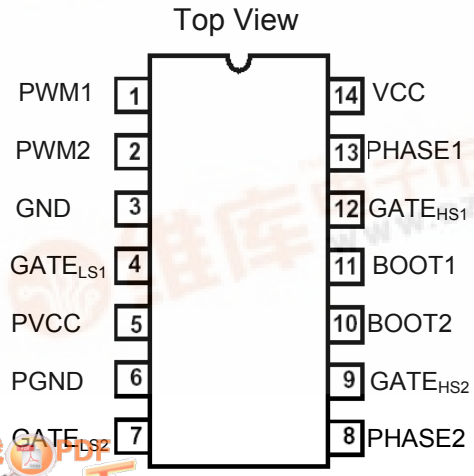
Features

- Fast rise and fall times for frequencies up to 2 MHz
- Capable of sinking more than 4 A peak current for lowest switching losses
- Charges the High Side and Low Side MOSFET´s gate to 6..12 V according to PVCC setting.
- Adjustable High Side and Low Side MOSFET gate drive voltage via PVCC pin for optimizing ON losses and gate drive losses
- Integrates the bootstrap diode for reducing the part count
- Prevents from cross-conducting by adaptive gate drive control
- High voltage rating on Phase node
- Supports shut-down mode for very low quiescent current through three-state input
- Compatible to standard PWM controller ICs (Intersil, Analog Devices)
- Floating High Side MOSFET drive
  - Ideal for multi-phase Desktop CPU supplies on motherboards and VRM´s

Type	Package	Marking	Ordering Code
TDA21102	P-DSO-14-3	21102	Q67042-S4244

Pinout

Top View



Number	Name	Description
1	PWM1	Input for the PWM1 controller signal
2	PWM2	Input for the PWM2 controller signal
3	GND	Ground
4	$GATE_{LS1}$	Gate drive output for the N-Channel Low Side MOSFET 1.
5	PVCC	Input to adjust the High Side gate drive
6	PGND	Power ground return for the Low Side Drivers
7	$GATE_{LS2}$	Gate drive output for the N-Channel Low Side MOSFET 2.
8	PHASE2	To be connected to the junction of the High Side and the Low Side MOSFET 2
9	$GATE_{HS2}$	Gate drive output for the N-Channel High Side MOSFET 2.
10	BOOT2	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 2.
11	BOOT1	Floating bootstrap pin. To be connected to the external bootstrap capacitor to generate the gate drive voltage for the High Side N-Channel MOSFET 1.
12	$GATE_{HS1}$	Gate drive output for the N-Channel High Side MOSFET 1.
13	PHASE1	To be connected to the junction of the High Side and the Low Side MOSFET 1
14	VCC	Supply Voltage

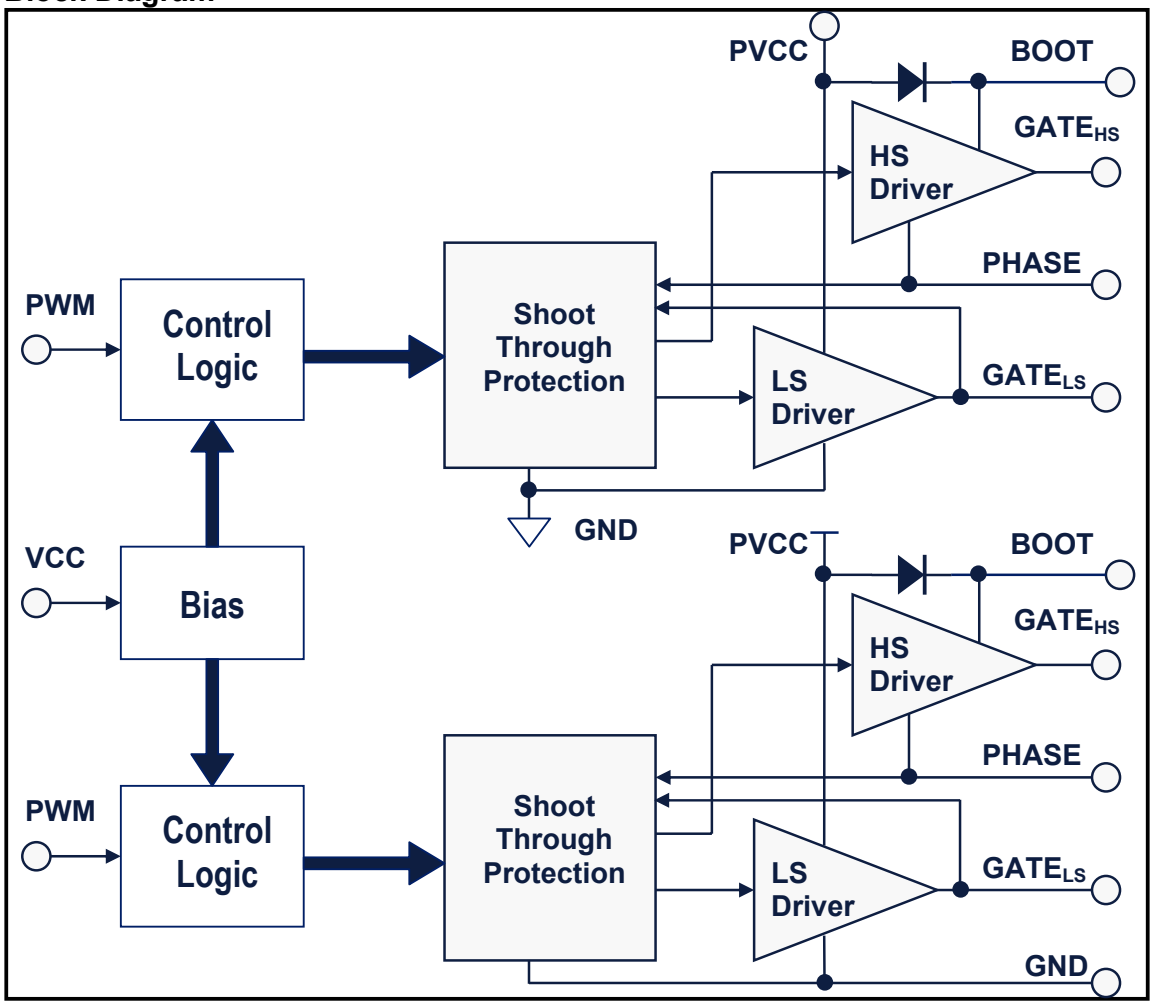
General Description

The dual high speed driver is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges. It has a small propagation delay from input to output, short rise and fall times and the same pin configuration as the HIP6602B. In addition it provides several protection features as well as a shut down mode for efficiency reasons. The high breakdown voltage makes it suitable for mobile applications.

Target application

The dual high speed driver is designed to work well in half-bridge type circuits where dual N-Channel MOSFETs are utilized. A circuit designer can fully take advantage of the driver´s capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM´s but also in motor drive and class-D amplifier type applications.

Block Diagram



Absolute Maximum Ratings

At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Value		Unit
		Min.	Max.	
Voltage supplied to 'VCC' pin	V_{VCC}	-0.3	25	V
Voltage supplied to 'PVCC' pin	V_{PVCC}	-0.3	25	
Voltage supplied to 'PWM' pin	V_{PWM}	-0.3	5.5	
Voltage supplied to 'BOOT' pin referenced to 'PHASE'	$V_{BOOT} - V_{PHASE}$	-0.3	25	
Voltage rating at 'PHASE' pin, DC	V_{PHASE}	-1	25	
Voltage rating at 'PHASE' pin, t_{pulse_max} =500ns Max Duty Cycle = 2%		-20	30	
Junction temperature	T_J	-25	150	°C
Storage temperature	T_S	-55	150	
ESD Rating; Human Body Model			4	kV
IEC climatic category; DIN EN 60068-1		55/150/56		-

Thermal Characteristic

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction-case	Rth-JC		44,7		K/W
Thermal resistance, junction-ambient	Rth-JA		116,2		

Electrical Characteristic

At Tj = 25 °C, unless otherwise specified

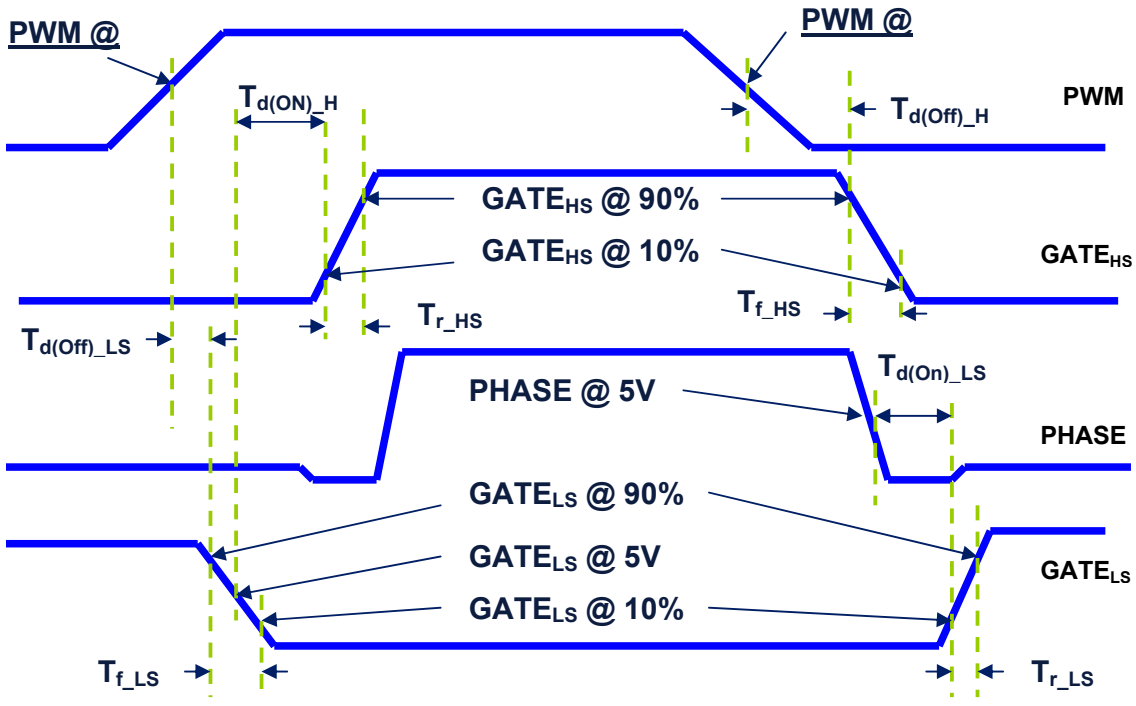
Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Supply Characteristic						
Bias supply current	I_{VCC}	f = 1 MHz, NO LOAD $V_{PVCC} = V_{VCC}$ = 12 V		0.95	1.65	mA
Quiescent current	I_{VCCQ}	1.8 V ≤ V_{PWM} ≤ 3.0 V		0.75	3	
Power supply current	I_{PVCC}	f = 1 MHz, NO LOAD $V_{PVCC} = V_{VCC}$ = 12 V		26		
Under-voltage lockout		V_{VCC} rising threshold	9.7	10.1	10.5	V
Under-voltage lockout		V_{VCC} falling threshold	7.3	7.6	8.0	V
Input Characteristic						
Current in 'PWM' pin	I_{PWM_L}	V_{PWM} = 0.4 V	-80	115	-150	µA
Current in 'PWM' pin	I_{PWM_H}	V_{PWM} = 4.5 V	120	180	250	
Shut down window	V_{IN_SHUT}	t_{SHUT} > 320 ns	1.7		3.1	V
Shut down hold-off time	t_{SHUT}	1.7 V ≤ V_{PWM} ≤ 3.1 V	100	230	350	ns
PWM pin open	V_{PWM_O}		1.8	2.0	2.2	

PWM Low level threshold (falling)	V_{PWM_L}		1.45	1.55		V
PWM High level threshold (rising)	V_{PWM_H}			3.45	3.6	
Pulse Width High Side	$t_{\_p}$	= Pulse with on PWM pin	40			ns

At Tj = 25 °C, unless otherwise specified

Dynamic Characteristic						
Turn-on propagation Delay High Side*	$t_{d(ON)\_HS}$	P_{PVCC} = V_{VCC}= 12 V C_{ISS} = 3000 pF		27	35	ns
Turn-off propagation delay High Side	$t_{d(OFF)\_HS}$			16	21	
Rise time High Side	t_{r_HS}			20	25	
Fall time High Side	t_{f_HS}			11	20	
Turn-on propagation Delay Low Side	$t_{d(ON)\_LS}$			20	23	
Turn-off propagation delay Low Side	$t_{d(OFF)\_LS}$			13	20	
Rise time Low Side	t_{r_LS}			22	25	
Fall time Low Side	t_{f_LS}			13	20	

Measurement Timing diagram



Operating Conditions

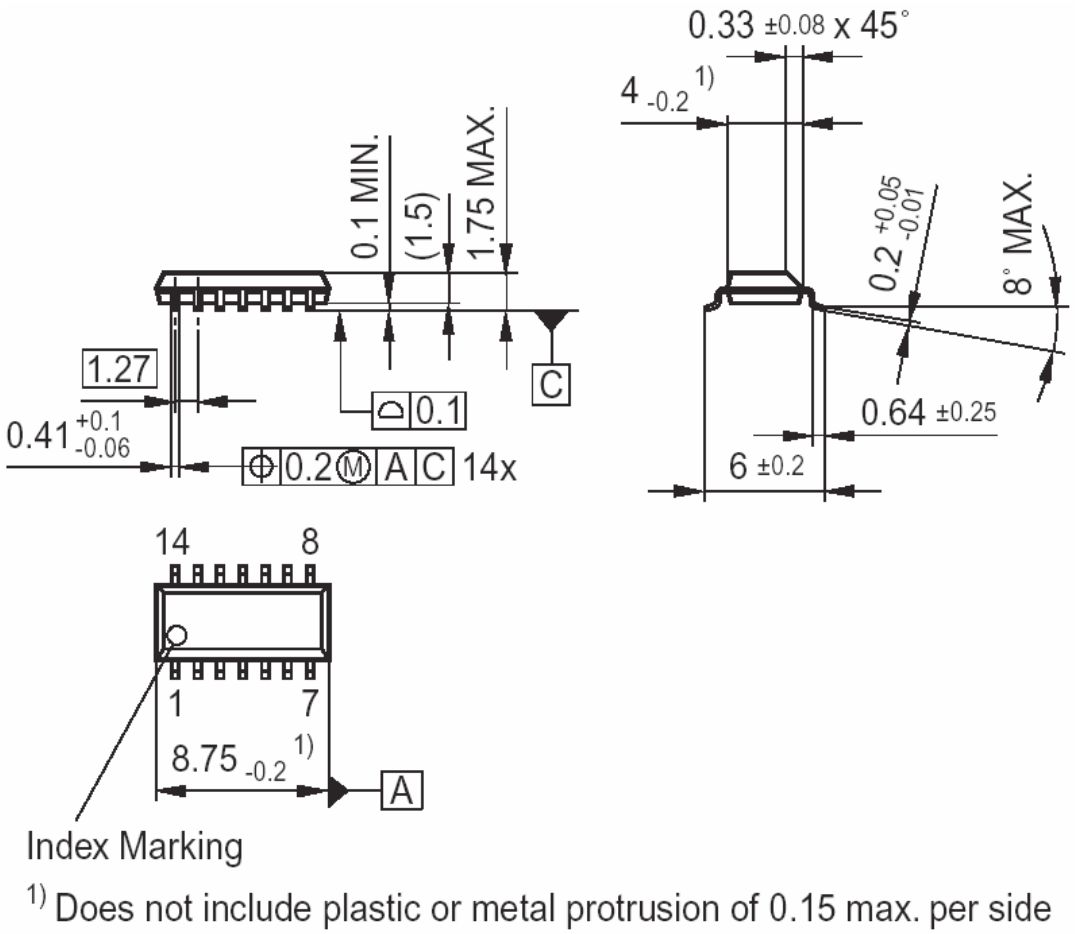
At Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Voltage supplied to 'VCC' pin	V_{VCC}		10.8		13.2	V
Voltage supplied to 'PVCC' pin	V_{PVCC}		6		13.2	V
Input signal transition frequency	f		0.1		2	MHz
Power dissipation	P_{TOT}	T_A = 25 °C, T_J = 125 °C		0.9		W
Junction temperature	T_J		-25		150	°C

At Tj = 25 °C, unless otherwise specified

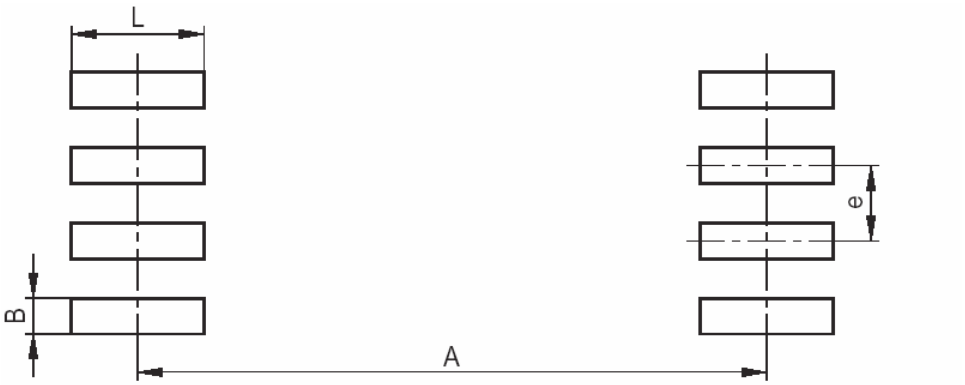
Parameter		Conditions	Values			Unit
			Min.	Typ.	Max.	
Output Characteristic High Side (HS) and Low Side (LS), ensured by design						
Output Resistance	HS; Source	P_{PVCC} = V_{VCC}= 12 V $I_{\_HS\_SRC}$ = 2 A		1.2		Ω
	HS; Sink	P_{PVCC} = V_{VCC}= 12 V		1	1.5	Ω
	LS; Source	P_{PVCC} = V_{VCC}= 12 V I_{HS_SRC} = 2 A		1		Ω
	LS; Sink	P_{PVCC} = V_{VCC}= 12 V		1	1.3	Ω
Peak output-current	HS; Source	P_{PVCC} = V_{VCC}= 12 V $t_{\_P\_HS}$ / Pulse < 20 ns $t_{\_P\_LS}$ / Pulse < 40 ns $D_{\_HS}$ < 2%, $D_{\_LS}$ < 4%	4			A
	HS; Sink		4			
	LS; Source		4			
	LS; Sink		4			

Package Drawing P-DSO-14-3



1) Does not include plastic or metal protrusion of 0.15 max. per side

Layout Footprints



e	A	L	B
1,27 mm	5,69 mm	1,31 mm	0,65 mm

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