HORIZONTAL COMBINATION

The TDA2594 is a monolithic integrated circuit intended for use in colour television receivers. The circuit incorporates the following functions:

- Horizontal oscillator based on the threshold switching principle.
- Phase comparison between sync pulse and oscillator voltage (φ_1).
- Internal key pulse for phase detector (φ_1) (additional noise limiting).
- Phase comparison between line flyback pulse and oscillator voltage (φ_2).
- Larger catching range obtained by coincidence detector (φ_3; between sync and key pulse).
- Switch for changing the filter characteristic and the gate circuit (VCR-operation).
- Sync separator.
- Noise separator.
- Vertical sync separator and output stage.
- Colour burst keying and line flyback blanking pulse generator and clamp circuit for vertical blanking.
- Phase shifter for the output pulse.
- Output pulse duration for transistor deflection systems.
- External switching off of the line trigger pulse.
- Output stage with separate supply voltage.
- Low supply voltage protection.
- Transmitter identification and muting circuit, and vertical sync switch-off.

QUICK REFERENCE DATA

Supply voltage	$V_{1\text{-}18} = V_S$	typ.	12 V
Supply current	I_1	typ.	30 mA
Input signals			
Sync separator input voltage (peak-to-peak value)	$V_{11\text{-}18(p\text{-}p)}$	typ.	3 V*
Noise separator input voltage (peak-to-peak value)	$V_{12\text{-}18(p\text{-}p)}$	typ.	3 V*
Pulse duration switch input voltage			
at t = 14 μs + t_d (transistor driving)	$V_{4\text{-}18}$		0 to 3,5 V
at t = 0 ($V_{3\text{-}18}$ = 0); input 4 open (I_4 = 0)	$V_{4\text{-}18}$		5,4 to 6,6 V
Output signals			
Vertical sync output pulse (peak-to-peak value)	$V_{8\text{-}18(p\text{-}p)}$	typ.	11 V
Burst key output pulse (peak-to-peak value)	$V_{7\text{-}18(p\text{-}p)}$	typ.	11 V
Line drive-pulse (peak-to-peak value)	$V_{3\text{-}18(p\text{-}p)}$	typ.	10 V

* Permissible range: 1 to 7 V.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT102).

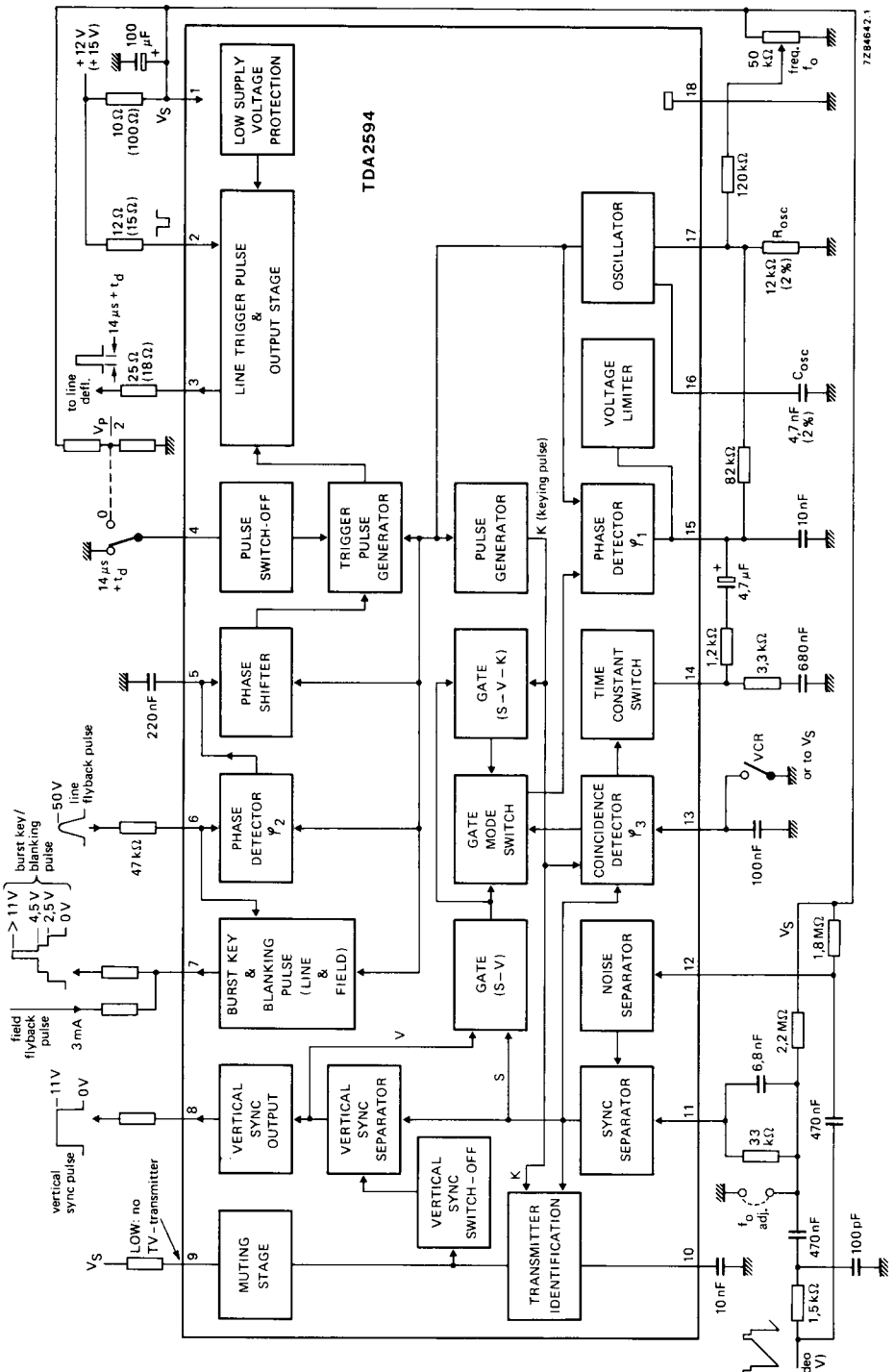

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
at pin 1 (voltage source)	$V_{1-18} = V_S$	max.	13,2	V
at pin 2	V_{2-18}	max.	18	V
Voltages				
Pin 4	V_{4-18}	max.	13,2	V
Pin 9	V_{9-18}	max.	18	V
	$-V_{9-18}$	max.	0,5	V
Pin 11	$\pm V_{11-18}$	max.	6	V
Pin 12	$\pm V_{12-18}$	max.	6	V
Pin 13	V_{13-18}	max.	13,2	V
Currents				
Pins 2 and 3 (transistor driving) (peak value)	$I_{2M}, -I_{3M}$	max.	400	mA
Pin 4	I_4	max.	1	mA
Pin 6	$\pm I_6$	max.	10	mA
Pin 7	$-I_7$	max.	5	mA
Pin 9	I_9	max.	10	mA
Pin 13	I_{13}	max.	2	mA
Total power dissipation	P_{tot}	max.	800	mW
Storage temperature range	T_{stg}		−25 to +125	°C
Operating ambient temperature range	T_{amb}		0 to +70	°C

CHARACTERISTICS at $V_{1-18} = 12$ V; $T_{amb} = 25$ °C; measured in Fig. 1

Sync separator (pin 11)

Input switching voltage	V_{11-18}	typ.	0,8	V
Input keying current	I_{11}		5 to 100	μA
Input leakage current at $V_{11-18} = -5$ V	I_{11}	⩽	1	μA
Input switching current	I_{11}	⩽	5	μA
Switch off current	I_{11}	⩾	100	μA
		typ.	150	μA
Input signal (peak-to-peak value)	$V_{11-18(p-p)}$		3 to 4	V*

* Permissible range 1 to 7 V.

Noise separator (pin 12)				
Input switching voltage	V_{12-18}	typ.	1,4	V
Input keying current	I_{12}		5 to 100	μA
Input switching current	I_{12}	⩾	100	μA
		typ.	150	μA
Input leakage current at $V_{12-18} = -5$ V	I_{12}	⩽	1	μA
Input signal (peak-to-peak value)	$V_{12-18(p-p)}$		3 to 4	V*
Permissible superimposed noise signal (peak-to-peak value)	$V_{12-18(p-p)}$	⩽	7	V
Line flyback pulse (pin 6)				
Input current	I_6	⩾	0,02	mA
		typ.	1	mA
Input switching voltage	V_{6-18}	typ.	1,4	V
Input limiting voltage	V_{6-18}		−0,7 to +1,4	V
Switching on VCR (pin 13)				
Input voltage	V_{13-18}		0 to 2,5	V
	or: V_{13-18}		9 to V_S	V
Input current	$-I_{13}$	⩽	200	μA
	or: I_{13}	⩽	2	mA
Pulse switching off (pin 4)				
For t = 0; input pin 4 open or $V_{3-18} = 0$				
Input voltage	V_{4-18}		5,4 to 6,6	V
Input current	I_4	typ.	0	μA
Vertical sync pulse (positive-going) (pin 8)				
Output voltage (peak-to-peak value)	$V_{8-18(p-p)}$	⩾	10	V
		typ.	11	V
Output resistance	R_8	typ.	2	kΩ
Delay between leading edge of input and output signal	t_{on}	typ.	15	μs
Delay between trailing edge of input and output signal	t_{off}	⩾	t_{on}	μs
Switching off the vertical sync pulse	V_{10-18}	⩽	3	V
Burst key pulse (positive-going) (pin 7)				
Output voltage	V_{7-18}	⩾	10	V
		typ.	11	V
Output resistance	R_7	typ.	70	Ω
Pulse duration; $V_{7-18} = 7$ V	t_p	typ.	4	μs
			3,7 to 4,3	μs
Phase relation between middle of sync pulse at the input and the leading edge of the burst key pulse; $V_{7-18} = 7$ V	t	typ.	2,65	μs
			2,15 to 3,15	μs
Output trailing edge current	I_7	typ.	2	mA
Saturation voltage during line scan	V_{7-18}	⩽	1	V

* Permissible range 1 to 7 V

Line flyback-blanking pulse (positive-going) (pin 7)

Output voltage	$V_{7\text{-}18}$	4,1 to 4,9	V
Output resistance	R_7	typ. 70	Ω
Output trailing edge current	I_7	typ. 2	mA

Field flyback/blanking pulse (pin 7)

Output voltage with externally forced in current I_7 = 2,4 to 3,6 mA	$V_{7\text{-}18}$	2 to 3	V
Output resistance at I_7 = 3 mA	R_7	typ. 70	Ω

TV-transmitter identification output (pin 9; open collector)

Output voltage at I_9 = 3 mA; no TV-transmitter	$V_{9\text{-}18}$	⩽ 0,5	V
Output resistance at I_9 = 3 mA; no TV-transmitter	R_9	⩽ 100	Ω
Output current at $V_{10\text{-}18} \geqslant 3$ V; TV-transmitter identified	I_9	⩽ 5	μA

TV-transmitter identification (pin 10)

When receiving a TV signal the voltage $V_{10\text{-}18}$ will change from ⩽ 1 V to ⩾ 7 V.

Line drive pulse (positive-going)

Output voltage (peak-to-peak value)	$V_{3\text{-}18(p\text{-}p)}$	typ. 10	V
Output resistance			
for leading edge of line pulse	R_3	typ. 2,5	Ω
for trailing edge of line pulse	R_3	typ. 20	Ω
Pulse duration (transistor driving) $V_{4\text{-}18}$ = 0 to 3,5 V; $-I_4 \geqslant 200$ μA; t_{fp} = 12 μs	t_p	$14 + t_d$	μs*
Supply voltage for switching off the output pulse	$V_{1\text{-}18}$	typ. 4	V

Overall phase relation

Phase relation between middle of sync pulse and the middle of the flyback pulse	Δt	typ. 2,6 ± 0,7	μs**

The adjustment of the overall phase relation and consequently the leading edge of the line drive pulse occurs automatically by phase control φ_2.

If additional adjustment is applied it can be arranged by current supply at pin 5, such that:

Supplying current	$\Delta I/\Delta t$	typ. 30	μA/μs

* t_d = switch-off delay of line output stage.

** Line flyback pulse duration t_{fp} = 12 μs.

Oscillator (pins 16 and 17)				
Threshold voltage low level	$V_{16\text{-}18}$	typ.	4,4	V
Threshold voltage high level	$V_{16\text{-}18}$	typ.	7,6	V
Charging current	$\pm I_{16}$	typ.	0,47	mA
Frequency; free running (C_{osc} = 4,7 nF; R_{osc} = 12 kΩ)	f_o	typ.	15,625	kHz
Spread of frequency	Δf_o	⩽	± 5	%▲
Frequency control sensitivity	$\Delta f_o/\Delta_{17}$	typ.	31	Hz/μA
Adjustment range of network in circuit (Fig. 1)	Δf_o	typ.	± 10	%
Influence of supply voltage on frequency; reference at V_S = 12 V	$\frac{\Delta f_o/f_o}{\Delta V/V_{nom}}$	⩽	± 0,05	%▲
Change of frequency when V_S drops to 5 V; reference at V_S = 12 V	Δf_o	⩽	± 10	%▲
Temperature coefficient of oscillator frequency	TC	⩽	$\pm 10^{-4}$	K^{-1}▲
Phase comparison φ_1 (pin 15)				
Control voltage range	$V_{15\text{-}18}$		4,1 to 7,9	V
Control current (peak value)	$\pm I_{15M}$		1,8 to 2,2	mA
Output leakage current at $V_{15\text{-}18}$ = 4,3 to 7,7 V	I_{15}	⩽	1	μA
Output resistance				
at $V_{15\text{-}18}$ = 4,3 to 7,7 V	R_{13}	high ohmic		*
at $V_{15\text{-}18} \leqslant$ 4,1 V or $\geqslant$ 7,9 V	R_{13}	low ohmic		**
Control sensitivity		typ.	2	kHz/μs
Catching and holding range (82 kΩ between pins 15 and 17)	Δf	typ.	± 680	Hz
Spread of catching and holding range	Δ(Δf)	typ.	± 12	%▲
Phase comparison φ_2 and phase shifter (pin 5)				
Control voltage range	$V_{5\text{-}18}$		5,4 to 7,6	V
Control current (peak value)	$\pm I_{5M}$	typ.	1	mA
Output resistance at $V_{5\text{-}18}$ = 5,4 to 7,6 V	R_5	high ohmic		*
Input leakage current at $V_{5\text{-}18}$ = 5,4 to 7,6 V	I_5	⩽	5	μA
Permissible delay between leading edge of output pulse and leading edge of flyback pulse (t_{fp} = 12 μs)	t_d	⩽	15,5	μs
Static control error	$\Delta t/\Delta t_d$	⩽	0,2	%
Coincidence detector φ_3 (pin 13)				
Output voltage	$V_{13\text{-}18}$		0,5 to 6	V
Output current (peak value)				
without coincidence	I_{13M}	typ.	0,1	mA
with coincidence	$-I_{13M}$	typ.	0,5	mA

* Current source.
** Emitter follower.
▲ Excluding external component tolerances

Time constant switch (pin 14)

Output voltage	$V_{14\text{-}18}$	typ.	6 V
Output current (limited)	$\pm I_{14}$	typ.	1 mA
Output resistance			
at $V_{13\text{-}18} = 3{,}5$ to 7 V	R_{14}	typ.	0,1 kΩ
at $V_{13\text{-}18} \leqslant 2{,}5$ V or $\geqslant 9$ V	R_{14}	typ.	60 kΩ

Internal keying pulse

Pulse duration	t_p	typ.	7,5 μs