INTEGRATED CIRCUITS

# DATA SHEET

# TDA3617
## Multiple voltage regulator

Preliminary specification
File under Integrated Circuits, IC01

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Philips Semiconductors

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## FEATURES

### General

- Three $V_P$-state controlled regulators (regulators 1, 2 and 3)
- Very good stability and noise behaviour
- Separate control pins for switching regulators 1, 2 and 3
- Supply voltage range from –18 to +50 V
- Low quiescent current (when regulators 1, 2 and 3 are switched off)
- High ripple rejection
- Hold output for indicating regulator 1 and/or 2 and/or 3 out of regulation.

### Protections

- Reverse polarity safe (down to –18 V without high reverse current)
- Able to withstand voltages up to 18 V at the outputs (supply line may be short circuited)
- ESD protection on all pins
- Thermal protection
- Load dump protection
- Foldback current limit protection for regulators 1, 2 and 3
- DC short-circuit safe to ground and $V_P$ for all regulator outputs.

## GENERAL DESCRIPTION

The TDA3617J is a multiple output voltage regulator with three independent regulators. It contains:

1. Three fixed voltage regulators with foldback current protection (regulators 1, 2 and 3)
2. A supply pin that can withstand load dump pulses and negative supply voltages
3. Independent enable inputs for regulators 1, 2 and 3
4. Local temperature protection for regulator 3
5. A hold output that can be used to interface with a microprocessor. The hold indicates that the selected output voltages are available and within their ranges.

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| $V_P$ | supply voltage | | | | | |
| | operating | | 9.5 | 14.4 | 17.5 | V |
| | jump start | $t \leq 10$ minutes | – | – | 30 | V |
| | load dump protection | for 50 ms; $t_r \geq 2.5$ ms | – | – | 50 | V |
| $I_{q(tot)}$ | total quiescent current | standby mode | – | 5 | 40 | μA |
| $T_j$ | junction temperature | | – | – | 175 | °C |
| **Voltage regulators** | | | | | | |
| $V_{REG1}$ | output voltage regulator 1 | 1 mA ≤ $I_{REG1}$ ≤ 1.3 A | 8.55 | 9.0 | 9.45 | V |
| $V_{REG2}$ | output voltage regulator 2 | 1 mA ≤ $I_{REG2}$ ≤ 600 mA; $V_P$ = 14.4 V | 4.75 | 5.0 | 5.25 | V |
| $V_{REG3}$ | output voltage regulator 3 | 1 mA ≤ $I_{REG3}$ ≤ 300 mA | 3.14 | 3.3 | 3.46 | V |

## ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|---|---|---|---|
| | NAME | DESCRIPTION | VERSION |
| TDA3617J | DBS9P | plastic DIL-bent-SIL power package; 9 leads (lead length 7.7 mm) | SOT157-4 |

## BLOCK DIAGRAM

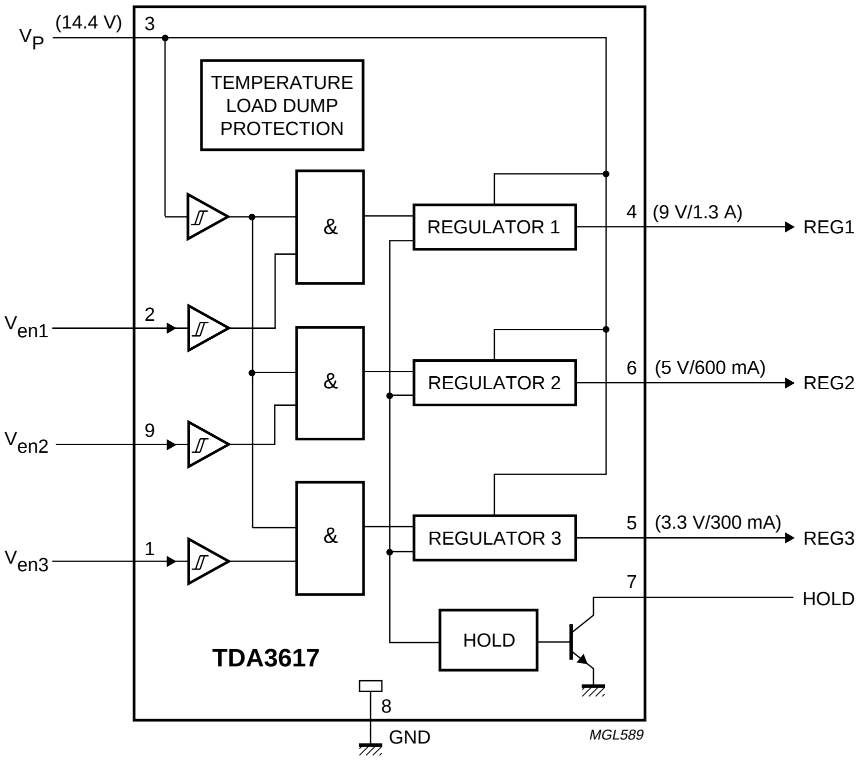



Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| $V_{en3}$ | 1 | enable input regulator 3 |
| $V_{en1}$ | 2 | enable input regulator 1 |
| $V_P$ | 3 | supply voltage |
| REG1 | 4 | regulator 1 output |
| REG3 | 5 | regulator 3 output |
| REG2 | 6 | regulator 2 output |
| HOLD | 7 | hold output |
| GND | 8 | ground |
| $V_{en2}$ | 9 | enable input regulator 2 |

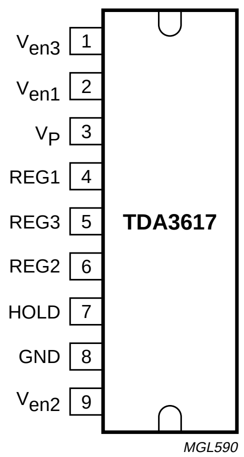



Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The TDA3617J is a multiple output voltage regulator with three independent switchable regulators. When the supply voltage ($V_P$ > 4.5 V) is available, regulators 1, 2 and 3 can be operated by means of three independent enable inputs.

Schmitt trigger functions are included to switch the regulators off at low battery voltage ($V_P$ < 4 V).
A hysteresis is included to avoid random switching.

All output pins are fully protected. The regulators are protected against load dump (the regulators switch off at supply voltages higher than 20 V) and short circuit (foldback current protection).

The TDA3617J has a hold circuit which indicates when one of the regulators is out-of-regulation. The hold function is disabled when all the enable inputs are LOW (TDA3617J in standby mode). The HOLD output (open collector output) can be wired OR-ed with other hold outputs of other regulator parts (e.g. TDA3618). When all the regulators of the TDA3617J are disabled (switched off), the HOLD output will be high ohmic. Because of this feature, the hold will not influence the hold information when wired OR-ed with other regulator parts.

Figure 3 shows the total timing of a semi-on/off logic set. Figure 4 shows the total timing of the HOLD signal.

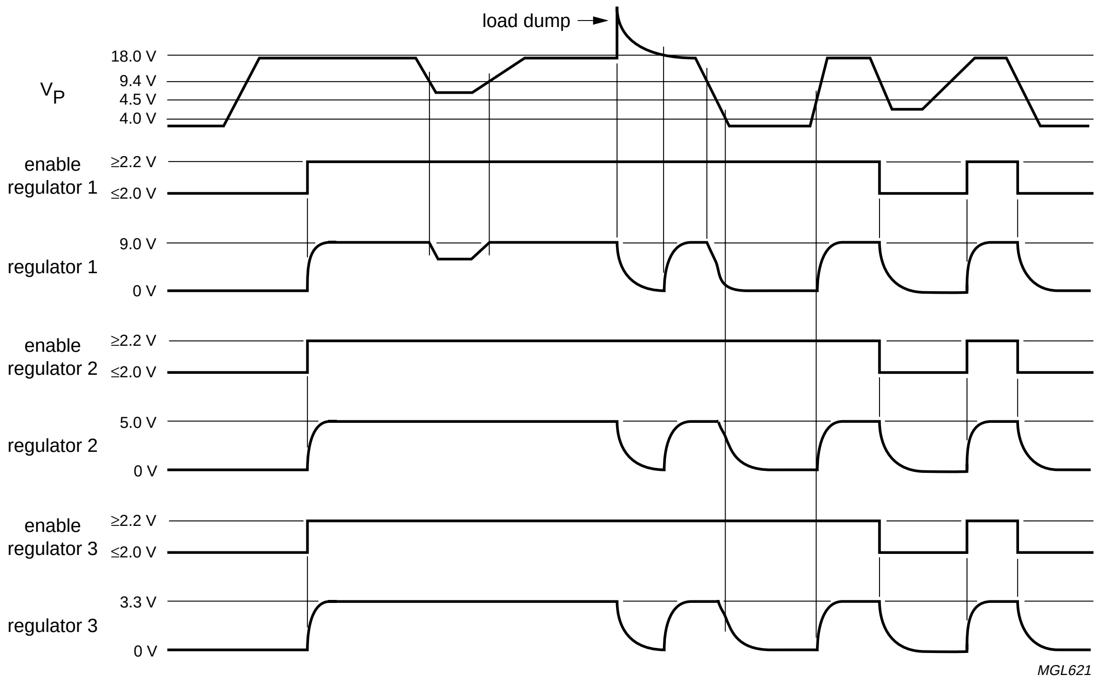



Fig.3 Timing diagrams of a semi-on/off logic set.

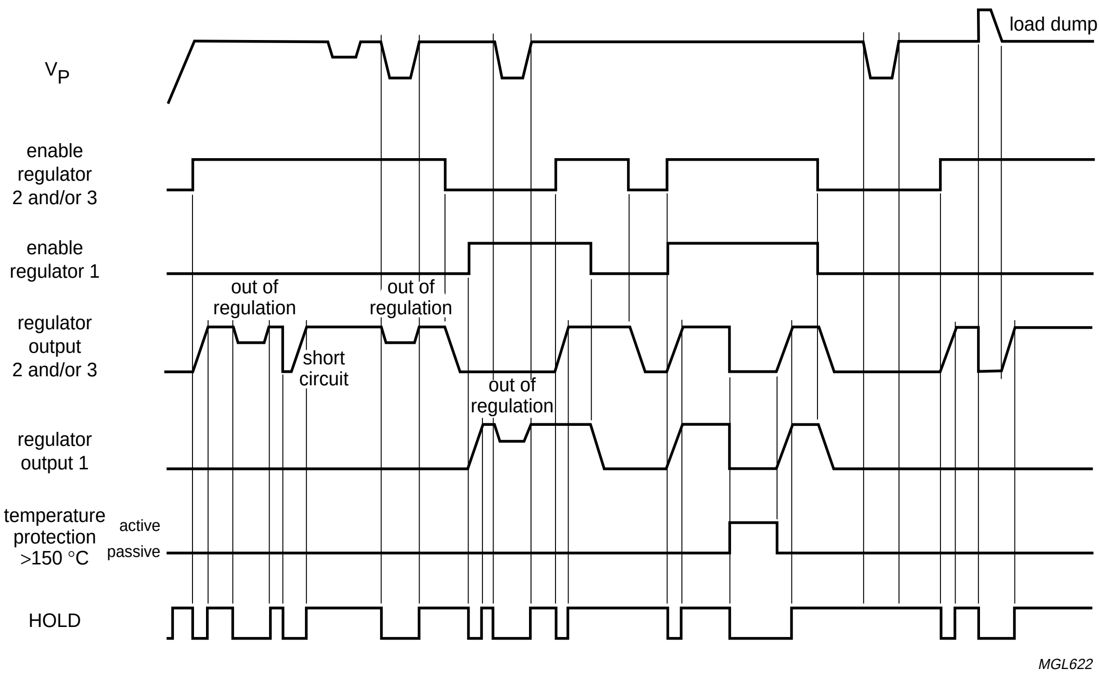



Fig.4 Timing diagrams of the HOLD signal.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_P$ | supply voltage | | | | |
| | operating | | – | 17.5 | V |
| | jump start | t ≤ 10 minutes | – | 30 | V |
| | load dump protection | for 50 ms; $t_r$ ≥ 2.5 ms | – | 50 | V |
| $V_{bat(rp)}$ | reverse polarity battery voltage | non-operating | – | –18 | V |
| $P_{tot}$ | total power dissipation | | – | 62 | W |
| $T_{stg}$ | storage temperature | non-operating | –55 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating | –40 | +85 | °C |
| $T_j$ | junction temperature | operating | – | 175 | °C |

## THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $R_{th(j-c)}$ | thermal resistance from junction to case | regulator and switch-on | 2 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 50 | K/W |

## QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611-E”*. The number of the quality specification can be found in the *“Quality Reference Handbook”*.

## CHARACTERISTICS

$V_P$ = 14.4 V; $T_{amb}$ = 25 °C; measured in test circuit of Fig.6; unless otherwise specified.

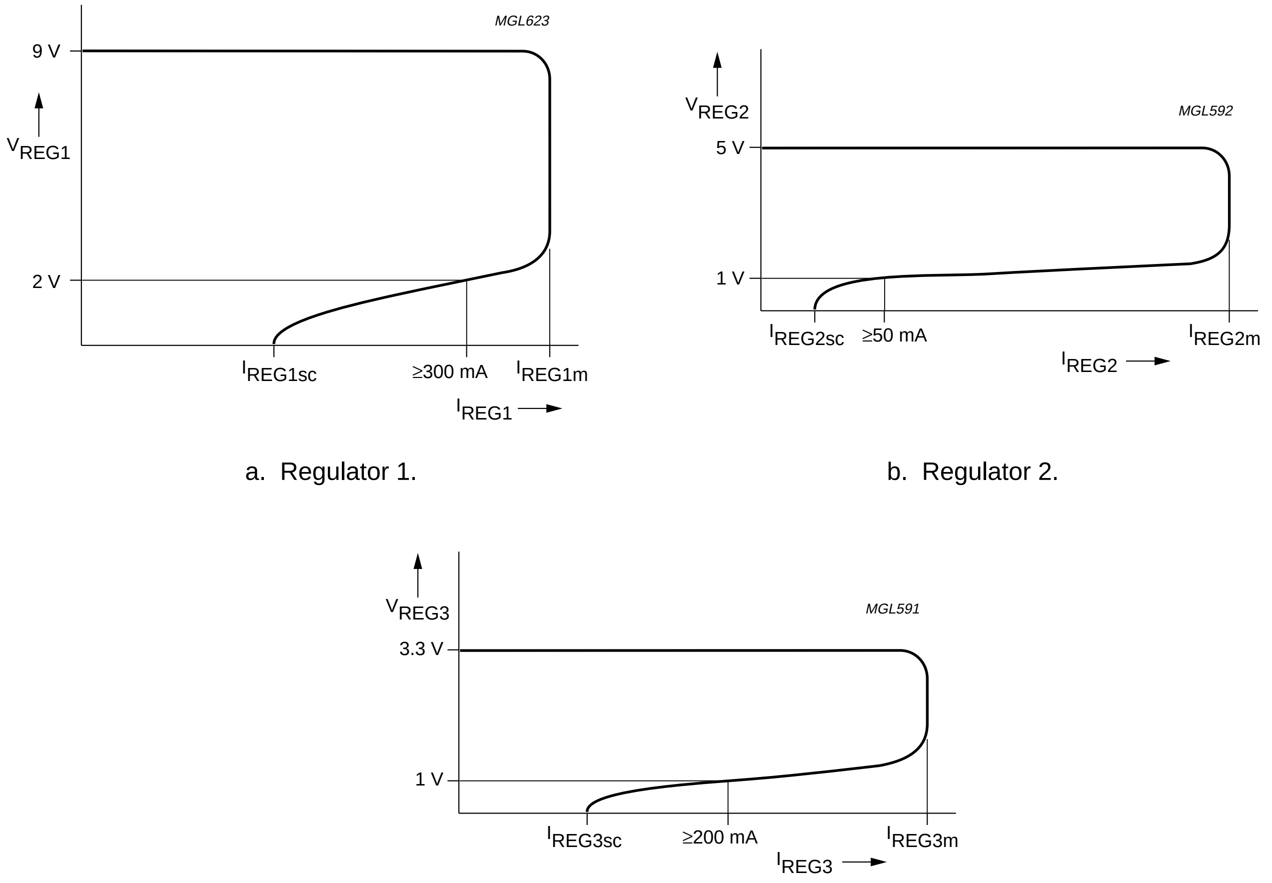
| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_P$ | supply voltage | | | | | |
| | operating | | 9.5 | 14.4 | 17.5 | V |
| | REGn on | note 1 | 6 | 14.4 | 17.5 | V |
| | jump start | t ≤ 10 minutes | – | – | 30 | V |
| | load dump protection | for 50 ms; $t_r$ ≥ 2.5 ms | – | – | 50 | V |
| $I_q$ | quiescent current | $V_P$ = 12.4 V; note 2 | – | 5 | 40 | μA |
| | | $V_P$ = 14.4 V; note 2 | – | 5 | – | μA |
| **Power supply Schmitt trigger for regulators 1, 2 and 3** | | | | | | |
| $V_{thr}$ | rising voltage threshold | $V_{en}$ = 3 V | 6.2 | 6.8 | 7.5 | V |
| $V_{thf}$ | falling voltage threshold | $V_{en}$ = 3 V | 4.0 | 4.5 | 5.0 | V |
| $V_{hys}$ | hysteresis | | 1.5 | 2.3 | 3.0 | V |
| **Enable input (regulators 1, 2 and 3)** | | | | | | |
| $V_{i(off)}$ | off-level input voltage | | –0.2 | | +1.2 | V |
| $V_{i(on)}$ | on-level input voltage | | – | 1.8 | – | V |
| $I_{LI}$ | input leakage current | $V_{en}$ = 5 V | 5 | 30 | 50 | μA |
| **Hold buffer** | | | | | | |
| $I_{sinkL}$ | LOW-level sink current | $V_{HOLD}$ ≤ 0.8 V | 2 | – | – | mA |
| $I_{LO}$ | output leakage current | $V_{HOLD}$ = 5 V | – | 0 | 5 | μA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Regulator 1 ($I_{REG1}$ = 5 mA)** | | | | | | |
| $V_{REG1(off)}$ | output voltage off | | – | 1 | 400 | mV |
| $V_{REG1}$ | output voltage | 1 mA ≤ $I_{REG1}$ ≤ 1.3 A | 8.55 | 9.0 | 9.45 | V |
| | | 10.5 V ≤ $V_P$ ≤ 17.5 V | 8.55 | 9.0 | 9.45 | V |
| $\Delta V_{REG1}$ | line regulation | 10.5 V ≤ $V_P$ ≤ 17.5 V | – | 20 | 50 | mV |
| $\Delta V_{REGL1}$ | load regulation | 1 mA ≤ $I_{REG1}$ ≤ 1.3 A | – | 35 | 70 | mV |
| $I_{qREG1}$ | quiescent current | $I_{REG1}$ = 1.3 A | – | 45 | 110 | mA |
| SVRR1 | supply voltage ripple rejection | f = 3 kHz; $V_{i(p-p)}$ = 2 V | 60 | 70 | – | dB |
| $V_{REG1d}$ | drop-out voltage | $I_{REG1}$ = 1.3 A; note 3 | – | 0.5 | 1 | V |
| $I_{REG1m}$ | current limit | $V_{REG1}$ > 7.5 V; note 4 | 1.3 | 1.4 | – | A |
| $I_{REG1sc}$ | short-circuit current | $R_L$ ≤ 0.5 Ω; note 5 | 250 | 500 | – | mA |
| $\alpha_{ct}$ | cross talk noise | note 6 | – | 25 | 150 | μV |
| **Schmitt trigger for hold of regulator 1** | | | | | | |
| $V_{thr}$ | rising threshold voltage of regulator 1 | $V_P$ rising | – | $V_{REG1}$ – 0.15 | $V_{REG1}$ – 0.075 | V |
| $V_{thf}$ | falling threshold voltage of regulator 1 | $V_P$ falling | 8.1 | $V_{REG1}$ – 0.35 | – | V |
| $V_{hys}$ | hysteresis voltage | | 0.1 | 0.2 | 0.3 | V |
| **Regulator 2 ($I_{REG2}$ = 5 mA)** | | | | | | |
| $V_{REG2(off)}$ | output voltage off | | – | 1 | 400 | mV |
| $V_{REG2}$ | output voltage | 0.5 mA ≤ $I_{REG2}$ ≤ 600 mA | 4.75 | 5.0 | 5.25 | V |
| | | 8 V ≤ $V_P$ ≤ 17.5 V | 4.75 | 5.0 | 5.25 | V |
| $\Delta V_{REG2}$ | line regulation | 8 V ≤ $V_P$ ≤ 17.5 V | – | 2 | 50 | mV |
| $\Delta V_{REGL2}$ | load regulation | 1 mA ≤ $I_{REG2}$ ≤ 600 mA | – | 20 | 85 | mV |
| $I_{qREG2}$ | quiescent current | $I_{REG2}$ = 0.4 A | – | 10 | 40 | mA |
| SVRR2 | supply voltage ripple rejection | f = 3 kHz; $V_{i(p-p)}$ = 2 V | 60 | 70 | – | dB |
| $V_{REG2d}$ | drop-out voltage | $I_{REG2}$ = 600 mA; $V_P$ = 6 V; note 3 | – | 1 | 1.5 | V |
| $I_{REG2m}$ | current limit | $V_{REG2}$ > 4 V; note 4 | 0.65 | 0.8 | – | A |
| $I_{REG2sc}$ | short-circuit current | $R_L$ ≤ 0.5 Ω; note 5 | 100 | 300 | – | mA |
| $\alpha_{ct}$ | cross talk noise | note 6 | – | 25 | 150 | μV |
| **Schmitt trigger for hold of regulator 2** | | | | | | |
| $V_{thr}$ | rising threshold voltage of regulator 2 | $V_P$ rising | – | $V_{REG1}$ – 0.15 | $V_{REG1}$ – 0.075 | V |
| $V_{thf}$ | falling threshold voltage of regulator 2 | $V_P$ falling | 4.3 | $V_{REG1}$ – 0.35 | – | V |
| $V_{hys}$ | hysteresis voltage | | 0.1 | 0.2 | 0.3 | V |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Regulator 3 ($I_{REG3}$ = 5 mA)** | | | | | | |
| $V_{REG3(off)}$ | output voltage off | | – | 1 | 400 | mV |
| $V_{REG3}$ | output voltage | 1 mA ≤ $I_{REG3}$ ≤ 300 mA | 3.14 | 3.3 | 3.46 | V |
| | | 5 V ≤ $V_P$ ≤ 17.5 V | 3.14 | 3.3 | 3.46 | V |
| $\Delta V_{REG3}$ | line regulation | 5 V ≤ $V_P$ ≤ 17.5 V | – | 2 | 50 | mV |
| $\Delta V_{REGL3}$ | load regulation | 1 mA ≤ $I_{REG3}$ ≤ 300 mA | – | 20 | 50 | mV |
| $I_{qREG3}$ | quiescent current | $I_{REG3}$ = 300 mA | – | 10 | 15 | mA |
| SVRR3 | supply voltage ripple rejection | f = 3 kHz; $V_{i(p-p)}$ = 2 V | 60 | 70 | – | dB |
| $I_{REG3m}$ | current limit | $V_{REG3}$ > 3 V; note 4 | 0.35 | 0.45 | – | A |
| $I_{REG3sc}$ | short circuit current | $R_L$ ≤ 0.5 Ω; note 5 | 15 | 50 | – | mA |
| $\alpha_{ct}$ | cross talk noise | note 6 | – | 25 | 150 | µV |
| **Schmitt trigger for hold of regulator 3** | | | | | | |
| $V_{thr}$ | rising threshold voltage of regulator 3 | $V_P$ rising | – | $V_{REG1}$ – 0.15 | $V_{REG1}$ – 0.075 | V |
| $V_{thf}$ | falling threshold voltage of regulator 2 | $V_P$ falling | 2.7 | $V_{REG1}$ – 0.35 | – | V |
| $V_{hys}$ | hysteresis voltage | | 0.1 | 0.2 | 0.3 | V |

**Notes**

1. Minimum operating voltage, only if $V_P$ has exceeded 4.5 V.
2. The quiescent current is measured in the standby mode. Therefore, the enable inputs of regulators 1, 2 and 3 are LOW ($V_{en}$ < 1 V).
3. The drop-out voltage of regulators 1, 2 and 3 is measured between $V_P$ and $V_{REGn}$.
4. At current limit, $I_{REGmn}$ is held constant (see Fig.5 for the behaviour of $I_{REGmn}$).
5. The foldback current protection limits the dissipated power at short circuit (see Fig.5).
6. Perform the load regulation test with sine wave load of 10 kHz on the regulator output under test. Measure the RMS ripple voltage on each of the remaining regulator outputs, using a 80 kHz low-pass filter.




a. Regulator 1.

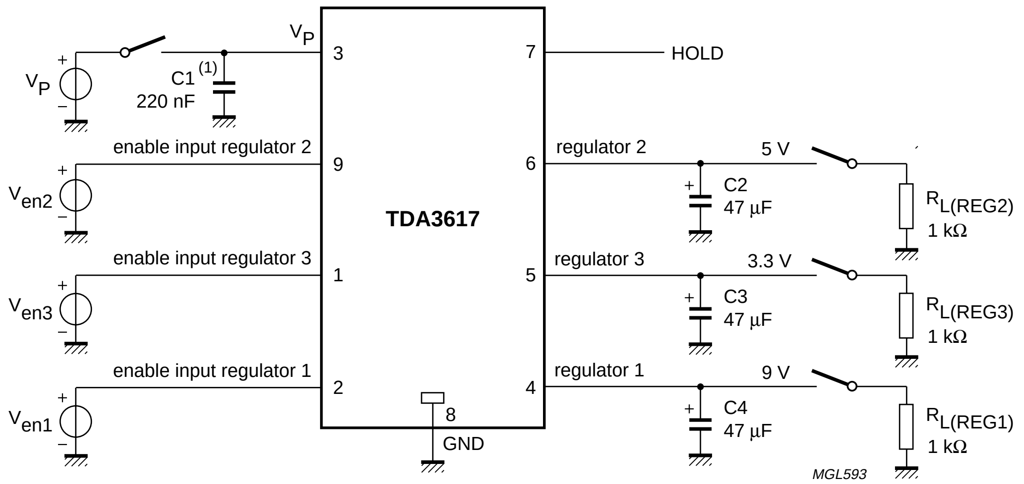
b. Regulator 2.

c. Regulator 3.

Fig.5 Foldback current protection for regulators 1, 2 and 3.

## TEST AND APPLICATION INFORMATION

### Test information




(1) Capacitor not required for stability.

Fig.6 Test circuit.

### Application information

NOISE

**Table 1** Noise figures

| REGULATOR | NOISE FIGURE (μV)(1) | | |
|---|---|---|---|
| | $C_o$ = 10 μF | $C_o$ = 47 μF | $C_o$ = 100 μF |
| 1 | tbf | 150 | tbf |
| 2 | tbf | 150 | tbf |
| 3 | tbf | 200 | tbf |

**Note**

1. Measured at a bandwidth of 200 kHz.

The noise on the supply line depends on the value of the supply capacitor and is caused by a current noise (output noise of the regulators is translated to a current noise by means of the output capacitors). The noise is minimum when a high frequency capacitor of 220 nF in parallel with an electrolytic capacitor of 100 μF is connected directly to pins 3 and 8 (supply and ground).

STABILITY

The regulators are stabilized with the externally connected output capacitors. The value of the output capacitors can be selected by referring to the graph illustrated in Fig.7.

When an electrolytic capacitor is used, its temperature behaviour can cause oscillations at temperatures lower than –20 °C. In this case, use a tantalum capacitor.

The two examples on the next page show how an output capacitor value is selected.

*Example 1*

Regulators 1, 2 and 3 are stabilized with an electrolytic output capacitor of 220 µF (ESR = 0.15 Ω). At –30 °C, the capacitor value is decreased to 73 µF and the ESR is increased to 1.1 Ω. The regulator will remain stable at –30 °C.

*Example 2*

Regulators 1, 2 and 3 are stabilized with an electrolytic output capacitor of 10 µF (ESR = 3.18 Ω). At –30 °C, the capacitor value is decreased to 3.3 µF and the ESR is increased to 23 Ω. The regulator will be instable at –30 °C.

*Solution*

Use a 47 nF HF capacitor in parallel with the output electrolytic output capacitor. As can be seen from the graph in Fig.7, the regulators will remain stable with an output capacitor of 47 nF onwards. The electrolytic output capacitor is only needed to minimize the output noise.

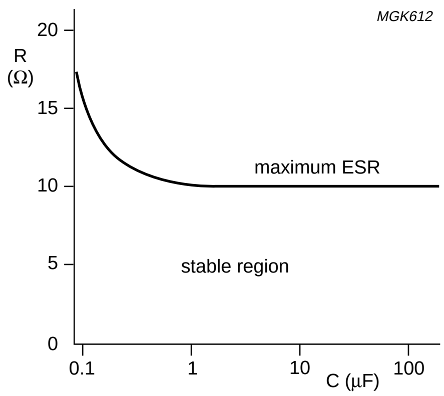
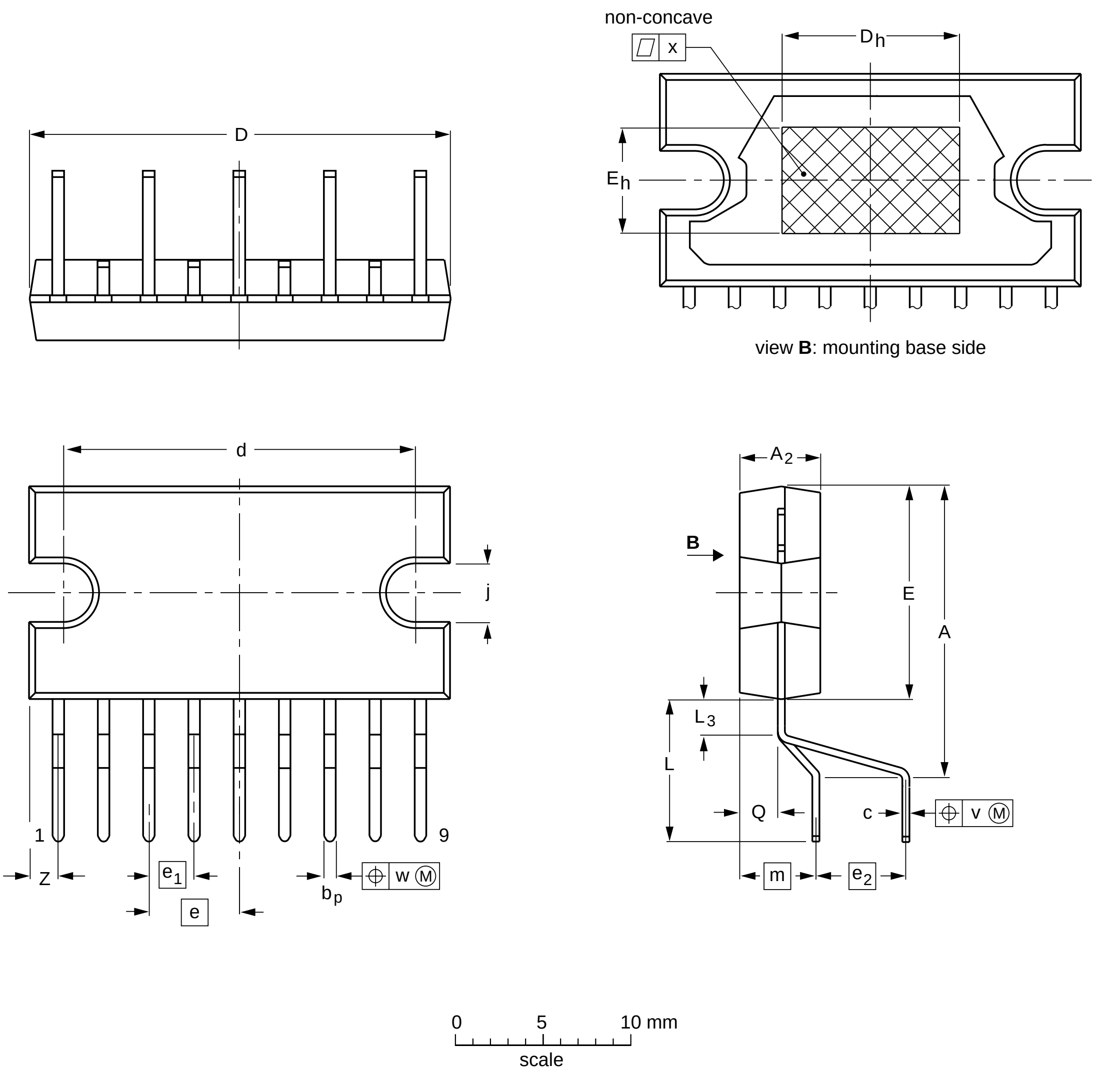



Fig.7 Curve for selecting the value of output capacitor for regulator 1.

## PACKAGE OUTLINE

**DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 7.7 mm)** **SOT157-4**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_2$ | $b_p$ | c | D(1) | d | $D_h$ | E(1) | e | $e_1$ | $e_2$ | $E_h$ | j | L | $L_3$ | m | Q | v | w | x | Z(1) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 17.0<br>15.5 | 4.6<br>4.2 | 0.75<br>0.60 | 0.48<br>0.38 | 24.0<br>23.6 | 20.0<br>19.6 | 10 | 12.2<br>11.8 | 5.08 | 2.54 | 5.08 | 6 | 3.4<br>3.1 | 8.4<br>7.0 | 2.4<br>1.6 | 4.3 | 2.1<br>1.8 | 0.6 | 0.25 | 0.03 | 2.00<br>1.45 |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT157-4 | | | | | | ~~95-03-11~~<br>97-12-16 |

## SOLDERING

### Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *“Data Handbook IC26; Integrated Circuit Packages”* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

### Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

### Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

### Suitability of through-hole mount IC packages for dipping and wave soldering methods

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | DIPPING | WAVE |
| DBS, DIP, HDIP, SDIP, SIL | suitable | suitable(1) |

**Note**

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

## DEFINITIONS

| Data sheet status | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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**NOTES**

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# Philips Semiconductors – a worldwide company

**Argentina:** see South America
**Australia:** 3 Figtree Drive, HOMEBUSH, NSW 2140, Tel. +61 2 9704 8141, Fax. +61 2 9704 8139
**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210
**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773
**Belgium:** see The Netherlands
**Brazil:** see South America
**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 68 9211, Fax. +359 2 68 9102
**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 800 943 0087
**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700
**Colombia:** see South America
**Czech Republic:** see Austria
**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905
**Finland:** Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615 800, Fax. +358 9 6158 0920
**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 4099 6161, Fax. +33 1 4099 6427
**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300
**Hungary:** see Austria
**India:** Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966
**Indonesia:** PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080
**Ireland:** Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200
**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007
**Italy:** PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI), Tel. +39 039 203 6838, Fax +39 039 203 6800
**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057
**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415
**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880
**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087
**Middle East:** see Italy
**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399
**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811
**Norway:** Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341
**Pakistan:** see Singapore
**Philippines:** Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474
**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327
**Portugal:** see Spain
**Romania:** see Italy
**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919
**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500
**Slovakia:** see Austria
**Slovenia:** see Italy
**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 58088 Newville 2114, Tel. +27 11 471 5401, Fax. +27 11 471 5398
**South America:** Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382
**Spain:** Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107
**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745
**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263
**Taiwan:** Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874
**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793
**Turkey:** Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye, ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813
**Ukraine**: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461
**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421
**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 800 943 0087
**Uruguay:** see South America
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