

DEVELOPMENT DATA

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TDA3740

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VIDEO PROCESSOR AND FREQUENCY MODULATOR FOR VIDEO RECORDERS

GENERAL DESCRIPTION

The TDA3740 is a monolithic integrated circuit for video signal processing and frequency modulation in video recorders.

Features

- Video controlled amplifier with clamping stage
- Fast and slow white amplitude detector
- Sync amplitude detector
- Black and white clip
- Insertion of sync and composite video signals
- Adder stage for composite video and chrominance signals
- Two-stage amplification for the composite video signal with dynamic (adjustable) and linear pre-emphasis
- White clip with external determination of clipping level
- Voltage controlled oscillator (frequency modulator)
- Blanking stage for the voltage controlled oscillator and limiter amplifier
- Reference voltage source

QUICK REFERENCE DATA

Supply voltage (pin 18, 28)	$V_P = V_{18, 28-27}$	typ.	10 V
Supply current (pin 18, 28) (record mode)	$I_P = I_{18, 28}$	typ.	58 mA
Supply current (pin 18) (playback mode)	$I_P = I_{18}$	typ.	28 mA
Composite video input signal (peak-to-peak value)	$V_{3-27(p-p)}$	typ.	350 mV
Composite colour video output signal (peak-to-peak value)	$V_{7-27(p-p)}$	typ.	2 V
Chrominance input signal (peak-to-peak value)	$V_{9-27(p-p)}$	typ.	240 mV
Output current (pin 22, 23)	$I_{22, 23}$	typ.	8,5 mA

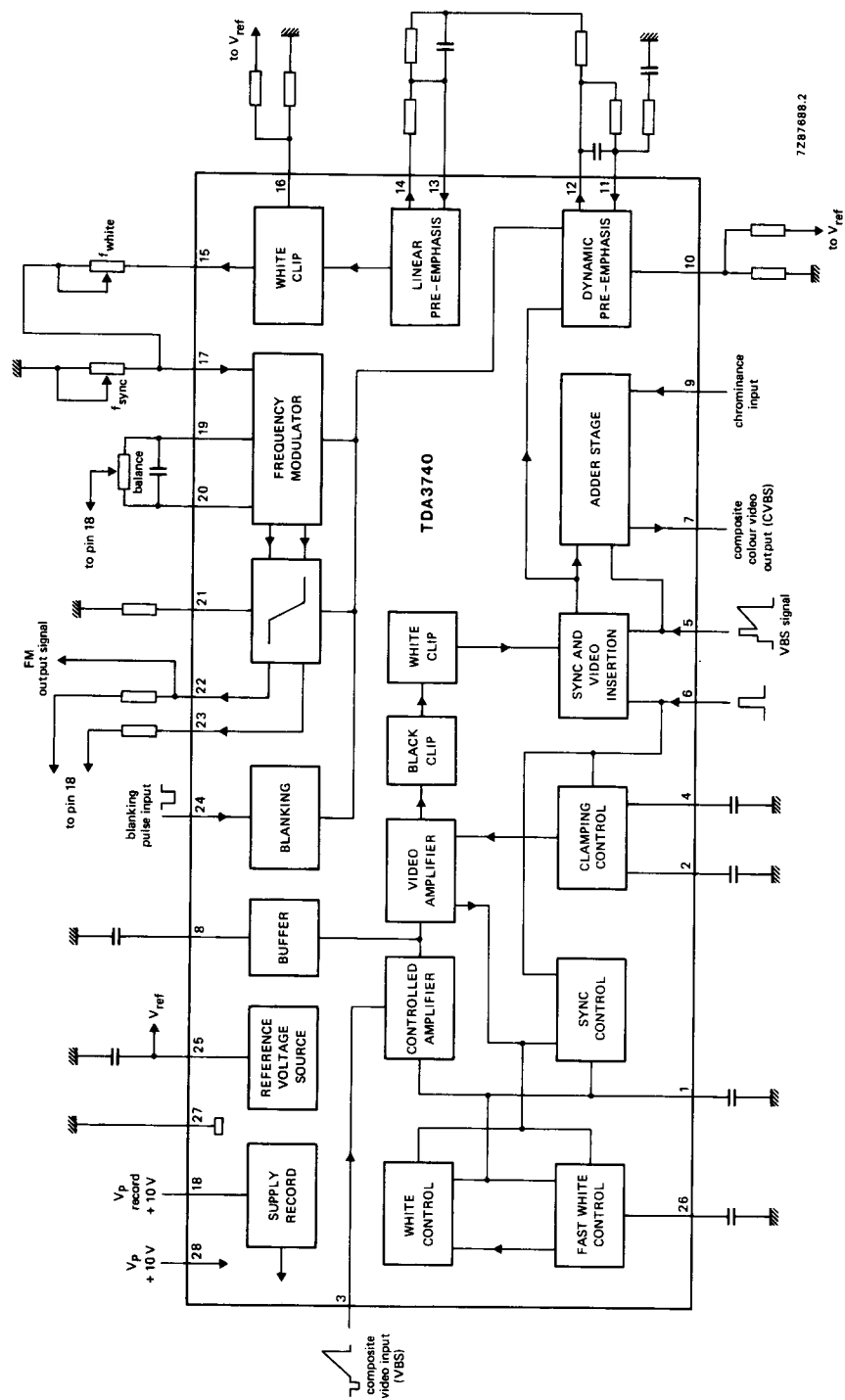


Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18, 28) $V_P = V_{18, 28-27}$ max. 13,2 VWith pin 27 connected to ground and pin 18 and 28 to supply voltage (V_P) all voltages between 0 and V_P are allowed.Total power dissipation P_{tot} max. 1,4 WStorage temperature range T_{stg} -25 to +150 °COperating ambient temperature range T_{amb} 0 to +70 °C**CHARACTERISTICS** $V_P = V_{18-28} = 10$ V; $T_{amb} = 25$ °C; measured in test circuit Fig. 2; unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pin 18, 28)					
Supply voltage	$V_P = V_{18, 28-27}$	9	10	13,2	V
Supply current					
at record (FM kill inactive)	$I_P = I_{18, 28}$	—	58	—	mA
at playback	$I_P = I_{28}$	—	28	—	mA
Controlled amplifier					
Composite video input signal (peak-to-peak value)	$V_{3-27(p-p)}$	0,20	0,35	0,62	V
Video signal control range (referred to 0,35 V input signal at pin 3)	α_{3-27}	±5	±6	—	dB
Input resistance	R_{3-27}	7	10	13	kΩ
Input capacitance	C_{3-27}	—	—	10	pF
Composite colour video output signal (peak-to-peak value)	$V_{7-27(p-p)}$	1,9	2	2,1	V
Frequency response (0 to 3 MHz)	α_{7-3}	-0,5	—	0,5	dB
Sync recovering and insertion of composite video signal					
Threshold voltage for sync recovering	V_{6-27}	3,0	3,5	4,0	V
Input resistance	R_{6-27}	100	—	—	kΩ

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parameter	symbol	min.	typ.	max.	unit
Insertion of composite video signal					
insertion inactive	V5-27	0	—	0,9	V
video + chroma mute	V5-27	2,5	—	3,0	V
insertion black level	V5-27	3,1	3,25	3,4	V
insertion white level (90% CVBS)	V5-27	3,7	4,0	4,3	V
Input resistance	V5-27	100	—	—	k Ω
Gain	G7-5	2,9	4,5	6,5	dB
Frequency response (0 to 5 MHz)	α 7-5	—	—	3	dB
Signal suppression pin 7 at mute		—40	—	—	dB
Clamping control					
Duration of clamping pulse (note 1) with C2-27 = 100 nF; C4-27 = 2,2 nF	t _d	1	3	4,5	μ s
Max. leakage current of external capacitor	I _{L2}	—	—	1	μ A
Black and white clip					
Black clip relative to black level	Δ V7-27	—40	—25	0	mV
White clip at pin 7 (referred to nominal VBS)		103	105	107	%
Chrominance signal adder and output stage					
Burst input signal (peak-to-peak value)	V9-27(p-p)	—	240	400	mV
Input resistance	R9-27	4	5,6	—	k Ω
D.C. level of top sync	V7-27	2,4	2,7	3,0	V
Sync amplitude at CVBS output pin 7	V7-27(p-p)	570	600	630	mV
Gain (f = 4,43 MHz)	G7-9	7	8	9	dB
Output resistance	R7-27	—	—	30	Ω
Frequency response (0 to 5 MHz)	α 7-9	—0,5	—	+0,5	dB
Dynamic and linear pre-emphasis; white limiter					
Input resistance pin 11	R11-27	15	—	—	k Ω
Output resistance (emitter follower with internal current source)	R12-27	—	—	30	Ω
Gain-bandwidth product dynamic (V24—27 = V _p)		24	36	—	MHz
linear		30	—	—	MHz

parameter	symbol	min.	typ.	max.	unit
Range of dynamic pre-emphasis (fixed by external resistors at pin 10)	V10-27	0	—	2,5	V
Gain adjustment range at 1 MHz and V7-27 = 632 mV	G12-7	1,5	—	8	dB
Output resistance (emitter follower with internal current source)	R14-27	—	—	30	Ω
White clip level deviation relative to V16-27 = 1,5 V	V16-15	75	—	125	mV
Range of clipping determination (note 2)	V16-27	1	—	3	V
Frequency modulator					
D.C. level at pin 21 (note 3)	V21-27	1,8	1,9	2,0	V
FM output voltage (note 3) R21-27 = 1,5 k Ω , R22, 23-18 = 470 Ω	V22, 23-27	—	660	—	mV
Slope between 3 MHz and 6 MHz	$\frac{\Delta f_{22,23}}{\Delta I_{17}}$	—	10,5	—	$\frac{\text{KHz}}{\mu\text{A}}$
	m	95	—	—	%
Linearity between 3 MHz and 6 MHz					
Suppression of the 2nd harmonic referred to the 1st harmonic 3,8 MHz (balanced)	α_{harm}	40	46	—	dB
Frequency drift dependent on: drift of supply voltage (Vp = 9 – 13,2 V)	$\frac{\Delta f_{22,23}}{\Delta V_p}$	—	5	10	$\frac{\text{KHz}}{\text{V}}$
drift of ambient temperature (Tamb = 0 – 70 °C) at 3,8 MHz	$\Delta f_{22,23}$	–85	—	+85	KHz
at 4,8 MHz	$\Delta f_{22,23}$	–85	—	+85	KHz
Drift of frequency span dependent on temperature drift (Tamb = 0 – 70 °C)	Δf	–70	—	+70	KHz
Input voltage to switch FM off	V24-27	—	—	2	V
Input voltage to switch FM on	V24-27	3	—	—	V
Input resistance	R24-27	10	—	—	k Ω

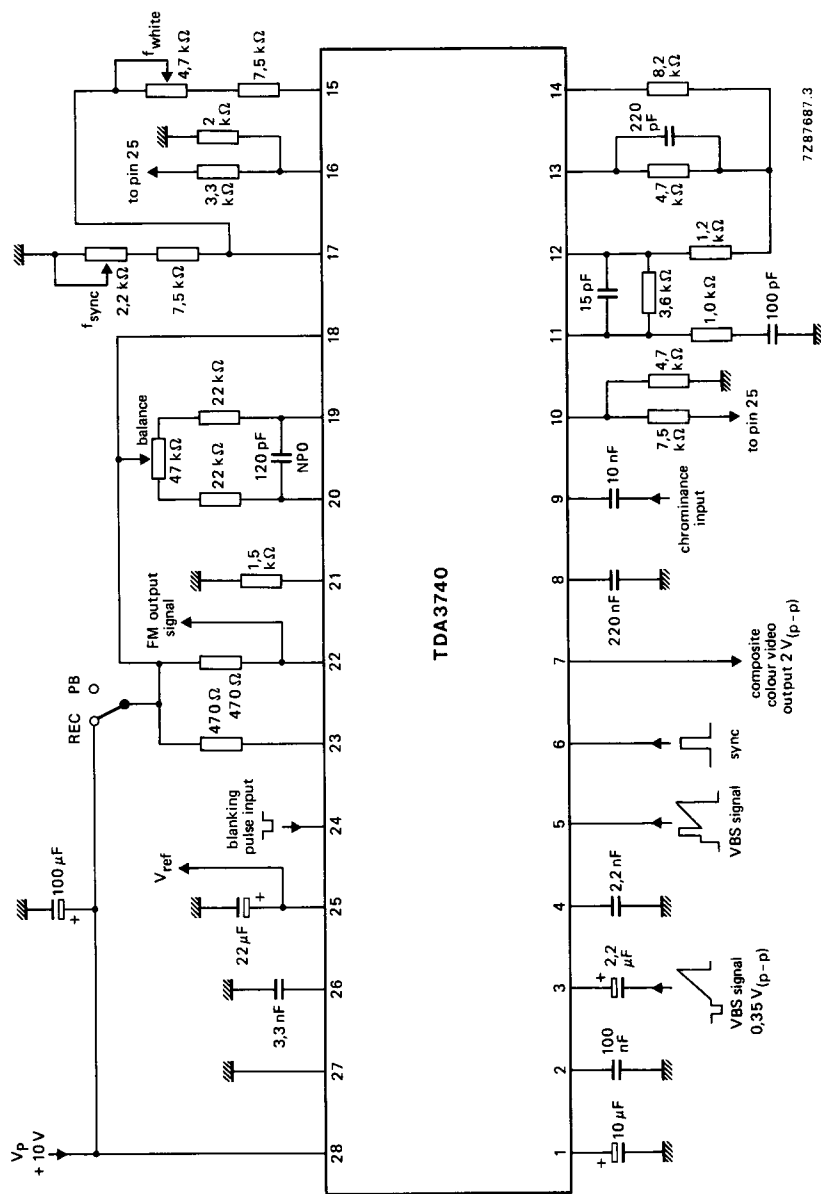
parameter	symbol	min.	typ.	max.	unit
Reference voltage source (pin 25)					
Output voltage	V_{25-27}	—	5,5	—	V
Output current (additional to application)	I_{25}	—3	—	+5	mA
Output voltage drift dependent on drift of supply voltage ($V_P = 9 - 13,2$ V)	$\frac{\Delta V_{25-27}}{\Delta V_P}$	—10	—	+10	$\frac{mV}{V}$
drift of ambient temperature ($T_{amb} = 0 - 70$ °C)	ΔV_{25-27}	—90	—	+90	mV

Notes

1. Duration of clamping pulse is determined by C4-27 as follows: $t_d (\mu s) = 1,364 \cdot C_{4-27} (nF)$.
2. White clipping level is fixed by the external resistors at pin 16, e.g. $R_{16-25} = 3,3$ k Ω and $R_{16-27} = 2$ k Ω results in 160% clipping level.
3. FM output amplitude at pins 22 and 23 is determined by the external fixed resistors R_{21-27} , R_{22-18} and R_{23-18} .

DEVELOPMENT DATA

APPLICATION INFORMATION



REC = record.
PB = playback.

Fig. 2 Application diagram; also used as test circuit.