DATA SHEET

TDA5345HT
5 V spindle & VCM driver combo

Preliminary specification

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Philips Semiconductors

PHILIPS

FEATURES

- Single chip voice coil and spindle motor drivers:
- Complementary outputs (Nmos & Pmos): No step-up converter needed
- On-chip isolation switch to allow synchronous rectification at power-down
- Suited for ramp load operation
- Register based architecture: on-chip serial interface
- Temperature shut down protection
- Linear 3.3 V regulator using one external NPN transistor
- Power monitor circuitrymonitoring the 5 V supply
- 1 axis shock sensor amplifier
- Switched capacitor regulator (-3 V) using 2 external capacitors and 2 external shottky diodes
- All main internal functions can be independently put in Sleep mode
- Small low profile package: TQFP64 (1.2 mm high).

Spindle motor driver:

- High efficiency drivers: 1.5 Ω Max
- 0.62 Amp capability, full wave (bipolar) drive
- Internal current mirrors to measure the motor curren
- Controlled fly-back pulse slopes, programmable through the serial interface
- Active fly-back pulse limitation, using the Power MOS instead of diodes
- Internal digital timing to control the commutations by back-EMF sensing (Start-up & running)
- Internal speed loop combining FLL and PLL
- Start-up current control by an internal 6-bit DAC (shared with the VCM loop).

Voice coil motor (VCM) driver:

- High efficiency drivers: 1.5 Ω Max (without the external sense resistor); 0.4 Amp capability
- External sense resistor to accurately control the VCM current
- True AB Class linear amplifier with no crossover distortion
- Internal 12-bit DAC to control the VCM transconductance input voltage
- Internal 6-bit DAC to cancel the VCM loop offsets
- Active fly-back pulse limitation, using the Power transistors instead of diodes
- 3-step programmable retract function activated by either the serial port or the power monitor circuitry
- Back-EMF amplifier to monitor the actuator speed when ramp loading.

Power Monitor:

- Monitors the 5 V power supply
- Power fault output (battery too low); threshold = 4.2 V
- Power on Reset output; threshold = 4.1 V (Vdd5)
- Threshold accuracy: +/-3%.

GENERAL DESCRIPTION

The TDA5345HT is a combination of a voice coil motor and a spindle motor driver, designed for 5 V high performance portable small form factor hard disk drives. Communications with the micro-controller take place through a 16-bit 3-wire uni-directional serial port. Power dissipation is a major concern in portable drives, therefore each main function can be individually put in sleep mode when it is not used, to save as much power as possible. The serial port and the power monitor are the only functions which remain always active.

The TDA5345HT integrates a spindle driver and the commutation logic that drives a three-phase brushless, sensorless DC motor in full wave mode. Commutations are generated from the internal back-EMF sensing circuitry from start-up to the running mode. An internal speed loop combining FLL and PLL technics makes sure that the spindle reaches the right speed, programmed through the serial port. The 6-bit DAC is used to limit the Start-up current by limiting the voltage on the speed loop filter. To reduce acoustical noise and current noise on both power supply and ground, the fly-back pulse leading edge slew-rate is controlled. 4 different slope values are programmable.
To prevent internal parasitic effects, positive and negative fly-back pulses are clamped by the output power transistors themselves: lower NMOS transistors are turned ON to limit the negative fly-back pulses just below ground while upper PMOS limit the positive fly-backs just above the power supply. This active limitation is still active at power down during the VCM retract. In this way, an efficient back-EMF rectification is obtained (no diodes losses).

The VCM driver is a linear transconductance amplifier; it is a true AB class with a 8 mA quiescent current. It means that there is absolutely no crossover distortion. An external compensation network is used to set the loop bandwidth and ensure the loop stability. With common VCM characteristics, the bandwidth can go up to 40 kHz. To prevent internal parasitic effects, positive and negative fly-back pulses are clamped by the output power transistors themselves.
An on-chip 12-bit DAC is used to generate the VCM amplifier input voltage. This a signed converter, with an output range of [1.25 V ; 1.75 V] when the low gain is selected and an output range of [0.5 V ; 2.5 V] when the high gain is selected. The all VCM transconductance works then around a 1.5 V reference (available on one pin). It is possible to add an external notch filter between the 12-bit DAC output and the VCM loop intput. An other 6-bit DAC is used to cancel the Vcm loop offsets. An additional Vcm back-EMF amplifier is provided to monitor the actuator speed when ramp loading. A ramp unload circuitry is included as well. It can be activated through the serial bus (SoftRetract) or automatically initiated in case of temperature shut down or at power-down. The ramp unload sequence is made of 3 steps : brake, slow retract and then full power. The retract steps duration is set by means of internal programmable counters, clocked by the spindle back-EMF. In case of power down, this sequence is followed by a spindle brake. The three spindle lower power NMOS are switched fully ON together.

The linear 3.3 V DC-DC converter is designed to drive an external power NPN that will supply the 3.3 V chips. It can be enabled or disabled by hardware, using the external Reg3v3On pin.

The switched capacitor -3 V regulator is designed to supply a very clean negative voltage to the PreAmp IC in the drive.

The shock sensor amplifier is intended to be connected to an external 1 axis shock sensor. The window comparator threshold is programmable through the serial bus.

An internal circuitry provides either an analog or a digital information about the junction temperature. These two informations can be selected through the serial bus. When the analog output is selected, the voltage is proportional to the internal chip temperature. When the digital output is selected, it indicates that the temperature exceeds 145 °C. An internal thermal shut down mode is initiated when the temperature is higher than 160 °C: the 3 spindle outputs are disabled while the vcm is immediately retracted.

The power monitor circuitry monitors the 5V power supply. The Power On Reset PORN output is driven low when the 5 V supply is below 4.1 V. This threshold can be changed by an external resistor divider. Once the power supplies is above its threshold, the Power On Reset output goes high after a delay that is set by an external capacitor. A second output, called Power Fault (active HIGH), indicates that the 5 V power supply is below 4.2 V when high. There is no delay between the supply crossing the threshold and the PowerFault output change.

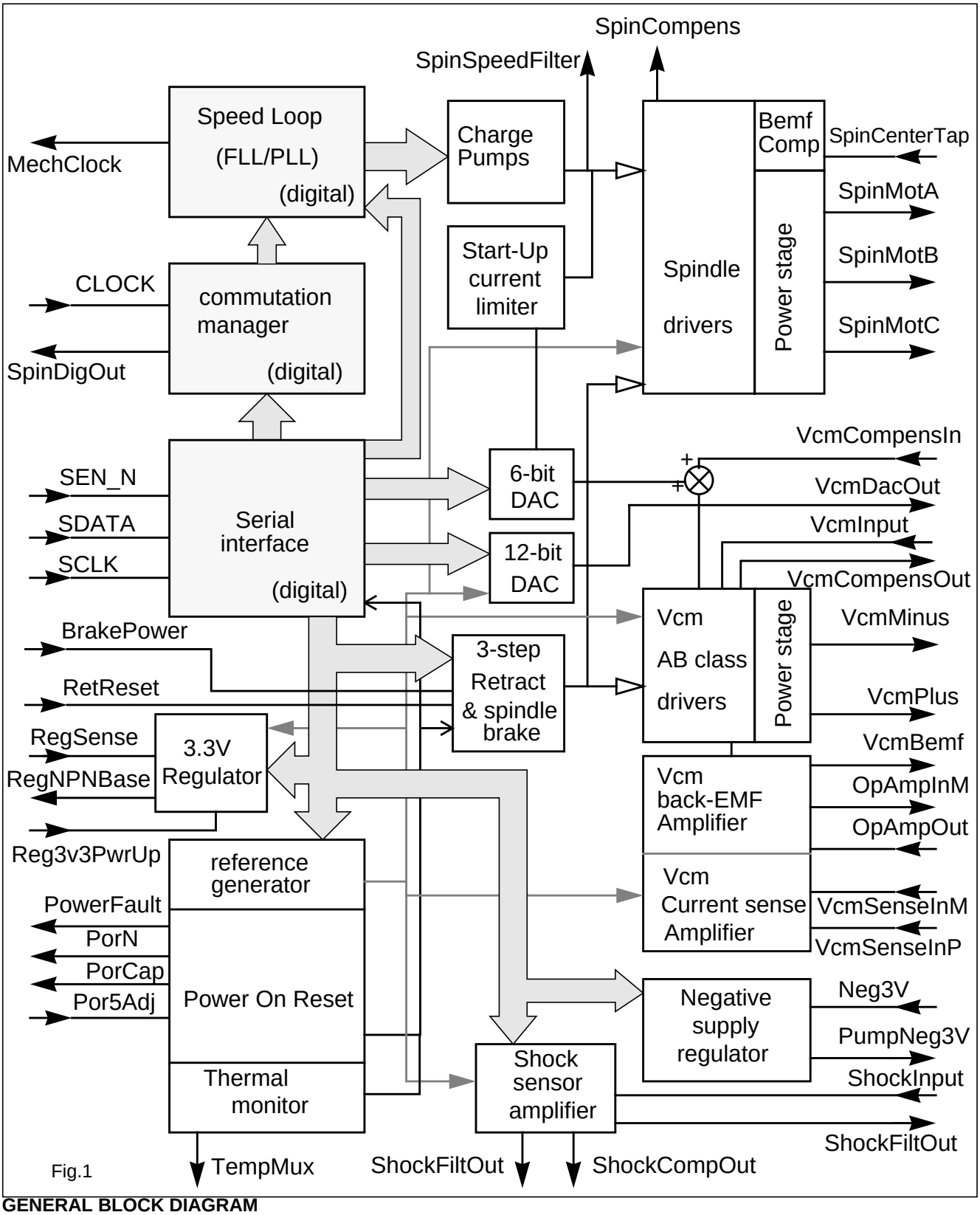

Fig.1

GENERAL BLOCK DIAGRAM

PINNING (GREY ROWS MEANS NEW PINS))

SYMBOL	PIN #	DESCRIPTION	I/O
SpinVddA	1	spindle MotA half bridge power supply	I
SpinRectBemf	2	spindle “Clamp”: rectified Bemf	O
SpinMotA	3	spindle power output: A	O
VcmVddM	4	VCM- half bridge power supply	SUPPLY
SpinGndAB	5	spindle MotA & MotB half bridges ground	GROUND
VcmMinus	6	VCM inverted power output (VCM-)	O
n.c.1	7	not connected ; connect it to ground	GROUND
SpinMotB	8	spindle power output: B	O
VcmGndPow	9	VCM H-bridge ground	GROUND
SpinVddBC	10	spindle MotC & MotB half bridges power supply	I
VcmPlus	11	VCM non-inverted power output	O
n.c.2	12	not connected; connect it to ground	GROUND
SpinMotC	13	spindle power output: C	O
VcmVddP	14	VCM+ half bridge power supply	SUPPLY
SpinGndC	15	spindle MotC half bridge ground	GROUND
GNDAna1	16	analog ground	GROUND
VcmCompensOut	17	VCM error amplifier output	O
VcmRef	18	VCM loop reference voltage (1.5 V)	O
VcmCompensIn	19	VCM error amplifier inverted input	I
VcmInput	20	VCM loop input	I
VcmVdd5Div2	21	internal Vdd5/2 reference voltage for the VCM	I/O
VcmSenseInM	22	VCM sense amplifier inverted input	I
VcmSenseInP	23	VCM sense amplifier non-inverted input	I
Vdd5Ana1	24	analog power supply	SUPPLY
PorN	25	power On Reset output	O
PorCap	26	external capacitor used to set the Power On Reset delay	O
BdGap	27	internal band-gap reference voltage (for production trimming)	I
Por5Adj	28	5 V power on reset threshold adjustment	I
VcmBemf	29	VCM Back-Emf amplifier output	O
OpAmpInM	30	VCM Back Emf Operational Amplifier inverted input	I
OpAmpOut	31	VCM Back Emf Operational Amplifier output	O
GNDAna2	32	analog ground	GROUND
RefCurRes	33	external 33 kΩ resistor	O
Reg3v3PwrUp	34	hardware enable / disable for the 3.3 V regulator (at Power Up)	I
PumpNeg3 V	35	-3 V regulator pump capacitor	O
Neg3 V	36	-3 V regulator output sense pin	I
PowerFault	37	battery low warning	O
CLOCK	38	digital timing clock	I
SDATA	39	serial port Data line	I
Vdd5Dig	40	digital power supply	SUPPLY

SYMBOL	PIN #	DESCRIPTION	I/O
SCLK	41	serial port Clock	I
SEN_N	42	serial port ENABLE line: active low	I
SpinMechClock	43	spindle rotation speed (1 pulse / revolution)	O
SpinDigOut	44	spindle back-EMF comparator output or commutation clock	O
RetReset	45	external capacitor used to reset the retract sequence state machine	I
RegNPNBase	46	3v3 DC-DC converter output (drives an external NPN)	O
RegSense	47	3v3 DC-DC converter input	I
GndDig	48	digital ground	GROUND
VcmDacOut	49	12-bit VCM DAC output	O
ShockRef	50	shock sensor reference voltage	O
ShockFiltOut	51	shock sensor RC low pass filter output	O
ShockCompOut	52	shock sensor comparator output	O
ShockCom	53	shock sensor input common mode	I
ShockAmpOut	54	shock sensor amplifier output	O
ShockInput	55	shock sensor input	I
Vdd5Ana2	56	analog power supply	SUPPLY
TempMux	57	internal thermal monitor circuitry voltage output	O
SpinSpeedFilter	58	external FLL/PLL speed loop filter	O
SpinCompens	59	spindle current loop compensation capacitor	O
BrakePower	60	external capacitor to supply the spindle brake at power down	I
SpinCenterTap	61	spindle centre tap connection	I
RetPmosDrain	62	retract Pmos transistor drain connection	O
IsoSwSo	63	spindle power outputs supply	SUPPLY
GNDAna3	64	analog ground	GROUND

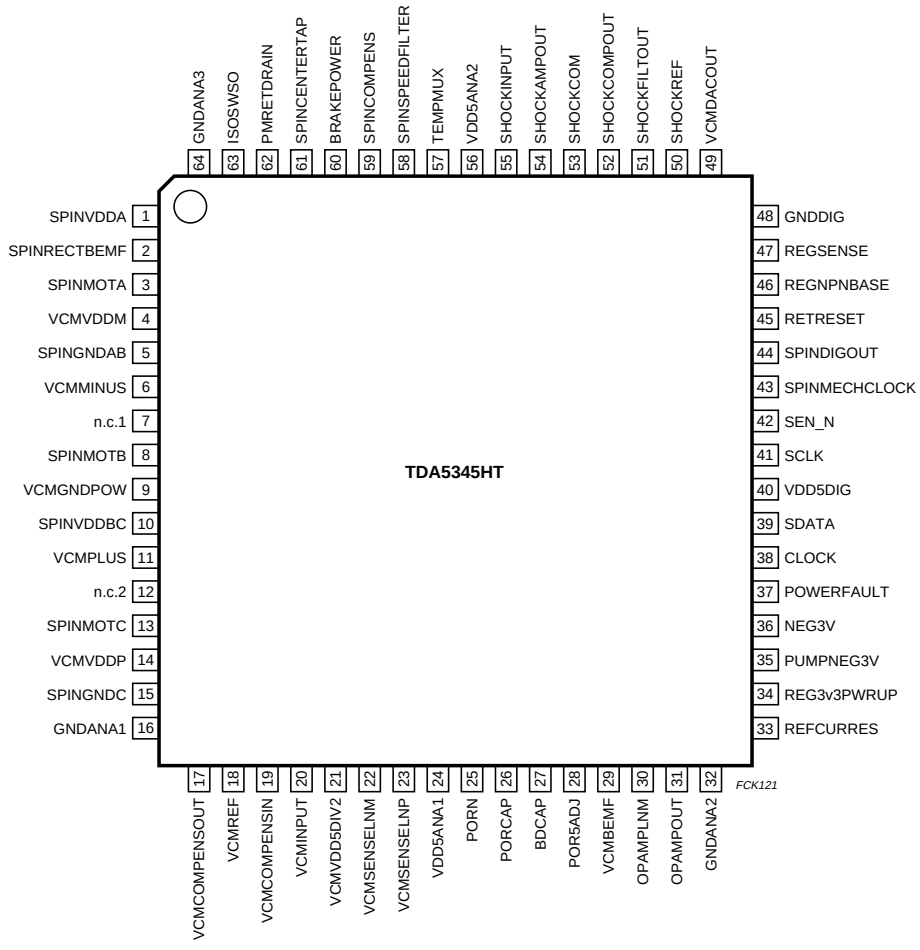

Fig.3 Pin configuration

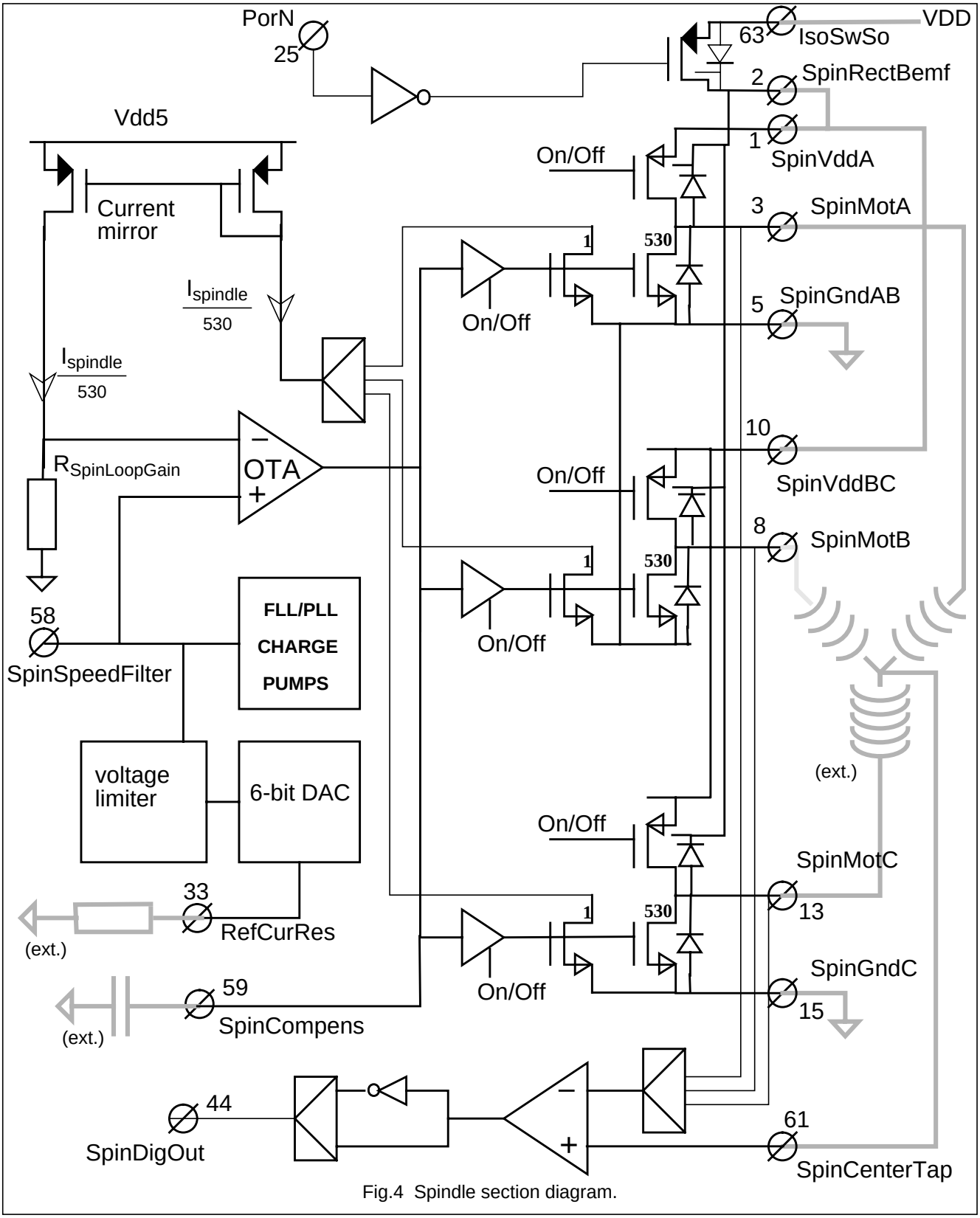

Fig.4 Spindle section diagram.

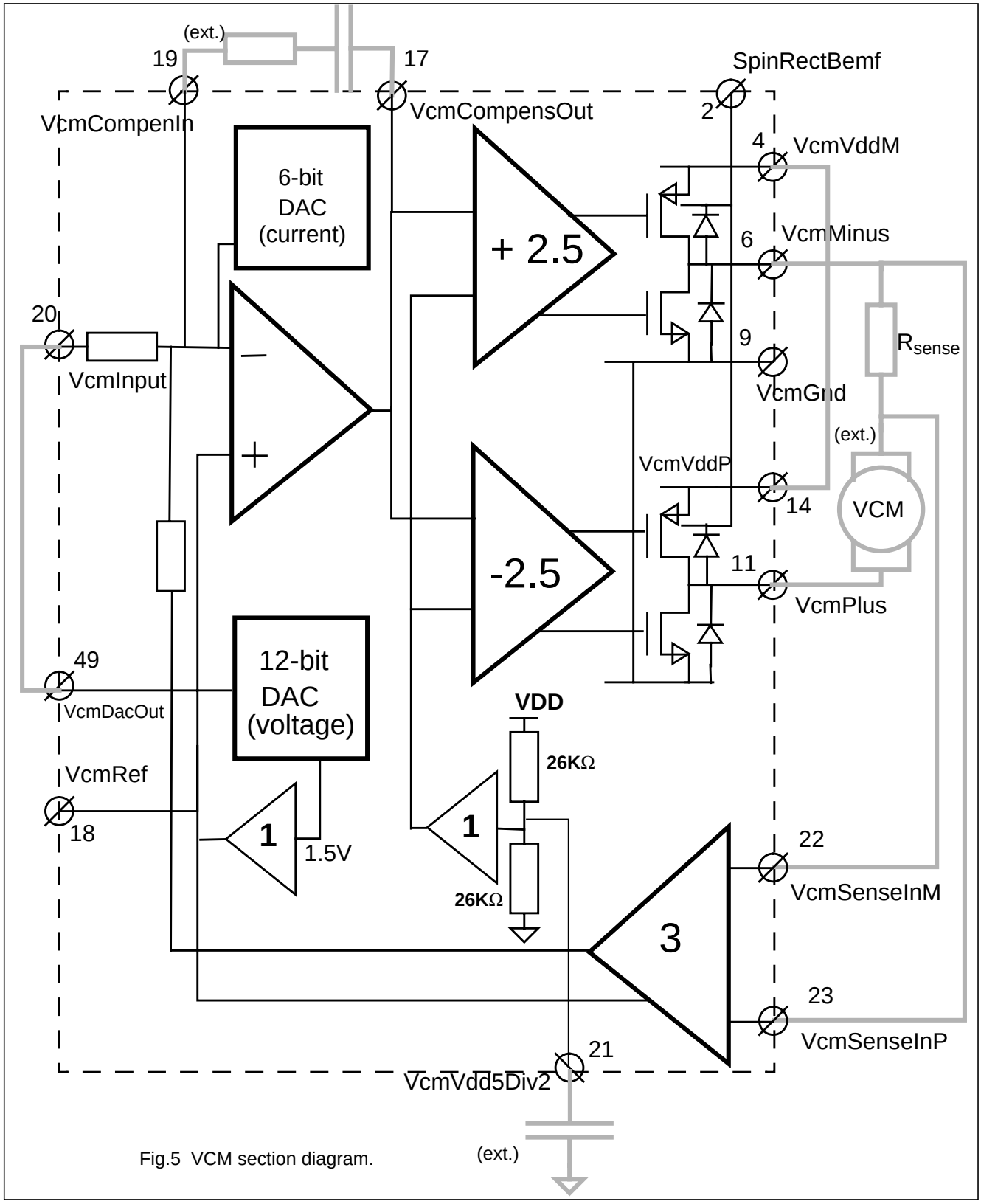

Fig.5 VCM section diagram.

FUNCTIONAL DESCRIPTION

Serial interface

The serial interface is a uni-directional port for writing data to the internal registers of TDA5345HT. Each write is composed of 16 bits. For data transfer SEN_N is brought low, serial data is presented at SDATA pin, and a serial clock is applied to the SCLK pin. After the SEN_N pin goes low, the first 16 pulses applied to the SCLK pin shifts the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SEN_N goes high. If less than 16 clock pulses are provided before SEN_N goes high, the data transfer is aborted.

All transfers are shifted into the serial port MSB first. The first 4 bits of the transfer determine the internal register to be accessed. The other 12 bits contain the programming data. During sleep modes, the serial port remains active and register programming data is retained.

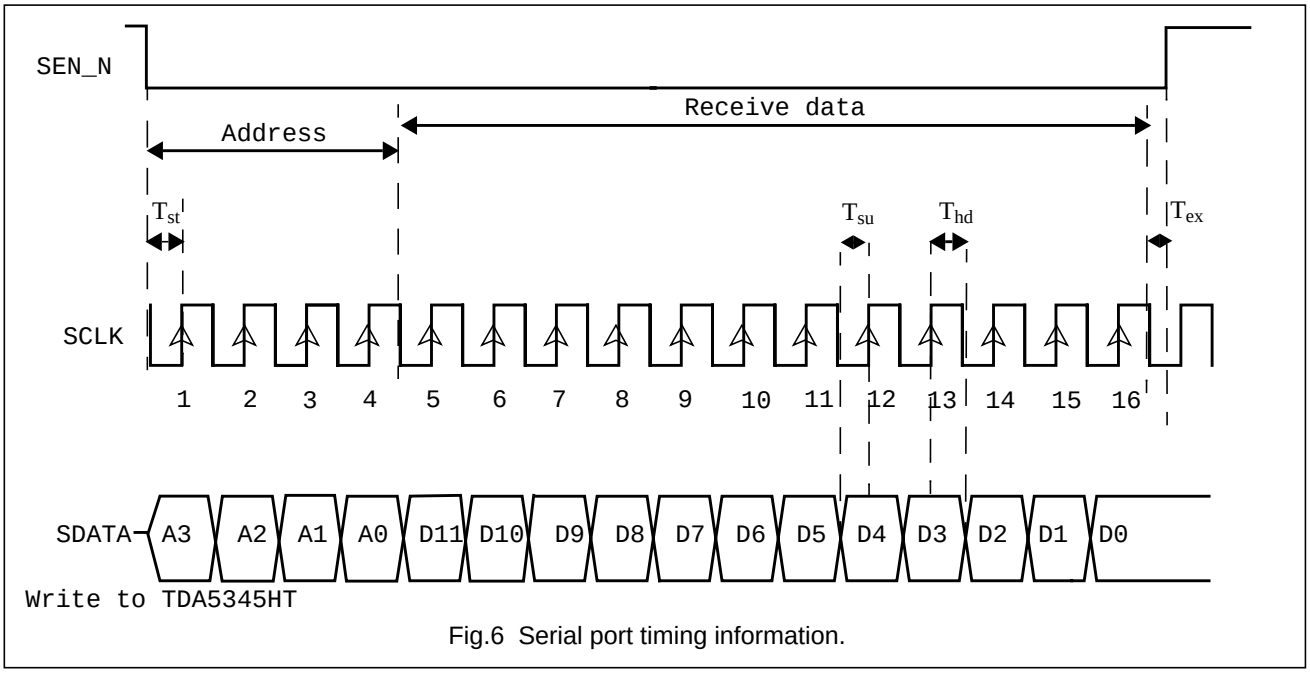

Fig.6 Serial port timing information.

Table 1 Address of registers

A3	A2	A1	A0	REG.	DESCRIPTION
0	0	0	0	0	clock dividers programmation, spindle mode control
0	0	0	1	1	start-up,comdelim & watch-dog delays
0	0	1	0	2	blank delay, bandgap adjust, 3-step retract param (begin)
0	0	1	1	3	3-step retract parameters (end)
0	1	0	0	4	fly-back slope, shock sensor threshold & sleep control bits
0	1	0	1	5	speed factor (MSBs), PLL control and 6-bit DAC
0	1	1	0	6	speed factor(LSBs)
0	1	1	1	7	Vcm 12-bit DAC (low gain)
1	0	0	0	8	Vcm 12-bit DAC (high gain)
1	0	0	1	9	shock sensor threshold

Table 2 Serial Interface REGISTERS floorplan

BIT\ REG	11	10	9	8	7	6	5	4	3	2	1	0
0	RegNeg Clk2 **[0]**	RegNeg Clk1 **[1]**	RegNeg Clk0 **[0]**	Presc Factor1 **[0]**	Presc Factor0 **[0]**	BiasCT **[0]**	Run/ Stop **[0]**	Pll Enable **[0]**	Manual **[0]**	Man Com2	Man Com1	Man Com0
1	StartUp Delay3	StartUp Delay2	StartUp Delay1	StartUp Delay0	ComDe Lim3	ComDe Lim2	ComDe Lim1	ComDe Lim0	Watch Dog3	Watch Dog2	Watch Dog1	Watch Dog0
2	Blank Delay3	Blank Delay2	Blank Delay1	Blank Delay0	DigOut Mux **[1]**	BdGap Adj2 **[0]**	BdGap Adj1 **[0]**	BdGAp Adj0 **[0]**	VcmRet SoftRis	Vretract 2	Vretract 1	Vretract 0
3	T_Full Power2	T_Full Power1	T_Full Power0	T_Slow Ret5	T_Slow Ret4	T_Slow Ret3	T_Slow Ret2	T_Slow Ret1	T_Slow Ret0	T_Vcm Brake2	T_Vcm Brake1	T_Vcm Brake0
4	FlyBack Slope1	FlyBack Slope0	Shock Thresh1	Shock Thresh0	Vcm Retract **[0]**	Vcm Sleep **[1]**	Dac12 Sleep **[1]**	RegNeg Sleep **[1]**	Shock Sleep **[1]**	Spin Sleep **[1]**	Reg3v3 Enable **[0]**	Temp Select **[0]**
5	Speed bit14	Speed bit13	Speed bit12	PllCur 1	PllCur 0	Dac6 ToVCM **[0]**	Dac6 bit5	Dac6 bit4	Dac6 bit3	Dac6 bit2	Dac6 bit1	Dac6 bit0
6	Speed bit11	Speed bit10	Speed bit9	Speed bit8	Speed bit7	Speed bit6	Speed bit5	Speed bit4	Speed bit3	Speed bit2	Speed bit1	Speed bit0
7	Dac12a bit11	Dac12a bit10	Dac12a bit9	Dac12a bit8	Dac12a bit7	Dac12a bit6	Dac12a bit5	Dac12a bit4	Dac12a bit3	Dac12a bit	Dac12a bit1	Dac12a bit0
8	Dac12b bit11	Dac12b bit10	Dac12b bit9	Dac12b bit8	Dac12b bit7	Dac12b bit6	Dac12b bit5	Dac12b bit4	Dac12b bit3	Dac12b bit2	Dac12b bit1	Dac12b bit0
9		Shock Thresh2 **[0]**										

Note:

1. **[1]** (or **[0]**) means that the bit is set to 1 (or 0) when PorN is low => default value at power up.
2. Use register 7 (Dac12a) for low VCM loop gain and register 8 (Dac12b) for high gain.

Control bits:

REGISTER #0:

Bits [11, 9] (RegNegClk[2, 0]): The Negative supply (-3V) regulator needs a 500 kHz clock. A programmable divider genreates this frequency from the external clock ([15-33] Mhz). Programmation is on 3 bits.

Bits [8, 7] (PrescFactor[1, 0]): used to select the prescaler division factor (see next section: “commutation control”).

Bit 6 (BiasCT): used to bias the spindle centre tap at Vdd5/2 when the spindle outputs are disabled (Run/Stop = 0). The back-EMF comparator remains operational when BiasCT = 1, to check if the spindle is running for instance.

Bit 5 (Run/Stop): after the power supply is turned on and PorN is high, the motor will start spinning when Run/Stop is set to ‘1’. The spindle power output starts from state code 0 (see table 3). The motor will stop when this bit is set to ‘0’. The 3 spindle power outputs are then switched off. No brake is applied.

bit 4 (PllEnable): enables the PLL to improve the speed accuracy.

Bit 3 (Manual): selects the manual commutation mode (Run/Stop bit also needs to be high). When getting out of the manual mode (=> Manual = ‘0’) and keeping the Run/Stop bit high, the internal commutation block will start from the last state programmed in manual mode.

Bits [2, 0] (ManCom[2, 0]): control the commutation in manual mode when Run/Stop = 1 & Manual = 1.

Table 3 Spindle power output states according to ManCom0, ManCom1, ManCom2 bit values.

MANCOM[2]	MANCOM[1]	MANCOM[0]	SPINMOT A	SPINMOT B	SPINMOT C	STATE CODE
0	0	0	low	high	float	0
0	0	1	low	float	high	1
0	1	1	float	low	high	2
1	1	1	high	low	float	3
1	1	0	high	float	low	4
1	0	0	float	high	low	5
1	0	1	low	low	low	6 (brake)
0	1	0	high	low	high	7 (tripolar)

REGISTER #1

bit [11, 8] (StartUp[3, 0]): programmable delay used to detect if the spindle is standing still at start-up.

bit [7, 4] (ComDeLim[3, 0]): Used to set a default value for the spindle commutation delay.

bit [3, 0] (WatchDog[3; 0]): programmable delay used to detect if the spindle is running backward at star-up.

REGISTER #2

bit [11, 8] (BlankDelay[3, 0]): programmable delay used to blank the first edge of the spindle inductive fly-backs.

bit 7 (DigOutMux): SpinDigOut pin is the commutation clock when DigOutMux = ‘1’ else back-EMF comparator output.

bit [6, 4] (BdGapAdj[2, 0]): used to adjust the internal BandGap reference voltage to improve several parameters.

bit 3 (VcmRetSoftRising): Enables the digital soft rising slope on the “full power retract” step.

bit [2, 0] (Vretract[2; 0]): used to program the VcmMinus output voltage during the “soft retract” step.

REGISTER #3

bit [11, 9] (T_FullPower[2, 0]): used to program how much time the full power retract step is applied.

bit [8, 3] (T_SlowRetract[5, 0]): used to program how much time the slow retract step is applied.

bit [2, 0] (T_VcmBrake[2, 0]): used to program how much time the VCM brake step is applied.

REGISTER #4

bit [11, 10] (FlyBackSlope[1, 0]): used to program the fly-back pulse leading edge slew rate.

bit [9, 8] (ShockThresh[1, 0]): set the shock sensor threshold value.

bit 7 (VcmRetract): activates a VCM retract when VcmRetract = ‘1’.

bit 6 (VcmSleep): puts the VCM section (except the VCM sense amplifier and the VCM 12-bit DAC) in sleep mode when VcmSleep = ‘1’.

bit 5 (DAC12Sleep): puts the VCM 12-bit DAC & the VCM sense amplifier in sleep mode when Dac12Sleep = ‘1’.

bit 4 (RegNegSleep): puts the -3 V regulator in sleep mode when RegNegSleep = ‘1’.

bit 3 (ShockSleep): puts the Shock sensor section in sleep mode when ShockSleep = ‘1’.

bit 2 (SpinSleep): puts the Spindle section in sleep mode when SpinSleep = ‘1’ ; SpinMotA, B, C are floating then.

bit 1 (Reg3v3Enable): Enables the internal 3.3 V regulator when bit 1= ‘1’.

bit 0 (TempSelect): selects whether the TempMux pin is a digital output (temperature-high warning) when TempSelect = ‘0’ or an analog output (temperature monitor) when TempSelect = ‘1’.

REGISTER #5

bit [11, 9] (Speed[14, 12]): division factor used to set the spindle speed controlled by onboard FLL/PLL (2 MSBs only).

bit [8, 7] (PllCur[0, 1]): Programmable current for the PLL charge pump.

bit 6 (Dac6ToVcm): 6-bit DAC is connected to the VCM section when Dac6ToVcm = ‘1’, else connected to the spindle.

bit [5, 0] (Dac6[5, 0]): 6-bit word converted to a current by the 6-bit DAC.

REGISTER #6

bit [11, 0] (Speed[11, 0]): division factor used to set the spindle speed controlled by onboard FLL/PLL (12 LSBs only).

REGISTER #7

bit [11, 0] (Dac12a[11, 0]): 12-bit word sent to the VCM 12-bit DAC. Low gain selected for the VCM loop.

REGISTER #8

bit [11, 0] (Dac12b[11, 0]): 12-bit word sent to the VCM 12-bit DAC. High gain selected for the VCM loop.

REGISTER #9

bit [10] (Shock thresh[23):set the shnock sensor threshold value.

Commutation control

DELAYS

The spindle block contains both the low-side and high-side drivers configured as a H bridge for a three phase DC brushless, sensorless motor. In each of the six possible states, two outputs are active, one sourcing current and one sinking current. The third output presents a high impedance to the motor which enables measurement of the BEMF in the corresponding motor coil. The back-EMF comparator output (available on pin SpinDigOut) is processed by the commutation logic circuit to calculate the correct time for the next commutation, which will change the output state.

The commutation block measures then the time between 2 consecutive zero-crossings and determines the actual commutation time and the next motor coils state. All the following situations must be taken into account:
=> Start up, No start, Backwards spin, Run and Manual commutation.

The commutation logic keeps the motor spinning by commutating the motor each time a zero-crossing is detected. The delay between the zero-crossing and the actual output driver change is either internally calculated or programmable via the serial port (useful at start-up: no delay has been measured!).

The internal commutation clock can be monitored on pin SpinDigOut (44). The falling edges are the relevant informations: they are caused by the zero-crossings. If preferred, SpinDigOut can be set to become the back-EMF comparator output, to check if the spindle is already spinning at power up for instance. If the spindle outputs are floating, don't forget to bias them, using the "BiasCT" bit, before considering the BemfCompOut value.
Fig.6 and Fig.7 show typical motor commutation timing diagrams.

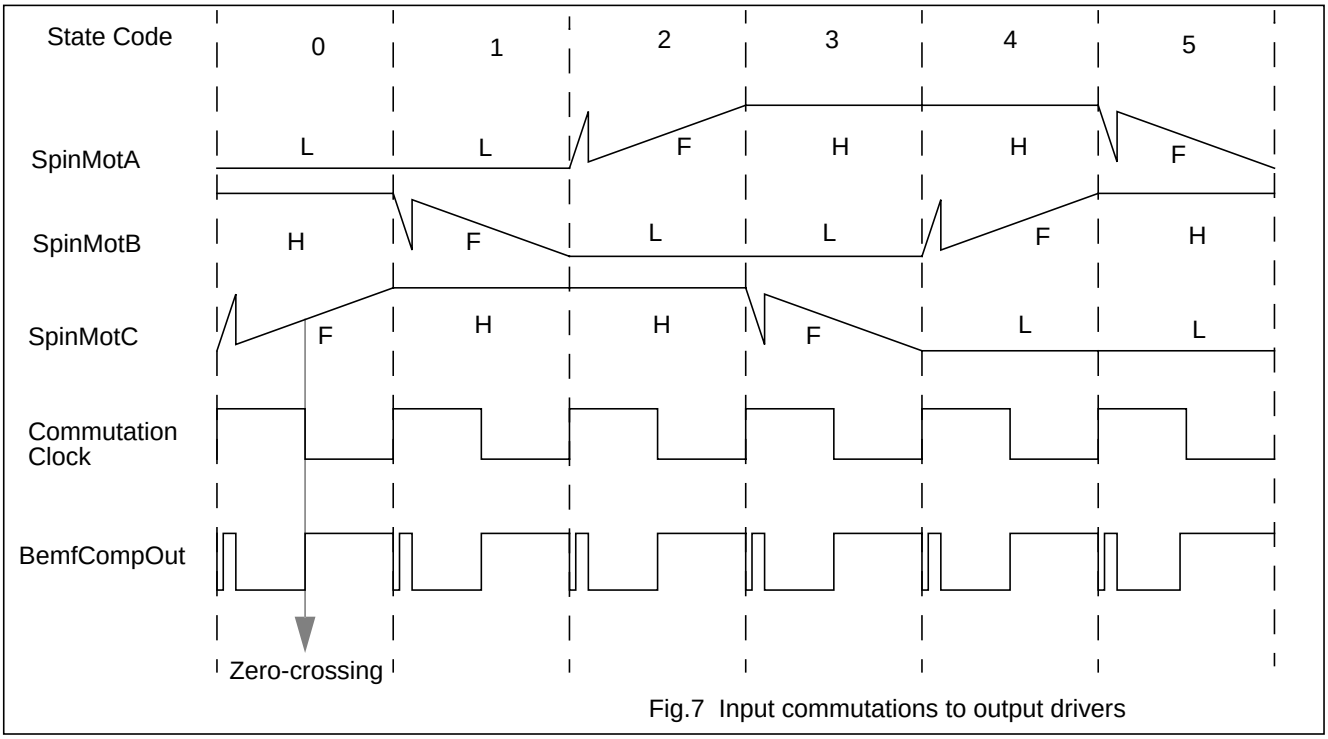

Fig.7 Input commutations to output drivers

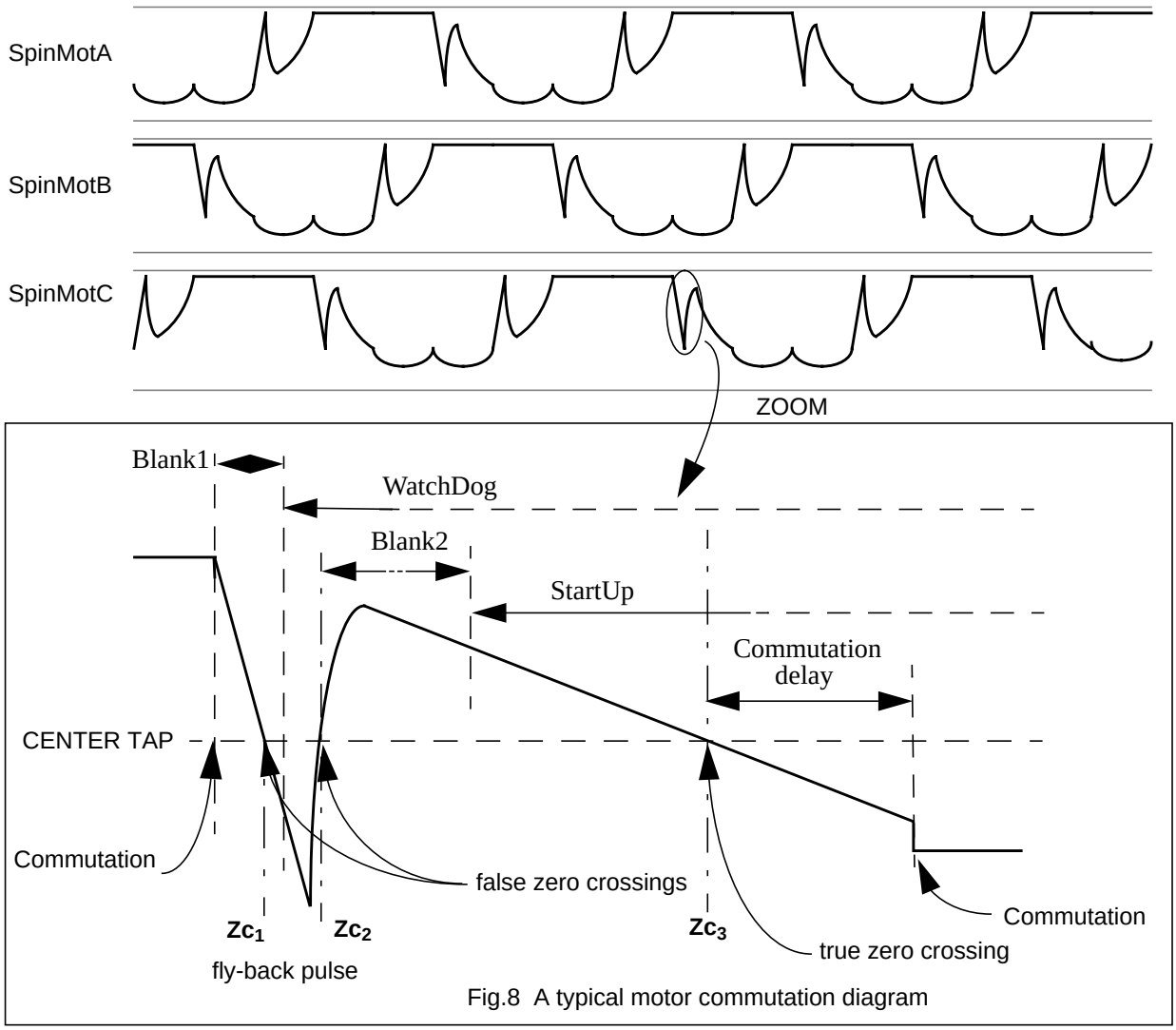

Fig.8 A typical motor commutation diagram

The digital control block ignores any crossing while the **Blank1** timer is counting. This means that the zero-crossing caused by the fly-back pulse leading edge (Z_{C1}) is not seen by the commutation block.

The **WatchDog** timer makes sure that the motor is running forward. If the motor is going backwards, the BEMF voltage will be inverted and the second crossing (Z_{C2}) of the inductive pulse will not occur until the actual BEMF zero crossing. Therefore, if the WatchDog timer expires before a zero-crossing occurs, the motor is assumed to be turning backwards. The commutation is advanced one step to correct this condition. The second inductive zero-cross (Z_{C2}) must occur within the WatchDog time. Therefore, the WatchDog must be set to a time that is greater than the fly-back pulse duration measured when the motor is standing still.

The **Blank2** timer starts counting as soon as the second zero-cross (Z_{C2}) occurs. After the second inductive zero-crossing all extra zero-crossings are ignored during the Blank2 time. This allows the coil voltage to ring slightly without causing a commutation advance.To make the chip smaller, Blank1 and Blank2 have the same value: Blank.

If the motor is not spinning, no BEMF zero-crossing will occur. The **StartUp** timer detects this if it expires before the true zero-crossing (Z_{C3}) has occurred. It will advance the commutation one step if this happens.

The Commutation Delay Limiter (**ComDeLim**) allows to control the maximum commutation delay time. This commutation delay time is equal to half the measured delay between 2 zero crossings ($\Delta Zc_{measured}$). ComDeLim value should be

programmed to be the ***maximum allowable delay value***.
If $\Delta Zc_{measured}$ is lower than ComDeLim, the next commutation delay will be $\Delta Zc_{measured}$ divided by 2.
If $\Delta Zc_{measured}$ is higher than ComDeLim, the next commutation delay will be ComDeLim value divided by 2.
ComDeLim can be limited to guarantee a faster lock after the motor has gone out of lock.

The clock used in the commutation control block is obtained by dividing the master clock of the chip (CLOCK: pin #38) by a clock divider (PRESCALER). This internal clock is named ClockOutPrescaler.
All the delays described above (Blank, WatchDog and StartUp) are generated by a down-counter (called TIMER1). The time between two zero-crossings is measured by a second counter called TIMER2. The commutation delay and the ComDeLim are derived from TIMER2. Both counters are clocked on ClockOutPrescaler clock, which is programmable through the serial interface, using bit 7 & 8 of register #0: (ClockOutPrescaler should be chosen as typically 1 MHz)

Table 4 Clock configurations

PRESCFACTOR1 (BIT 8, REG#0)	PRESCFACTOR0 (BIT 7, REG#0)	CLOCKOUTPRESCALER
0	0	CLOCK/4
0	1	CLOCK/8
1	0	CLOCK/16
1	1	CLOCK/32

TIMER 1

Timer 1 is used to generate Blank, WatchDog and StartUp delays: It loads one of these programmed values and counts down till it reaches zero. All LSB bits are internally set to '1': bits [2:0] for Blank, bits [8:0] for WatchDog, bits [13:0] for StartUp.

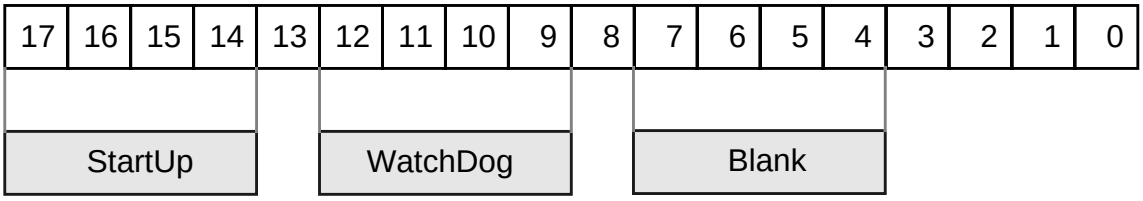

Fig.9 Timer 1 configuration.

Calculations:
The actual delay will be: Delay = (Value * Step) + min, where:
Value = the decimal value programmed in the considered register
Step size = 2^{LSB} / *ClockOutPrescaler*
Min = (2^{LSB} -1) / *ClockOutPrescaler* (bits from 0 to (LSB-1) are internally set to 1)
maximum = ($2^{(MSB+1)}$ -1) / *ClockOutPrescaler*

Table 5 Numeral application with CLOCK = 16 MHz

DELAYS	CLOCKOUTPRESCALER= CLOCK/4 = 4 MHZ			CLOCKOUTPRESCALER= CLOCK/8 = 2 MHZ			CLOCKOUTPRESCALER= CLOCK/16 = 1 MHZ			CLOCKOUTPRESCALER= CLOCK/32 = 0.5 MHZ		
	MIN	STEP	MAX	MIN	STEP	MAX	MIN	STEP	MAX	MIN	STEP	MAX
Blank	3 µs	4 µs	63 µs	7 µs	8 µs	127 µs	15 µs	16 µs	255 µs	31 µs	32 µs	511 µs
WatchDog	127 µs	128µs	2.05 ms	255 µs	256 µs	4.0 ms	511 µs	512 µs	8.2 ms	1023 µs	1024 µs	16.4 ms
StartUp	4.1 ms	65.5 ms	65.5 ms	8.2 ms	8.2 ms	131 ms	16.4 ms	16.4 ms	262 ms	32.8 ms	32.8 ms	524 ms

TIMER 2

TIMER2 is used to measure the delay between two zero-crossings and also to set the maximum commutation delay through comdelim delay:

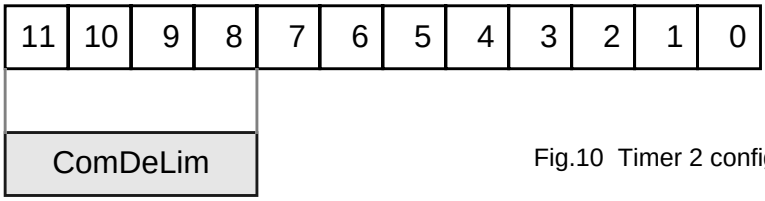

Fig.10 Timer 2 configuration.

Explanation: COMDELIM is the maximum value that can be reached by TIMER 2. So, this is the maximum delay ***between 2 zero-crossings***. The maximum commutation delay is then ***half this value!***

Calculations:

Delay between 2 zero-crossings (Δ Zc):

step size = 2^{LSB} / *ClockOutPrescaler*
min = (2^{LSB}-1) / *ClockOutPrescaler* (bits from 0 to (LSB-1) are internally set to 1)
maximum = ($2^{(MSB+1)}$ - 1) / *ClockOutPrescaler*

Maximum commutation delay:

step size = $2^{(LSB-1)}$ / *ClockOutPrescaler*
maximum = ($2^{(MSB)}$ - 1) / *ClockOutPrescaler*

Table 6 Numeral application with CLOCK = 16 MHz

DELAYS	CLOCKOUTPRESCALER= CLOCK/4 = 4 MHZ			CLOCKOUTPRESCALER= CLOCK/8 = 2 MHZ			CLOCKOUTPRESCALER= CLOCK/16 = 1 MHZ			CLOCKOUTPRESCALER= CLOCK/32 = 0.5 MHZ		
	MIN	STEP	MAX	MIN	STEP	MAX	MIN	STEP	MAX	MIN	STEP	MAX
ΔZ_C	63 µs	64 µs	1.02 ms	127 µs	128 µs	2.05 µs	255 µs	256 µs	4.1 ms	511 µs	512 µs	8.2 ms
ComDeLim	31 µs	32 µs	511 ms	63 µs	64 µs	1.02 ms	127 µs	128 µs	2.05 ms	255 µs	256 µs	4.1 ms

Spindle current loop

The spindle current I_{Spin} is sensed by internal current mirrors and copied to an internal resistor $R_{SpinLoopGain}$. The current loop input is controlled by the internal FLL/PLL speed loop. The transconductance is defined by the following formula (see Fig.3) :

$$G_{Spin}[(A)/(V)] = \frac{\Delta I_{Spin}}{\Delta V_{SpinSpeedFilter}} = \frac{530}{R_{SpinLoopGain}} = \frac{530}{1700\Omega} = 312 mA/V \quad (1)$$

The spindle current loop bandwidth is given by the following formula : (gm means transconductance : di/dv)

$$BW_{SpinCurLoop} = \frac{gm_{OTA} \times \frac{R_{SpinLoopGain}}{530} \times gm_{NMOS}}{2 \cdot \pi \times C_{SpinCompens}} = 65.5 \cdot 10^{-6} \times \frac{\sqrt{I_{Spin}}}{C_{SpinCompens}} \quad (2)$$

where the typical values for gm_{OTA} and gm_{NMOS} are : gm_{OTA} = 50 µA/V & gm_{NMOS} = 2.62 x Sqrt(I_{Spin}) A/V

$BW_{SpinCurLoop}$ should be kept <= 20 kHz, whatever the current. Take care of the fact that the higher the current, the higher the BandWidth => the bandwidth is maximum at Start-Up.

To make sure that the OTA output is 0V when Run/Stop bit = '0', a 30 mV (typ.) offset is introduced inside the OTA. By this way, we make sure that SpinCompens external capacitor is kept discharged until the next start-up.

Spindle FLL/PLL speed loop :

An internal speed loop is provided, intended to work with **12 poles** spindle motors. It is mainly composed of a Frequency Locked Loop. A Phase Locked Loop can be associated when bit 9 in register #5 (PllOn/Off) is '1'. The typical FLL charge pump current is 500 µA while the typical PLL charge pump current is given in table 7 :

Table 7 PLL charge pump typical current (PllCur[1,0] are bits 8 & 7 in register #5):

PLLCUR[1,0]	PLL CH. PUMP CURRENT
00	0.25 µA
01	0.5 µA
10	0.75 µA
11	1 µA

A 15-bit division factor (Speed[14, 0]) is used to set the required speed split in bits [11, 9] in register #5 and bits [11, 0] in register #6:

The Speed[14, 0] division factor can be calculated by :

$$Speed[14,0] = \frac{5}{3} \times \frac{CLOCK}{SpindleSpeed(rpm)} \quad (3)$$

Where CLOCK is between 10 MHz and 33 MHz.

When the spindle is not running (Run/Stop = '0') the FLL charge pump discharge current is active so that the external filter is discharged before the next start-up. When the spindle is running (Run/Stop = '1'), the speed can be continuously monitored on pin SpinMechClock (1 pulse per revolution / 50% duty cycle waveform).

SPINDLE / VCM 6-bit current DAC:

An internal 6-bit current DAC is used to limit the spindle start-up current (bit 6 in register #5 : Dac6ToVcm = '0') or to cancel the VCM loop offset (Dac6ToVcm = '1').

When the 6-bit DAC is used for the spindle, the LSB current is set externally, by means of a 33 kΩ resistor (to have a very good absolute accuracy). The Spindle Current limit is then set by 31 steps of 20 mA. Please note that only the positive codes of the 6-bit DAC can be used, so only (2^5 - 1) = 31 steps can be defined.

Table 8 Spindle Start-up current limit according to the spindle 6-bit DAC code :

INPUT CODE	SPINDLE START-UP CURRENT
000000	0 mA
000001	20 mA
011111	620 mA

When the 6-bit DAC is used for the VCM section, the LSB current is set by an internal resitor to have a good matching with the 2 internal resistors used to set the VCM loop Gain. The VCM current offset is set by steps of :

$$I_{VCMOffset\,(LSB)} = \frac{1.613 \cdot 10^{-3}}{R_{Sense}}\,(A) \quad (4)$$

Table 9 VCM current offset according to the spindle 6-bit DAC code (assuming that R_{Sense} = 1 Ω, 1 LSB = 1.613 mA) :

INPUT CODE	VCM OFFSET CURRENT
011111	+50 mA
000000	0 μA
1111111	-1.613 mA
100001	-50 mA
100000	-50 mA

VCM driver

The VCM is a linear, AB class type with both low-side and high-side drivers configured as a H-bridge. The zero-current reference voltage for the VCM loop is internally set at Vdd5/2=2.5 V. The sense resistor R_{sense} enables the VCM current to be measured through the sense amplifier. The gain of the sense amplifier is internally set to typically 3. The output VcmSenseOut is given by the following equation:

$$VcmSenseOut = 3 \times (VcmSenseInP - VcmSenseInM) + VcmRef \quad (5)$$

Figure 14 presents the VCM sense amplifier.

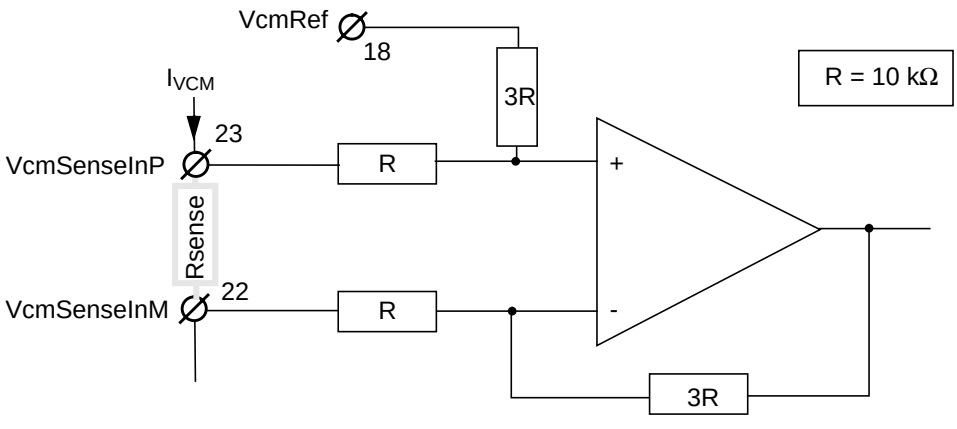

Fig.11 VCM sense amplifier

The error amplifier compares the VcmDacOut(49) input command and the VcmSenseOut(18) sense amplifier output signal to generate the control voltage of the power drivers.

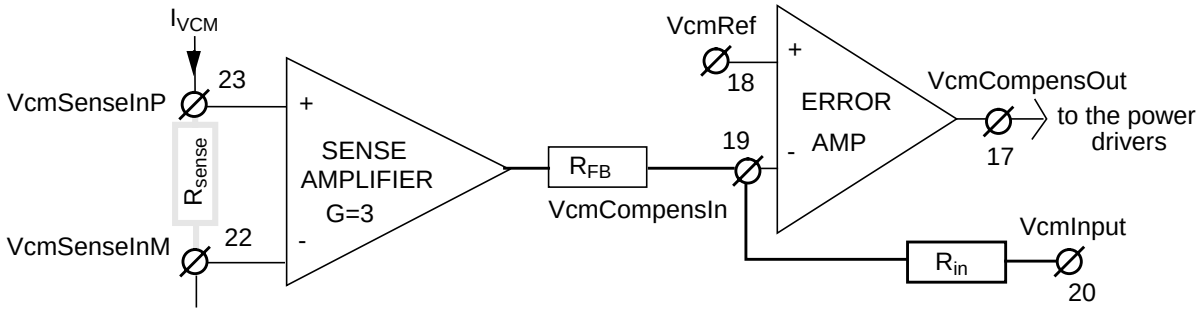

Fig.12 VCM transconductance gain schematic.

$$\frac{VcmDacOut - VcmRef}{R_{in}} = \frac{VcmSenseOut - VcmRef}{R_{FB}} = \frac{3 \times R_{sense} \times I_{VCM}}{R_{FB}} \quad (6)$$

Finally, the transconductance gain of the VCM loop is given by the following equation:

$$G_{VCM}\,[(A)/(V)] = \frac{I_{VCM}}{VcmDacOut - VcmRef} = \frac{R_{FB}}{R_{in}} \times \frac{1}{3 \times R_{sense}} = \frac{0.4}{R_{sense}} \quad (7)$$

VCM 12-bit resistive ladder DAC:

The VCM loop input voltage is provided by an internal signed 12-bit resistive ladder DAC. The output voltage is a linear function of the input code written in register #7 (low gain) or register #8 (high gain), bits [11:0] :

Table 10 Dac12 output voltage versus the input code (1 LSB = 125 µV) when writing in register #7 :

INPUT CODE	DAC12 VOLTAGE
$(7FF)_H$	1.732 V -1 LSB
$(000)_H$	1.482 V
$(FFF)_H$	1.482 V -1 LSB
$(800)_H$	1.232 V

Table 11 Dac12 output voltage versus the input code (1 LSB = 500 µV) when writing in register #8 :

INPUT CODE	DAC12 VOLTAGE
$(7FF)_H$	2.482 V - 1LSB
$(000)_H$	1.482 V
$(FFF)_H$	1.482 V -1 LSB
$(800)_H$	0.482 V

Warning : at power up, the 12-bit DAC needs to be programmed so that it is in a defined state.

VCM back-EMF amplifier

To prevent any actuator crash on the disk when a ramp load is used, an internal VCM back-EMF amplifier is build to monitor the actuator speed. Indeed, the VCM back-EMF is a picture of the actuator speed. The voltage across the VCM motor is divided in several contributions:

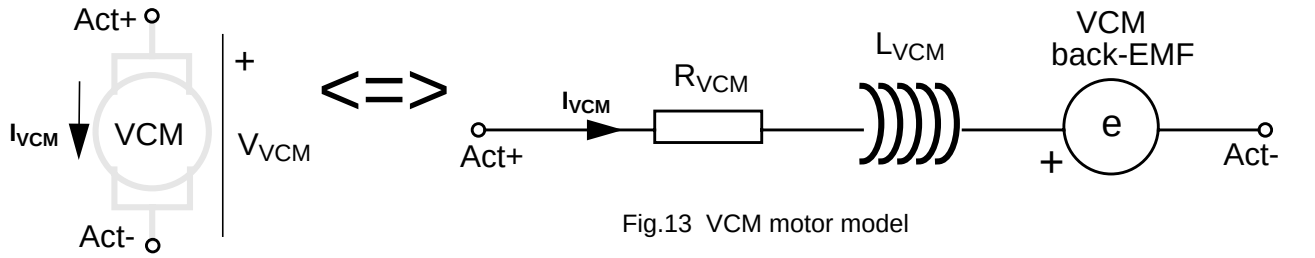

Fig.13 VCM motor model

$$V_{VCM} = (R_{VCM} \times I_{VCM}) + \left(L_{VCM} \times \frac{dI_{VCM}}{dt}\right) + e \quad (8)$$

If the VCM current I_{VCM} can be considered as constant, the back-EMF becomes:

$$e = V_{VCM} - (R_{VCM} \times I_{VCM}) \quad (9)$$

Figure 14 presents the VCM back-EMF amplifier as it is implemented in the TDA5345HT:

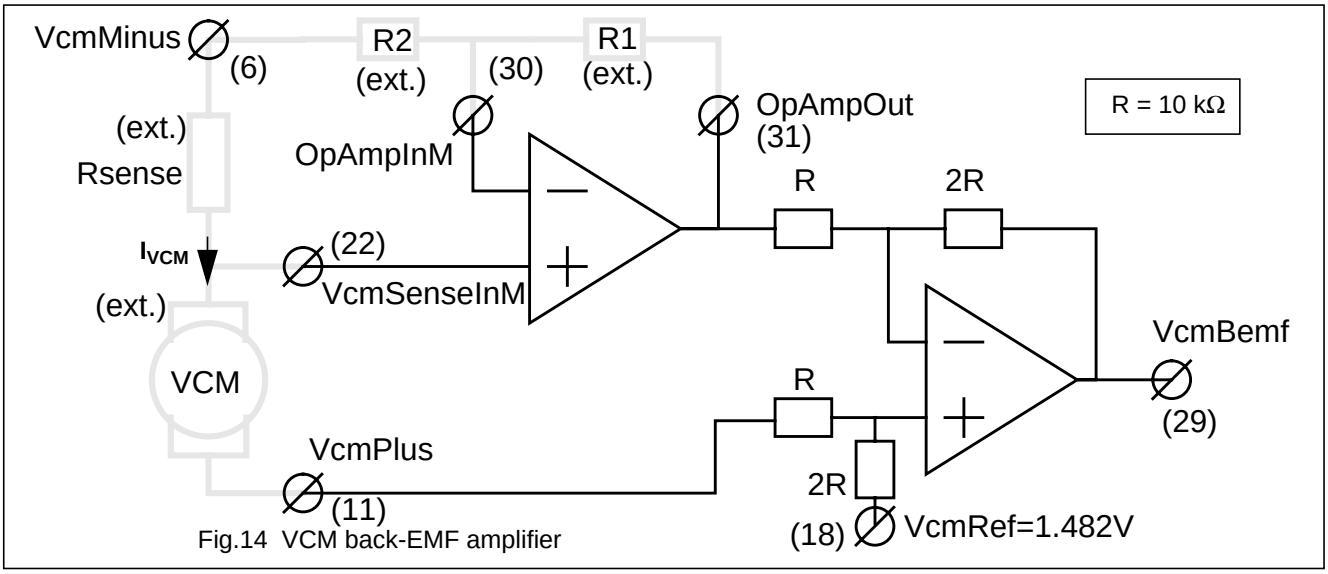

Fig.14 VCM back-EMF amplifier

The first operational amplifier output voltage (OpAmpOut) is:

$$OpAmpOut = VcmSenseInM - \left(\frac{R1}{R2} \times R_{Sense} \times I_{VCM}\right) \quad (10)$$

The VCM back-EMF amplifier output voltage (VcmBemf) is:

$$VcmBemf = 2 \times (VcmPlus - OpAmpOut) + VcmRef \quad (11)$$

$$VcmBemf = 2 \times \left[VcmPlus - \left(VcmSenseInM - \left\langle \frac{R1}{R2} \times R_{Sense} \times I_{VCM} \right\rangle\right)\right] + VcmRef \quad (12)$$

$$VcmBemf = 2 \times \left((VcmPlus - VcmSenseInM) + \left(\frac{R1}{R2} \times R_{Sense} \times I_{VCM} \right) \right) + VcmRef \quad (13)$$

Where:

$$V_{VCM} = -(VcmPlus - VcmSenseInM) \quad (14)$$

and if you set:

$$\frac{R1}{R2} \times R_{Sense} = R_{VCM} \quad (15)$$

you get:

$$VcmBemf = -2 \times (V_{VCM} - R_{VCM} \times I_{VCM}) + VcmRef \quad (16)$$

$$VcmBemf = -2 \times e + VcmRef \quad (17)$$

VCM ramp unload sequence :

The VCM ramp unload sequence can be ordered by either the serial interface or by internal emergency procedures: power down or temperature shut down. **It will not start if VcmSleep bit is '1'**, because the actuator is supposed to be on the ramp already.

Three different states are programmable : first a VCM brake, second a VCM slow retract and then a VCM full power retract.

In all cases, the spindle isolation switch is cut off. If the power transistors are still supplied, the VCM current will come from the power supply, through the isolation switch parasitic diode. If the power transistors are no more supplied, the VCM current will come from the spindle itself. It is used as a generator, thanks to its back-EMF.

When the sequence is initiated by a Power down detection, PorN signal will not go up until the end of the sequence.

Figure 14 shows the link created between the spindle and the VCM power structures to transfer the spindle energy to the actuator :

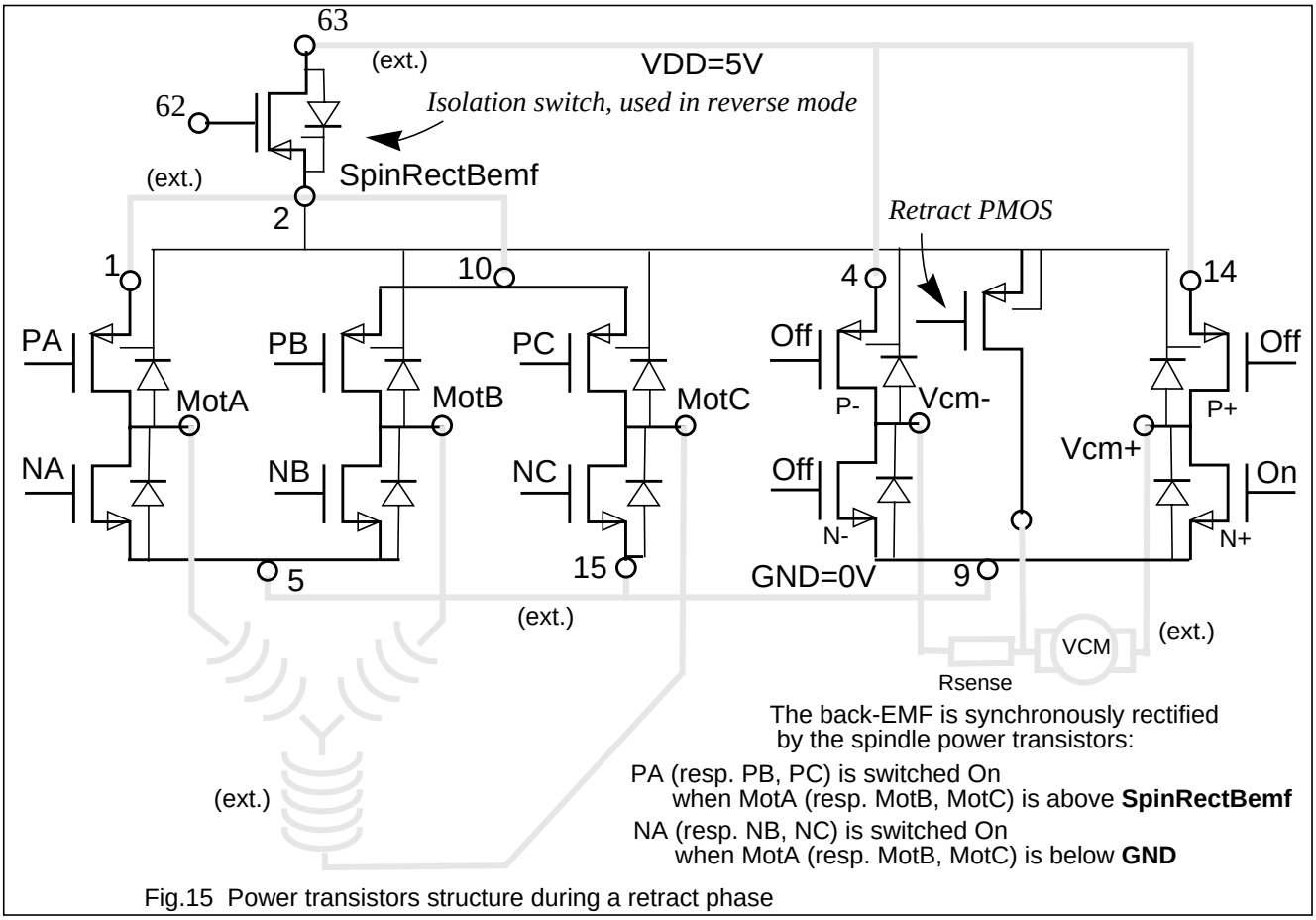

Fig.15 Power transistors structure during a retract phase

During the VCM brake, VCM power transistors N- & N+ are switched fully On while transistors P- & P+ are switched off. During the soft retract step, N- transistor is switched off while the retract PMOS brings some current to the VCM. The control loop is drawn in figure 14 (the voltage on VcmMinus is regulated).

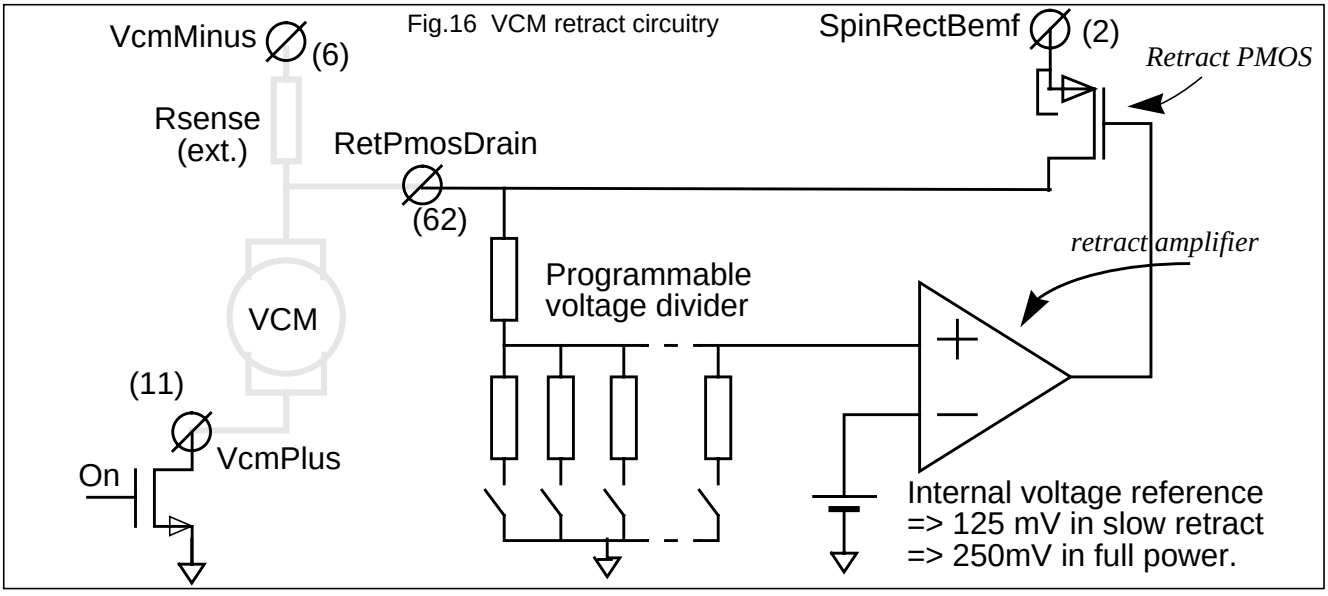

Fig.16 VCM retract circuitry

Table 12 VcmMinus voltage during the slow retract step versus Vretract[2:0] programming (bits [2:0] in register #2):

VRETRACT[2:0]	VCMMINUS VOLTAGE
111	1 V
...	...
001	250 mV
000	125 mV

In full power mode, VcmMinus voltage is limited to 2.8 V. When the spindle back-EMF is used as a supply (power down) the voltage will not be so high. The loop is working in saturation mode and the retract PMOS is fully saturated.

It is possible to have a kind of “soft rising” slope on VcmMinus voltage when switching from the slow retract state (VcmMinus voltage is small) to the full power state (VcmMinus voltage is high). An internal digital counter generates some steps (250 mV high) from $V_{VcmMinus}$(SlowRetract) to $V_{VcmMinus}$(FullPower) when VcmRetSoftRis = ‘1’ (bit 3, reg #2).

During all the VCM ramp unload sequence, a programmable state machine is activated, clocked by the spindle back-EMF on SpinMotA.

If T_{bEMF} is the spindle back-EMF period, the steps duration will vary according to the following table:

Table 13 Brake duration versus the T_VcmBrake[2:0] programming (bits [2:0] in register #3):

T_VCMBRAKE[2:0]	BRAKE DURATION
111	$7*(2*T_{bEMF}) + T_{bEMF}$
...	...
010	$2*(2*T_{bEMF}) + T_{bEMF}$
001	$1*(2*T_{bEMF}) + T_{bEMF}$
000	0

Table 14 Slow retract duration versus the T_SlowRet[5:0] programming (bits [8:3] in register #3):

T_SLOWRET[5:0]	SLOW RET. DURATION
111111	$63*T_{bEMF}+T_{bEMF}$
...	...
000010	$2*T_{bEMF}+T_{bEMF}$
000001	$1*T_{bEMF}+T_{bEMF}$
000000	0

Table 15 Full Power retract duration versus the T_FullPower[2:0] programming (bits [11:9] in register #3):

T_FULLPOW[2:0]	FULL POWER DURATION
111	$7*(32*T_{bEMF}) + T_{bEMF}$
...	...
010	$2*(32*T_{bEMF}) + T_{bEMF}$
001	$1*(32*T_{bEMF}) + T_{bEMF}$
000	0

* Include typical waveform

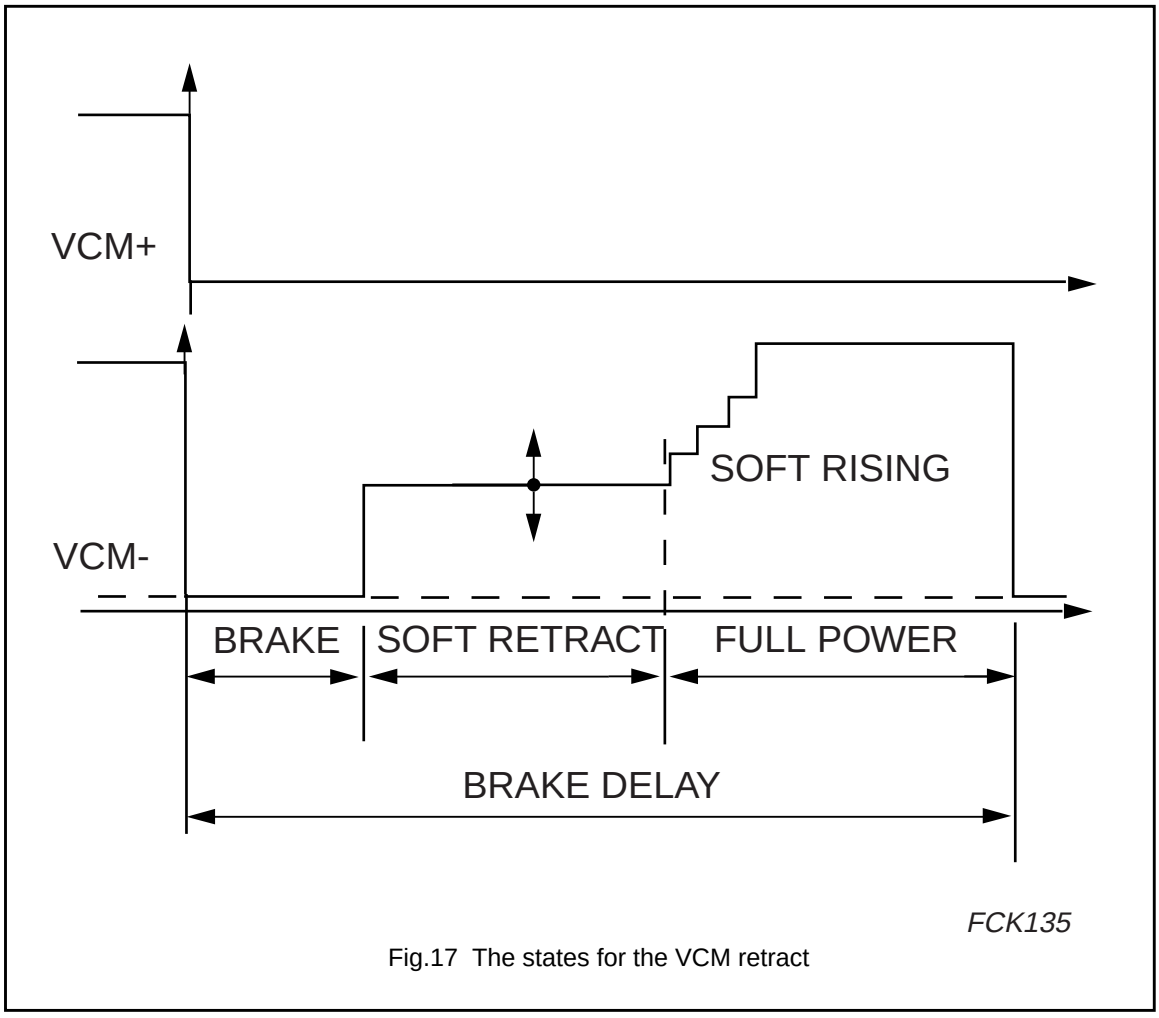

Fig.17 The states for the VCM retract

Spindle brake after retract sequence :

In case of power down, an emergency procedure is initiated by the PorN signal : the spindle back-EMF is synchronously rectified to supply the VCM ramp unload function. At the end of the full power step, a spindle short-circuit brake is activated (SpinMotA, SpinMotB & SpinMotC are together short-circuited to ground). It is supplied by an external reservoir capacitor connected to pin BrakePower (60).

Shock sensor amplifier:

A complete circuitry is included on-chip to control an external shock sensor.
Figure 14 shows a typical application diagram:

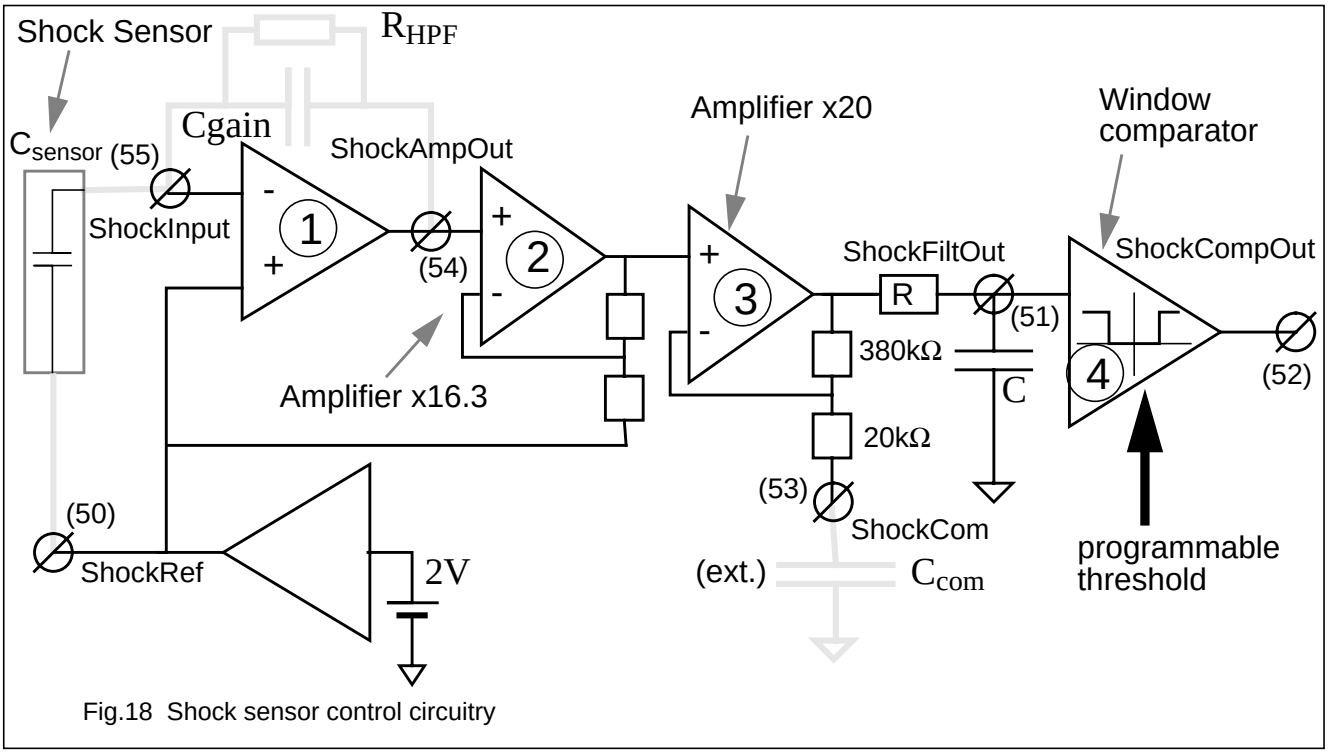

Fig.18 Shock sensor control circuitry

The first amplifier gain is given by : $G = C_{gain}/C_{sensor}$. It has to be set so that the sensor voltage sensitivity becomes 220 µV/G on the 1 st stage output.

The 2nd amplifier stage gain is internally set to 16.3. The 3rd amplifier stage gain is internally set to 20. The external capacitor C_{com} and R_{HPF} have to be chosen so that : C_{com}x20 kΩ = C_{gain}xR_{HPF}. This time constant makes the input high pass filter pole. The internal RC low pass filter pole is 8 kHz typical. The window of the comparator input (ShockCompInP) is programmable through the serial interface. The values are given in the following table:

Table 16 Window comparator threshold versus ShockThresh[1:0] (bits [9,8] in register #4):

SHOCKTHRESH[1:0]	WINDOW	2ND STAGE INPUT SENSITIVITY
000	74 mV	227 µV
001	148 mV	454 µV
010	222 mV	681 µV
011	296 mV	908 µV
100	370 mV	1.135 mV
101	444 mV	1.362 mV
110	518 mV	1.589 mV
111	592 mV	1.816 mV

Temperature monitor:

The TDA5345HT includes an analog circuitry that monitors the junction temperature.
Figure 25 shows its diagram:

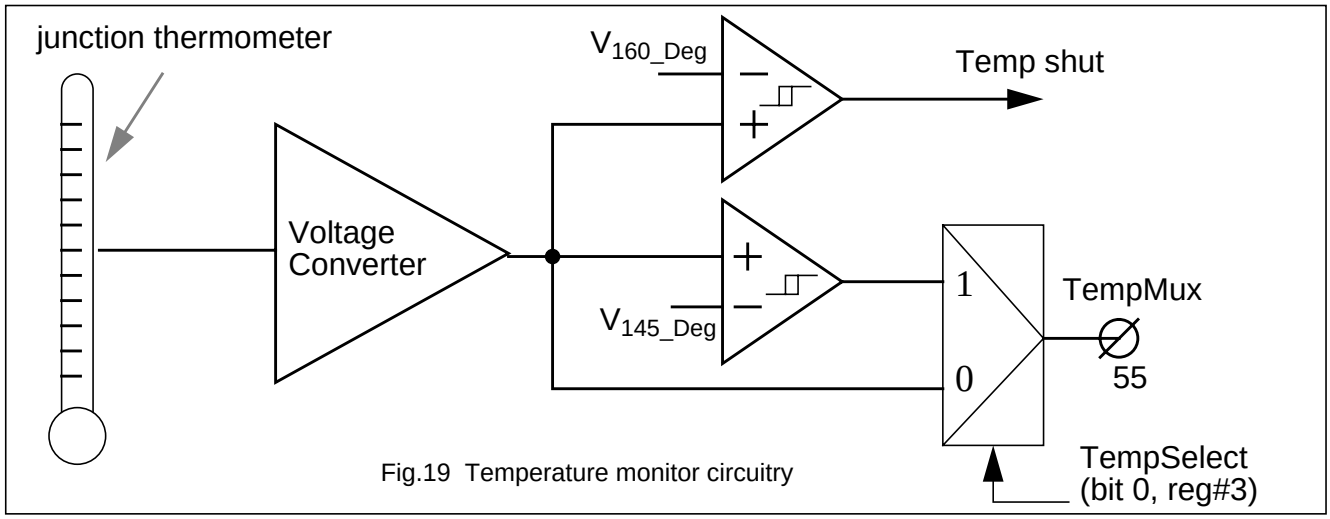

Fig.19 Temperature monitor circuitry

The device is protected against over-temperature by the temperature shutdown circuit. When the temperature of the chip exceeds 160 °C, the device is automatically set to a VCM retract and a spindle disable mode. It remains in this mode until the temperature goes below 160 °C - 30 °C = 130 °C (30 °C is an internal hysteresis).

During normal operation, the signal TempMux provides either a voltage that is function of the chip temperature when TempSelect = '1' or a digital warning when TempSelect = '0'.

When the analog information is selected, the equation of the voltage versus the temperature is:

$$V_{TempMux} = 2.954 - \left(7.55 \cdot 10^{-3}\right) \times Temperature\,(°C) \quad (18)$$

When the digital information is selected, you get a temperature warning on pin TempMux (57). If the internal temperature over passes 145 °C, TempMux = '1' and remains high until the temperature comes below 130 °C (see Fig.19).

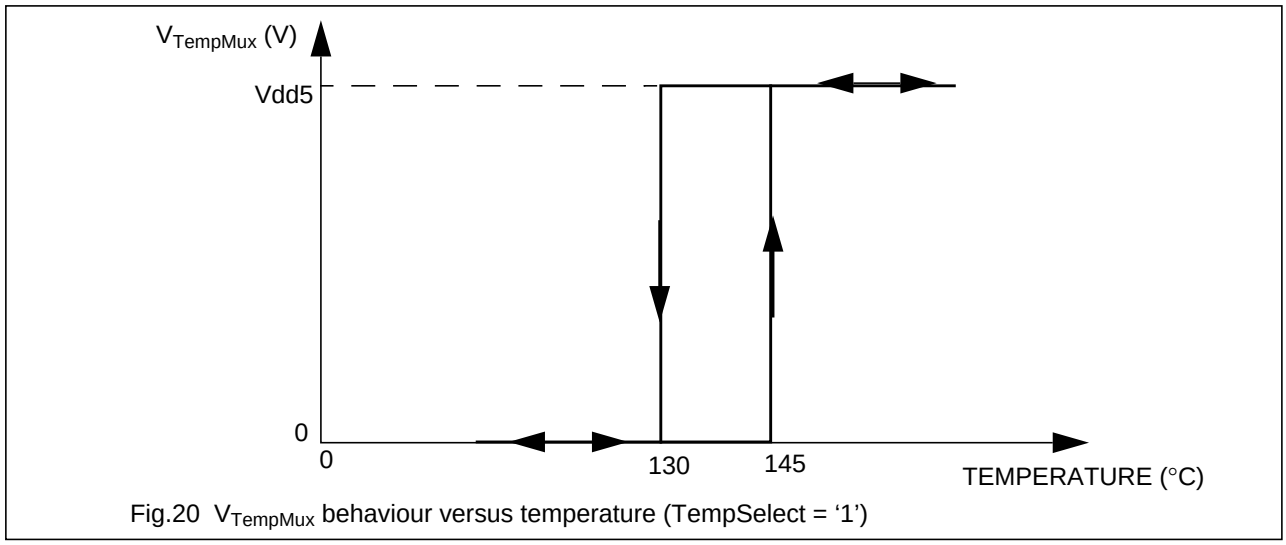

Fig.20 $V_{TempMux}$ behaviour versus temperature (TempSelect = '1')

IT IS STRONGLY ADVISED TO USE THE TempMux INFORMATION (analog or digital) TO GENERATE EMERGENCY PROCEDURES INSTEAD OF WAITING FOR THE TEMPERATURE SHUT DOWN MODE TO TRIGGER. The temperature shut down has to considered as an ultimate self-protection.

Power on reset

The Power On Reset circuit monitors the voltage level of +5 V supply voltage (pin named VddAna1).

The PorN output (pin #25) is set HIGH when the +5 V supply voltage arise above a specified voltage threshold plus an hysteresis. This LOW to HIGH transition is delayed by a time T_C that is determined by the external PorCap capacitor (connected to pin #26).

This PorN output remains HIGH until +5 V supply drops below its voltage threshold. PorN output immediately becomes LOW. A brake after retract is initiated and the digital section is reset while PorN remains LOW.

The C_{PorCap} capacitor is charged by a constant current I_{PorCap}. The voltage on PorCap pin is compared to the POR circuit reference voltage V_{PorRef}. The T_C time is set then by the following equation:

$$T_C = C_{PorCap} \times \frac{V_{PorRef}}{I_{PorCap}} = C_{PorCap} \times \frac{1.23V}{2 \cdot 10^{-6}} = C_{PorCap} \times 615 \cdot 10^3 \quad (19)$$

The T_C time value only depends on the external C_{PorCap} capacitor value.

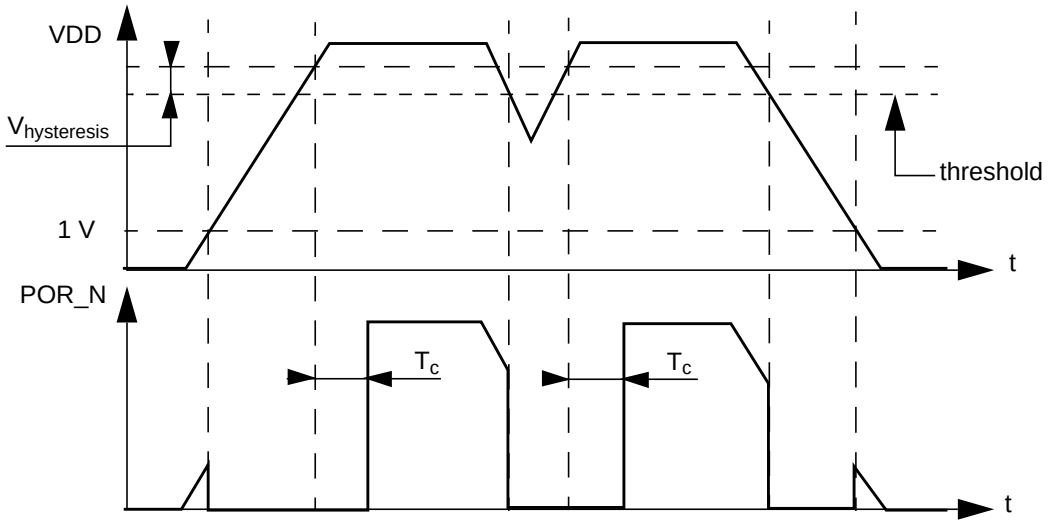

Fig.21 Power on reset timing

The value of the +5 V supply threshold voltage can be adjusted by adding an external resistor divider on the Por5Adj(28) . Internally, pin is designed as it is described in figure 20.

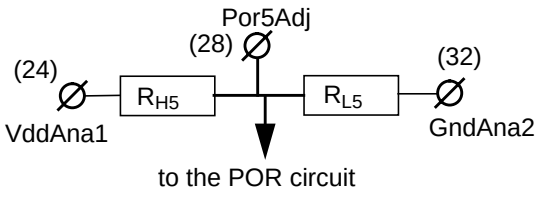

Fig.22 Por5vAdj pin

It is advised to connect external capacitors on pins Por5Adj to filter the power supplies noise. See figure 21.

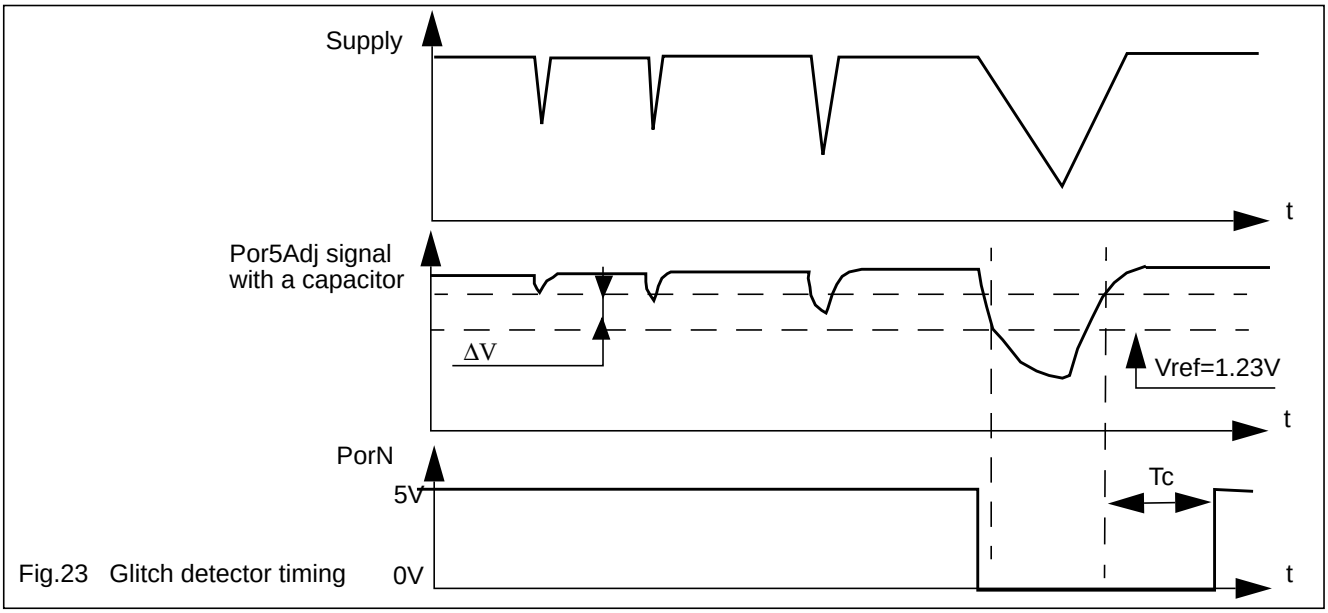

Fig.23 Glitch detector timing

The PorN output can also be driven by the retract sequence manager:

If there is a power supply failure at the sequence start-up or during the sequence, PorN will be kept low during all the programmed sequence, what ever the supply is restored or not.

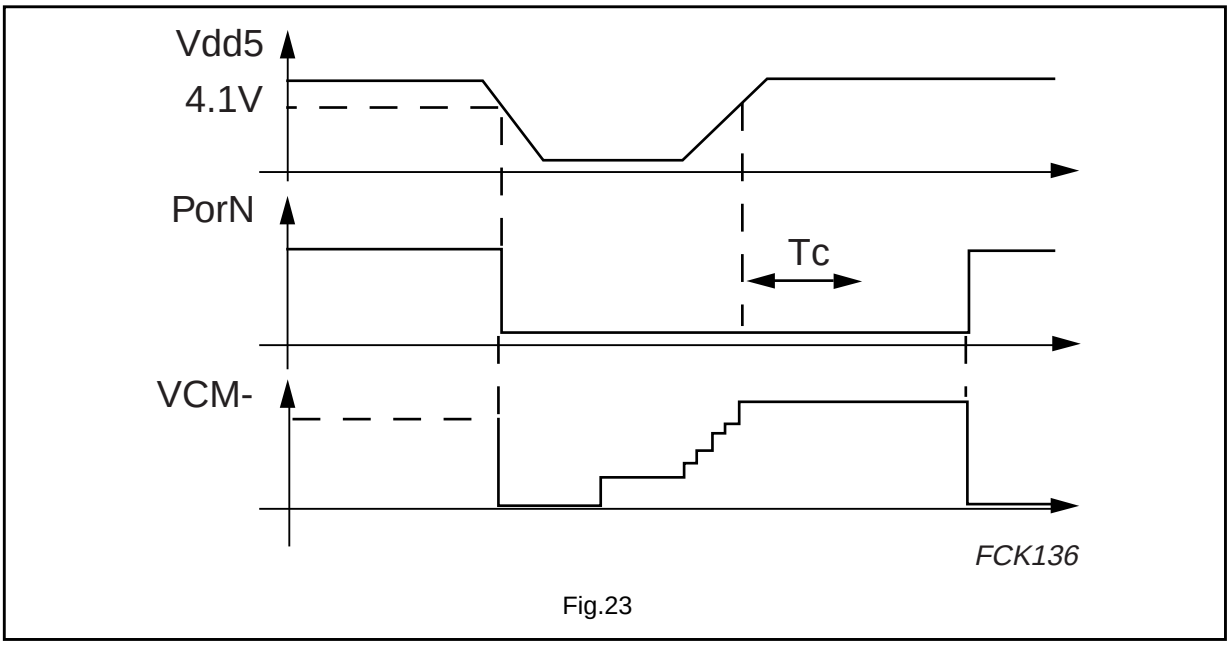

Fig.23

Caution !!

It is not allowed to wake the VCM up (VcmSleep = ‘0’’) if the spindle is not on speed, because a retract sequence would start on a power supply failure without any clock (generated from the spindle back-EMF). PorN would be maintained low by the retract manager, waiting for clock pulses.

3.3V linear regulator:

The Tda5345HT includes an analog amplifier suited to drive an external NPN that will supply the 3.3 V digital chips used in the application **together with the internal digital outputs** (pins SpinDigOut (44), SpinMechClock (43), PowerFault (37), ShockCompOut (52), TempMux (57)). The external pin Reg3v3PwrUp is used to enable (Reg3v3Pwr = 5 V) or disable the regulator (Reg3v3Pwr = 0 V). When Reg3v3Pwr = 0 V, it is possible however to wake the regulator up through the Reg3v3Enable bit (bit number 1 in register #4).

It has been designed to minimise the external components count.
Figure 25 shows the regulator diagram:

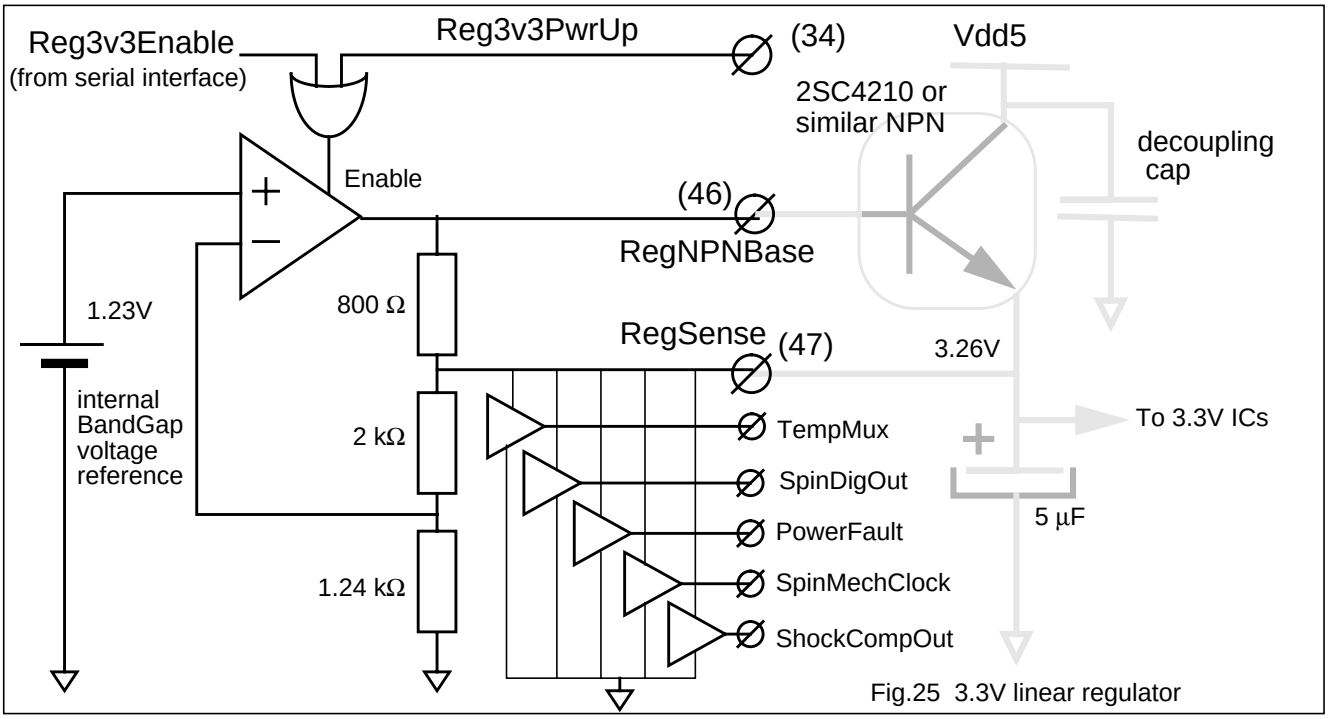

Fig.25 3.3V linear regulator

Negative supply regulator (-3 V) :

A capacitor-based negative supply regulator is also provided.

Due to process limitations, 2 external shottky diodes need to be added to the 2 external capacitors to make it work.
Figure 25 shows the regulator diagram:

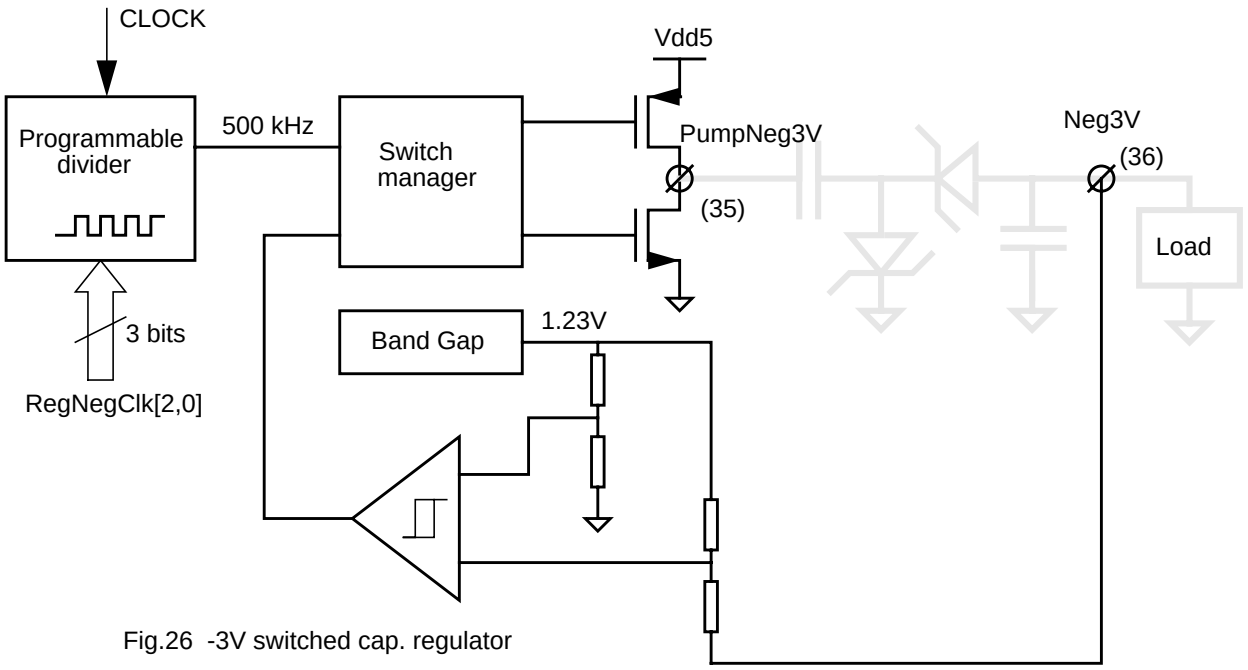

Fig.26 -3V switched cap. regulator

Depending on the external CLOCK value, the programmable CLOCK divider has to be programmed according to the following table :

Table 17 Division factor to program in order to get 500 kHz for the -3 V switched cap. regulator :

CLOCK	REGNEGCLK[2:0]	DIVISION FACTOR
10 MHz	000	20
12.5 MHz	001	22
15 MHz	010	30
16.5 MHz	011	32
20 MHz	100	40
25 MHz	101	50
30 MHz	110	60
33 MHz	111	66

Adjustable bandgap :

An internal regulated voltage source (called BandGap) delivers a very accurate voltage to many different circuitry inside the IC. This voltage (1.23 V) is almost independant of power supply, temperature and process spread. However, there is still a +/- 3% spread on this voltage. To come to about +/- 0.5%, it is possible to adjust this voltage from an external micro controller with a very accurate voltage source and an ADC. The following table gives the voltage added or substracted to the BandGap voltage according to the code written in register 2, bit 4 to 6.

Table 18 BandGap :

BDGAPADJ[2,0]	VOLTAGE ADJUSTMENT
011	-27.6 mV
010	-18.4 mV
001	-9.2 mV
000	0 mV
111	9.2 mV
110	18.4 mV
101	27.6 mV
100	0 mV

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltage						
$V_{DD5A/D}$	+5 V supply voltage		4.5	5.0	5.5	V
Voice coil motor driver						
I_{out}	maximum VCM output current		–	400		mA
R_{DSon}	VCM power MOS total on resistance	T_j = 140 °C V_{DD5} = 4.5 V	–	–	1.5	Ω
Spindle motor driver						
$I_{out\_StartUp}$	maximum spindle output current	start-up	-	620		mA
I_{out_Brake}	spindle output current	Brake	-	-	1.5	A
R_{DSon}	spindle power MOS total on resistance	T_j = 140 °C V_{DD5} = 4.5 V	-	-	1.5	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA5345HT	TQFP64	plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.2 mm	SOT 357BB6

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD5A/D}$	+5 V supplies	indefinite time period	- 0.3	5.5	V
$V_{DD5A/D}$	+5 V supplies	see note1	-0.3	7	V
$V_{PeakVCM}$	VCM drive output voltage	Inductance connected to VCM+ and VCM-	–0.5	V_{DD5} + 0.5	V
$I_{PeakVCM}$	VCM drive output peak current	peak < 0.5 s		1.0	A
$V_{PeakSpin}$	spindle drive output voltage	Inductance connected to SpinMotA, B & C.	-0.5	V_{DD5} + 0.5	V
$I_{PeakSpin}$	spindle drive output peak current	peak < 0.5 s		2.0	A
V_i	other pins	I < 1 mA	-0.5	V_{DD5} + 0.5	V
P_{tot}	total Power dissipation			1.1	W
T_{stor}	IC storage temperature		–55	+125	°C
$T_{j(max)}$	junction temperature		–	+140	°C

Note to the limiting values:

1. Stress beyond these levels may cause permanent damage to the device. This is a stress rating only and functional operation of the device under this condition is not implied.

RECOMMANDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DDN}	supply voltage	4.5	5.5	V
T_{AMB}	operating ambient temperature	0	85	°C
T_{JUNC}	junctiontemperature	0	140	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

ESD according to MIL STD 883C - method 3015 (HBM 1 500 Ω, 100pF) 3 pulses (+) and 3 pulses (-) on each pin versus ground - Class 1: 0 to 1 999 V

THERMAL RESISTANCE

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	from junction to ambient in free air (TQFP64, SOT 357BB6)	50	°C/W

This is obtained in a PCB tailored to heat dissipation : pin number 16, 32, 48, 64 have to be connected to a good ground layer to improve the IC heat dissipation.

ELECTRICAL CHARACTERISTICS
(Condition: V_{DD5} = 4.5-5.5 V; T_{AMB} = 0-85 °C; unless otherwise specified); GBD means Guaranted by Design.

1. Supply current

1-1 Analog and power supply (pin 4, 14, 63, 24, 56together) when there is no current in spindle & VCM motors

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
I_{Sleep}	sleep current	all Sleep bits = '1'		1.1		mA
I_{Sleep1}	sleep mode 1 current	only Spindle is active		8.8		mA
I_{Sleep2}	sleep mode 2 current	only ShockSen is active		2.7		mA
I_{Sleep3}	sleep mode 3 current	only -3 V reg is active		8		mA
I_{Sleep4}	sleep mode 4 current	only DAC12 is active		4.4		mA
I_{Sleep5}	sleep mode 5 current	only DAC12 & VCM are active		9		mA
I_{Supply}	supply current	all sections are active		25.5		mA

1-2 digital supply (Vdd5Dig)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
I_{Sleep}	sleep current	spinSleep bits = '1'		56		µA/MHz
I_{Supply}	supply current	spinSleep bits = '0'		78		µA/MHz

2. DIGITAL section

2-1 Inputs / Outputs (3.3 V regulator ENABLED !)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{IH}	high level input voltage		2.0			V
V_{IL}	low level input voltage				0.8	V
V_{OH}	high level output voltage	(I_{OUT} = 100 µA)	V_{3v3}-0.5			V
V_{OL}	low level output voltage	(I_{OUT} = 100 µA)			0.4	V
$t_{r/f}$	rise/Fall time	C = 20 pF, GbD			20	ns
I_{IN}	input leakage current				+/- 1	µA

2-2 16-bit serial interface

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
f_{SCLK}	serial Clock	GbD			33	MHz
δ_{SCLK}	serial Clock duty cycle	GbD	30	50	70	%
tr_{SCLK}	serial Clock rise time	GbD			10	ns
tf_{SCLK}	serial Clock fall time	GbD			10	ns
t_{START}	chip Select to first Active clock edge	GbD	T_{SCLK}/2			ns
t_{SU}	data to clock setup time	GbD	8			ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
t_{HD}	clock to data hold time	GbD	2			ns
t_{FINISH}	last active clock to chip select inactive on write	GbD			$T_{SCLK}/2$	ns
t_{WAIT}	time between successive serial port accesses	GbD	5			CLOCK cycles

3. Spindle circuits

3-1 Spindle driver: (assuming that Resistor @ pin RefCurRes is exactly 33 kΩ)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT.
R_{DSon}	total FET resistance	I_{SPIN} = 620 mA			1.5	Ω
$I_{StartMax}$	maximum start-up current	DAC6[5,0] = “011111”		620		mA
$I_{StartStep}$	start-up current step			20		mA
$I_{StartRes}$	start-up current resolution		5	5		bits
I_{RUN}	running current	continuous			300	mA
SR_1	fly-backs slew rate control	FlyBackSlope[0,1] = “00”	19	26.5	34	mV/µs
SR_2	fly-backs slew rate control	FlyBackSlope[0,1] = “01”	48	59	70	mV/µs
SR_3	fly-backs slew rate control	FlyBackSlope[0,1] = “10”	105	124	143	mV/µs
SR_4	fly-backs slew rate control	FlyBackSlope[01] = “11”	222	256	290	mV/µs
ACC_{R_FB}	relative accuracy on the 6 fly-backs slew-rate		-20		+20	%
V_{fbmax}	max voltage on spinmotx	positive fly-back, I <100 mA	Vdd5+ 0.05	Vdd5+ 0.2	Vdd5+ 0.35	V
V_{fbmin}	min voltage on spinmotx	neg. fly-back, I <100 mA	-0.35 V	-0.2 V	-0.05 V	V
I_{BP}	brake power leakage	PorN = “0”, GbD		5	250	nA

3-2 Spindle current loop (assuming that Resistor @ pin RefCurRes is exactly 33 kΩ)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ACC_{StCur}	spindle start-up current accuracy	I_{StUp} > 400 mA	-6		+6	%
$ACCR_{StCur}$	current relative accuracy between each phase	I_{StUp} > 400 mA	-5		+ 5	%
gm_{OTA}	OTA transconductance	GbD	35	50	65	µA/V

3-3 Spindle Fll Charge Pump (assuming that Resistor @ pin RefCurRes is exactly 33 kΩ)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{ch/disch}$	charge/discharge current		465	500	535	µA
SYM_{Cur}	charge/discharge currents symetry		0.98		1.02	
$t_{r/f}$	rise/Fall time	GbD		1	2	ns

3-4 Spindle Pll Charge Pump (assuming that Resistor @ pin RefCurRes is exactly 33 kΩ)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{ch/disch00}$	charge/discharge current	PllCur[1, 0] = “00”	0.212	0.25	0.287	µA
$I_{ch/disch01}$	charge/discharge current	PllCur[1, 0] = “01”	0.425	0.5	0.575	µA
$I_{ch/disch10}$	charge/discharge current	PllCur[1, 0] = “10”	0.612	0.72	0.828	µA
$I_{ch/disch11}$	charge/discharge current	PllCur[1, 0] = “11”	0.808	0.95	1.09	µA
SYM_{Cur}	chargedischarge currents symetry		0.93		1.07	
	rise/Fall time	GbD		1	2	ns

3-5 back-EMF comparator

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
V_{OSen}	comparator offset	start up mode	1	8	15	mV
V_{OSdis}	comparator offset	running mode	-5	0	5	mV
V_{CT}	center tap bias voltage	biasCt = ‘1’ or PorN = ‘0’		SpinRect Bemf/2		V

4. VCM circuits

4-1 VCM driver

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
R_{DSon}	total FET resistance	(I_{VCM}= 400 mA)			1.5	Ω
I_{OS}	output offset current	DAC12 = “00000000000” & R_{Sense} = 1 Ω	-10		+10	mA
$I_{Max+400}$	maximum positive current	high Gain, without offset	384	400	416	mA
$I_{Max-400}$	maximum negative current	high Gain, without offset	-416	-400	-384	mA
$I_{Max+100}$	maximum positive current	low Gain, without offset	92.5	98.5	102.5	mA
$I_{Max-100}$	maximum negative current	low Gain, without offset	-102.5	-98.5	-92.5	mA
Lin	transconductance linearity	3 different sections measured	-3		+3	%
I_{QUIES}	quiescent current	2 legs of the H-bridge		3.4	15	mA
$V_{VcmVdd5Div2}$	reference voltage accuracy	Ref = Vdd5/2	-3		+3	%
G_{PD}	power driver gain		4.8	4.95	5.1	V/V
DISTO	crossover distortion	GbD			0	
V_{fbmax}	max voltage on Vcm+ or Vcm-	positive fly-back, I<100 mA	Vdd5+ 0.1	Vdd5+ 0.2	Vdd5+ 0.3	V
V_{fbmin}	min voltage on Vcm+/-	negative fly-back, I<100 mA	-0.3	-0.2	-0.1	V
$V_{RetRefSR}$	retract circutry ref voltage	slow retract mode	110	125	140	mV
$V_{RetRefFP}$	retract circutry ref voltage	full power retract mode	220	250	280	mV
V_{RetLim}	retract voltage limitation	full power retract mode	2.45	2.8	3.14	V
R_{RetTot}	total mos resistance in retract mode	spinRectBemf >= 2.5 V GbD			3.5	Ω

4-2 VCM current control

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
GBW	error amplifier bandwidth	@ unity Gain, GbD	4	5.5		MHz
V_{VcmRef}	Vcm loop ref. voltage	generated by DAC-12	1.402	1.482	1.562	V
$V_{ClampOutL}$	error amp out clamping	Vdd5 = 5 V	1.2	1.3	1.4	V
$V_{ClampOutL}$	error amp out clamping	Vdd5 = 5 V	3.6	3.7	3.8	V

4-3 VCM current sense amplifier

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ComMod}	input voltage range		-0.3		V_{DD5} +0.3	V
BW	bandwidth	GbD	260	530		kHz
R_{FB}	feed back resistor		2.5	3.145	3.9	kΩ
PSRR	power supply rejection ratio	@ 1 kHz, GbD	60			dB
CMRR	common mode rejection ratio	@ 1 kHz, GbD	60			dB

4-4 VCM back-EMF amplifier

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{ComMod}	input voltage range	both OpAmps	-0.3		V_{DD5} +0.3	V
V_{OL}	minimum output voltage	both OpAmps, GbD		100		mV
V_{OH}	maximum output voltage	both OpAmps, GbD		V_{DD5} -0.1		V
PSRR	power supply rejection ratio	both OpAmps, @ 1 kHz, GbD	60			dB
CMRR	common mode rejection ratio	both OpAmps, @ 1 kHz, GbD	60			dB
GBW	unity-gain bandwidth		0.77	1.6		MHz
	1rst stage input offset		-5		+5	mV
G_{BEMF2}	2nd stage amplifier gain		1.96	2	2.04	
V_{OS2}	2nd stage output offset		-20		+20	mV

4-5 VCM DAC12

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$RESO_{12}$	resolution		12	12		Bits
t_{SET}	settling time	to within 0.5 LSB			2.0	µs
$Vref_{HighHG}$	output voltage @ code 7FF	code written to register #8	2.382	2.482	2.582	V
$Vref_{HighLG}$	output voltage @ code 7FF	code written to register #7	1.652	1.732	1.852	V
$Vref_{Middle}$	output voltage @ code 000		1.422	1.482	1.542	V
$Vref_{LowLG}$		code written to register #7	1.192	1.232	1.272	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{ClampOutL}$	output voltage @ code 800	code written to register #8	0.462	0.482	0.502	V
INL_{12}	integral non-linearity		-5		+5	LSB
DNL_{12}	differential non-linearity		-0.5		+0.5	LSB

4-6 VCM offset current using DAC 6

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
$RESO_6$	resolution		6	6		Bits
$t_{SetFull}$	settling time, full range	GbD			2.0	µs
t_{SetLSB}	settling time, 1 LSB	GbD			1.0	µs
$I_{OffFullPos}$	full scale positive current		45	50	55	mA
$I_{OffFullNeg}$	full scale negative current		-55	-50	-45	mA
INL_6	integral non-linearity		-1		+1	LSB
DNL_6	differential non-linearity		-0.5		+0.5	LSB

5. Others features

5-1 Power-On-Reset circuit:

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{T5}	threshold voltage level for the 5 V supply.		3.98	4.1	4.22	V
V_{H5}	5 V detection hysteresis		80	110	140	mV
R_{L5}	resistor between Por5Adj and GND			54		kΩ
$RATIO_{5v}$	por5Adj resistors ratio	$Ratio_5 = R_{L5} / (R_{L5} + R_{H5})$		0.3		
i_{CPOR}	por cap current charge			2.4		µA
V_{OP}	minimum operating voltage	GbD			0.5	V
V_{OL}	low level output voltage	I_L = 1 mA			0.5	V
R_{PU}	pull up resistor	between Vdd5 & PorN	14	20	26	kΩ
t_{RES}	response time			0.5	1	µs

5-2 Low voltage monitor circuit:

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{FAULT}	fault detect voltage		4.08	4.2	4.32	V
V_{Hfault}	fault detection hysteresis		70	100	130	mV
t_{RES}	response time			0.5	1	µs

5-3 Thermal monitor

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OLT}	output voltage at low temp	T_{JUNC} = 0 °C, TempSel = 1		2.954		V
V_{OHT}	output voltage at high temp	T_{JUNC} = 150 °C, TempSel =1		1.896		V
V_{ONT}	output voltage at 25 °C	T_{JUNC} = 25 °C, TempSel =1		2.769		V
K_{TEMP}	temperature coefficient			-7.55		mV/
T_{Warn}	thermal warning threshold	tempSel = 0		145		°C
T_{Why}	thermal warning hysteresis	tempSel = 0		15		°C
T_{Shut}	temperature Shutdown			160		°C
T_{Shy}	thermal Shutdown hysteresis			30		°C

5-4 Shock Sensor

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
I_{leak}	shockinput leakage current	@ Vref = 2 V, GbD			5	nA
S_{in}	input sensitivity	@ 1 kHz, GbD	35			µV
Fc_{RC}	RC filter cut-off frequency		6	8	10	kHz
V_{T1}	2nd stage input window	shockThreh[2, 0] = “000”	122	227	306	µV
V_{T2}	2nd stage input window	shockThreh[2, 0] = “001”	386	454	522	µV
V_{T3}	2nd stage input window	shockThreh[2, 0] = “010”	612	681	750	µV
V_{T4}	2nd stage input window	shockThreh[2, 0] = “011”	816	908	1000	µV
V_{T5}	2nd stage input window	shockThreh[2, 0] = “100”	1021	1135	1248	µV
V_{T6}	2nd stage input window	shockThreh[2, 0] = “101”	1226	1362	1498	µV
V_{T7}	2nd stage input window	shockThreh[2, 0] = “110”	1430	1589	1747	µV
V_{T8}	2nd stage input window	shockThreh[2, 0] = “111”	1634	1816	1998	µV

5-5 3.3 V DC-DC linear converter

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
I_{SOURCE}	source current		5			mA
I_{SINK}	sink current			250		µA
C_{DEC}	external decoupling cap			4.7		µF
V_O	output voltage	I_{LOAD} constant & NPN V_{BE} <= 0.7 V	3.15	3.3	3.45	V
V_{O_4v1}	output voltage	same as V_O +Vdd5 = 4.1 V	3.05	3.2	3.45	V
BW	control loopband width	GbD		600		kHz

Note:

1. **External NPN: 2SC4210 for instance**

5-5 -3 V switched capacitor regulator

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	Unit
I_{OUT_max}	maximum output current		100			mA
V_{OUT}	output voltage	shottky diodes V_f <= 0.4 V	-2.88	-3.0	-3.12	V
V_{OUT_4v1}	output voltage	shottky diodes V_f <= 0.4 V, t_{sw} < 100ps & Vdd5 = 4.1 V	-2.7			V
R_O	output ripple	Iout between 20 and 100 mA + Note 1			30	mV

Note:

1. C_{LOAD} >= 9.4 µ**F , C_{PUMP} = 4.7** µ**F**

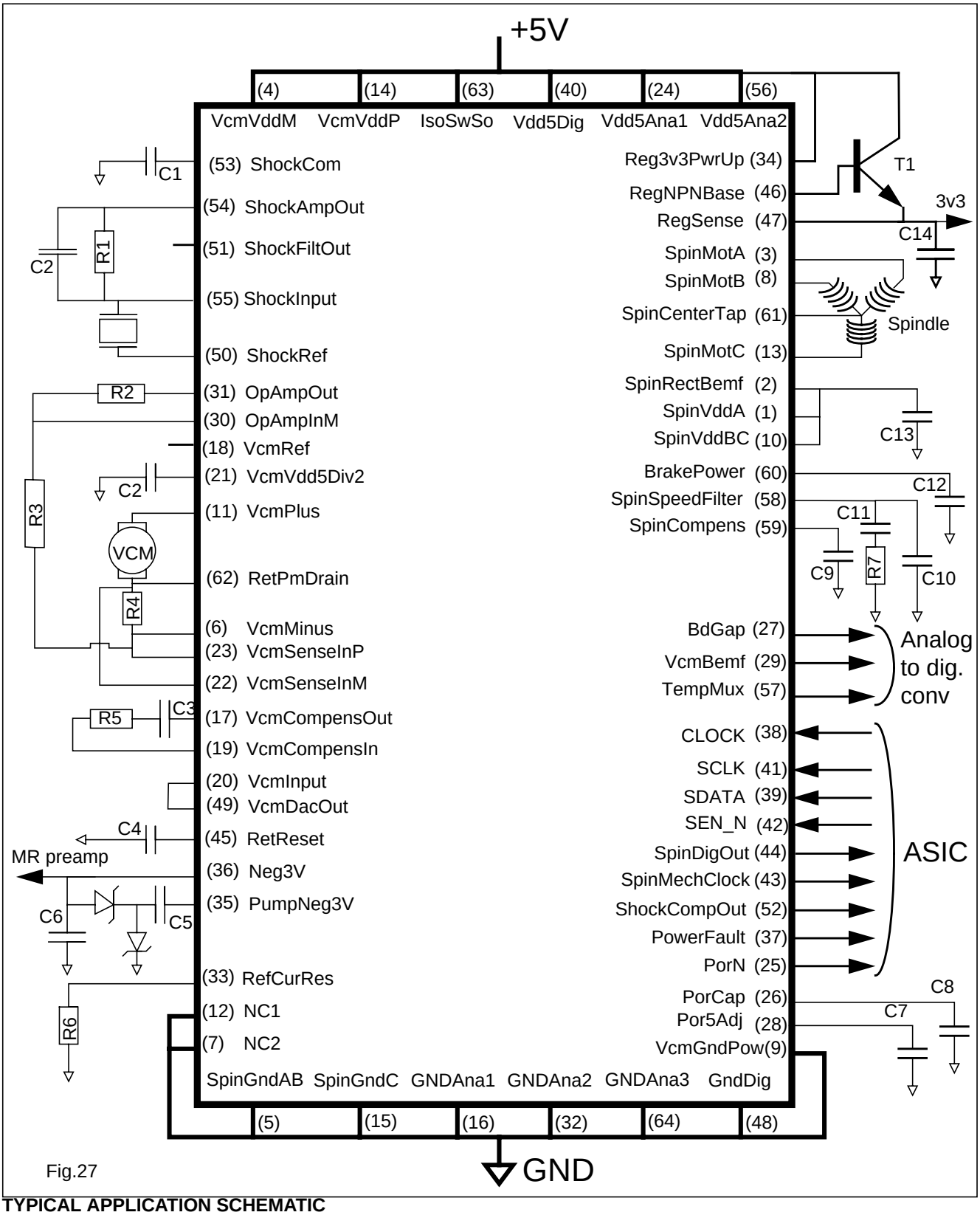

Fig.27

TYPICAL APPLICATION SCHEMATIC

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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