DATA SHEET

TDA5360
Pre–Amplifier for Hard Disk Drive with MR-Read / Inductive Write Heads

Objective specification, Revision 2.2

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Philips Semiconductors

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1 FEATURES

- 12 channels design for Single-stripe (SAL and GMR) Read / Thin-film Write heads.
- Design target 350 Mbps, for d=0 (16 / 17) rate code.
- Differential Hybrid sense Reader architecture.
- MR element biased by direct programmable constant Power or constant Current.
- Voltage driven Writer architecture.
- MR read / inductive write heads biased at ground level.
- Short rise and fall time with near rail to rail voltage swing.
- Dual power supplies : +5.0 V and -5.0 V.
- On-chip AC couplings eliminate MR head DC and DC offset voltage.
- Programmable 3-wire Serial Port Interface for programming (3.3 V and 5 V TTL / CMOS compatible).
- Extensive programmability of Write current wave overshoot.
- Programmable voltage / current mode write data input.
- Programmable voltage / current mode read data output.
- Programmable Read gain.
- Programmable Reader input impedance.
- Thermal asperity detection with programmable threshold.
- Thermal asperity compression with extensive programmability.
- High spurious-noise rejections.
- Internal Dummy Head available for MR heads protection during switchings.
- FAST mode available for short Write to Read mode transient.
- Sleep, Standby, Active, Servo Track Write, and Test modes available.
- Support servo writing.
- Write / Read Fault detection with fault code read back register and Fault masking capability.
- Low power-supplies fault protections.
- Short Write to Read Recovery, including DC settling.
- On-chip digitizing of Temperature and MR element Resistance value.
- Vendor ID and chip revision register.
- Illegal Multiple Device Selected detection.
- 2 pads CS0 and CS1, hard wired, for separate activation for multiple pre-amplifiers operation.
- Requires one external resistor.

2 APPLICATIONS

Hard Disk Drive (HDD).

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	DC Supply voltage		+4.5	+5	+5.5	V
V_{EE}			-4.5	-5	-5.5	V
NF	Noise Figure	Note 3, Section 14		1.7	1.7	dB
IRNV	Input Referred Noise Voltage	Rmr=66Ω; Imr=8mA; 10 MHz<f<100 MHz		0.8		nV/ sqrtHz
Avd	Differential gain	V_{IN}=1mVpp @ 20 MHz, $R_{Loaddif}$=330Ω, Imr=8mA, Rmr=66Ω, GAIN0=0, GAIN1=1;		50		dB
f_{HR}	-3dB frequency bandwidth	Rmr=66Ω, Lmr=30 nH -3dB: without Boost SAL GMR	 225 225			 MHz MHz
CMR	Common Mode Rejection	Imr=8 mA, Rmr=66Ω, 10MHz<f<200MHz 1 MHz<f< 10 MHz f<100 kHz, 1mV input signal		 20 40 60		 dB dB dB
PSR	Power Supply Rejection	200mVpp on Vcc or Vee, Imr=8mA, Rmr=66Ω, 10MHz<f<200MHz 1 MHz<f<10 MHz f < 100 kHz		 20 40 60		 dB dB dB
t_r, t_f	Write Current Rise/Fall times (-0.8 * Iwr => +0.8 * Iwr)	Iwr=50 mA; f=20 MHz; L_H=75nH, R_H=10Ω			0.84	ns
$I_{MR(PR)}$	Programming MR bias current range	SAL GMR (see note section 10)	4 3		10.2 6 .1	mA mA
$I_{WR(b-p)}$	Programming Write current range (base-to-peak)	Rext = 10 kΩ	10		50.3	mA
f_{sclk}	Serial interface clock rate				40	MHz

4 DESCRIPTION

The +/- 5.0 volt pre-amplifier for HDD described here has been designed for 12 terminals, comprised of a SAL or GMR magneto-resistive reader and an inductive thin film writer. In read mode, the device operates as a low noise differential preamplifier which senses resistance changes in the MR element that correspond to flux changes on the disk. In write mode, the circuit operates as a thin film head current switch, driving the inductive element of the head.

The IC incorporates Read amplifiers with programmable gain and HF boosts, Write amplifiers, 3-wires Serial Interface, Digital-to-Analog Converters, Thermal Asperity Detector and Programmable Thermal Asperity Compressor, reference and control circuits which operate on a Dual Supply Voltage of +/-5V (+/-10%).

The Read amplifier has programmable medium input impedance. The DC offset between the two terminals of the MR head is eliminated using on chip AC coupling. The bandwidth can be enhanced by using programmable high frequency gain-boost. Fast settling features are used to keep the transients short. As an option, the Read amplifier may be left biased during writing, so as to reduce the duration of these transients even further.

The Write amplifier has a programmable current overshoot which may be added to the programmable steady state write current.

Fault protection is provided for a variety of read or write unsafe conditions. For added data protection, internal pull up resistors are connected to RWN, CS0, CS1, STWN, WDP and WDN pins and pull down resistors are connected to SEN, SDATA, SCLK, DRN and BFAST pins, to prevent accidental writing due to open lines and to ensure the device will power up in a non-writing condition.

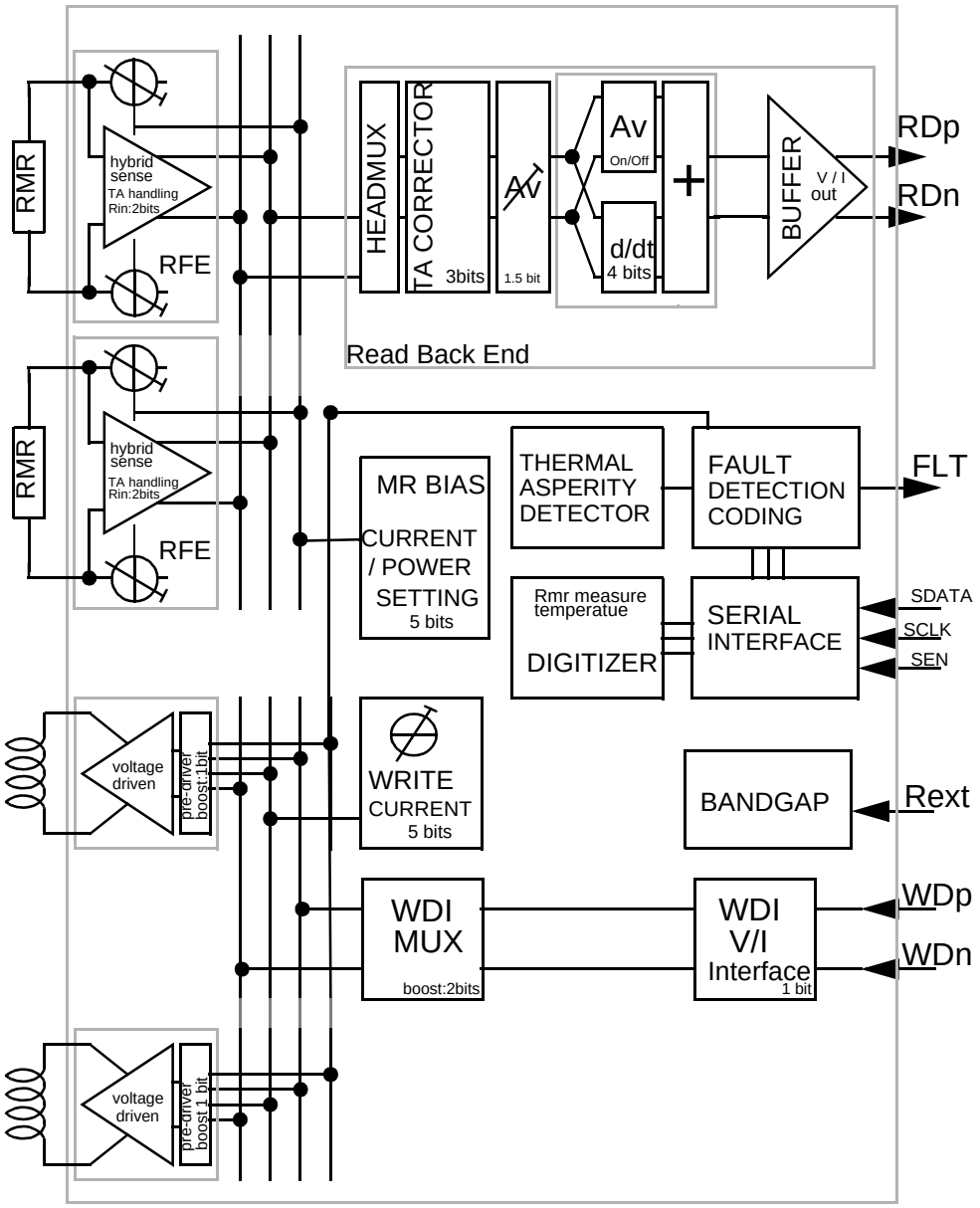
On-chip Digital to Analog converters for MR bias current or power and Write current are programmed via a 3 wire Serial Interface. Head selection, Mode control, Testing and Servo Writing can also be programmed using the serial interface. In Sleep mode, the CMOS serial interface is operationnal. Fig 2 shows the block diagram of the IC. Invalid head select codes disable the writer, select the dummy head and trigger the FLT output.

5 ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
TDA5360UH		bare die		
TDA5360UK		bumped die		

Fig.1 Type Number

6 BLOCK DIAGRAM



7 PAD ARRANGEMENT

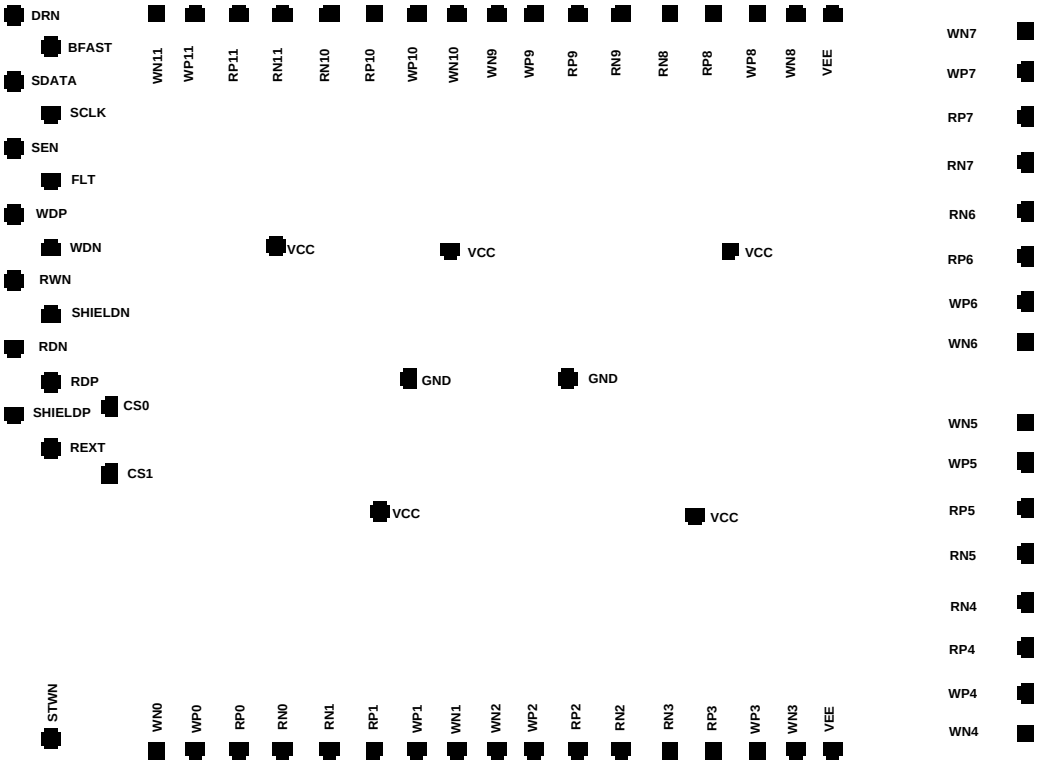


Fig.2 TDA5360 pad arrangement pads up.

8 PAD DESCRIPTION

SYMBOL	Pin	Description
VCC		+5V supply
GND		Ground
VEE		-5V supply
RDP,RDN	output	Read Data, Differential read signal outputs
RWN	logic input	Read/Write : read = HIGH, write = LOW
WDP,WDN	input	Differential PECL or current mode write data input
FLT	output input	In Write mode, a fault is flagged when FLT is high. In Read Mode, a fault is flagged when FLT is low. a 5kΩ external resistor must be connected between FLT and VCC. This pad is used as an input in MDS mode.
REXT		a 10kΩ external resistor must be connected between REXT and GND
SEN	logic input	Serial Enable line. Active High
SCLK	logic input	Serial Clock line. 40 MHz max.
SDATA	logic input/output	Serial Data line. Bi-directional interface
BFAST	logic input	Controls reader passband or enables the Imr generator depending on the state of BFCTL bit from Reg.01
DRN	logic input	Selects the dummy head or performs a system reset depending on the state of RSTDMY bit from Reg.09
RP0...RP11	input	MR head connections, positive end
RN0...RN11	input	MR head connections, negative end
WP0...WP11	output	Write head connections, positive end
WN0...WN11	output	Write head connections, negative end
STWN	logic input	Set Low for Servo Track Write mode only
CS0	logic input	Code for Chip ID
CS1	logic input	Code for Chip ID

9 FUNCTIONAL DESCRIPTION

9.1 Active READ mode

Taking RWN high and programming bits MODE0 and MODE1 (see Reg.09) selects the read mode.
The Head select inputs, in serial register, select the appropriate head.
In read mode, the circuit provides either a constant power bias or a constant current bias that flows from the P to the N side of the MR section of the head.
The value of the current/power is programmed in Reg. 02 and is referenced by the external resistor, REXT, which is connected between the REXT pin and GND. The reference voltage on REXT pin is stable over the entire operating temperature range and process.
The current or power in the MR element is constant over temperature.
The resistance of the MR element, R_{MR}, changes in the presence of a magnetic field and causes a change in the MR head voltage. The circuit acts as a low-noise differential amplifier to sense this voltage change. The read amplifier outputs, RDP and RDN, are in phase with the MRP and MRN head ports.

The read data at pins RDP, RDN can output either voltage or current, depending on how the RVORI bit in Reg.01 is set: LOW or HIGH respectively.

The polarity convention for current mode is :

“positive” => pin with least current flowing

“negative” => pin with most current flowing

Write current is not present in read mode under any circumstances; either transient or steady state.

The read path includes the following programmable features :

Gain programmation (Reg. 02 and Reg. 03) :

- gain only,
- a combination of gain plus differentiator (therefore HF-gain-boost),
- differentiator only.

The gain is programmable with step of 3dB between 44dB and 50dB.

Input impedance :

With bits RIN1, RIN0 (Reg.01), the input impedance of the readpath can be programmed from 15 to 30Ω.

Low Pole Frequency :

Bits LFP (Reg.03) allow the programmation of the Low Pole Frequency from 1 to 4 MHz.

Thermal Asperity Detection and Compression :

Thermal Asperity Detector flags an error on FLT line when a thermal disturbance is detected and load the appropriate error code in Reg. 07. The threshold is programmable via Reg. 05.

Thermal Asperity Compressor extracts the signal from the disturbance. Its thresholds levels and frequency response are also programmable with Reg.11.

9.2 Active WRITE mode

Taking RWN low from an Active READ mode selects the Active WRITE mode. The head select inputs, in a serial register, select the appropriate head.

In write mode the circuit acts as a current switch with write current toggled between the P and N directions of the thin-film section of the selected head x. The signal polarity is noninverting from WDP, WDN to WPx, WNx.

The write data at pins WDP, WDN could be driven by either a voltage or a current, according to the WVORI bit in Reg.01 (set LOW or HIGH respectively.)

The polarity convention for current mode is :

"positive" => input pin with minimum current flowing

"negative" => input pin with maximum current flowing

The writer terminal voltages are driven to GND during read mode to avoid accidental discharges to the disc.
Note that the write mode CAN NOT be selected directly from a sleep or standby condition.

The steady state value of the write current is programmed in Reg. 04 and is referenced by the external resistor, REXT, which is connected between the REXT pin and GND. The reference voltage on REXT pin is stable over the entire operating temperature range and process.

Internal compensation networks are optimized and provided to control the write current shape and settling characteristics based on specified head loads. The value can be programmed in Reg. 04.

9.3 Active STW mode

In Active Read or Active Write mode, only one head in one preamp is selected.

A special programmation of Reg. 09, using (STWN = LOW) AND (CS0 = CS1 = HIGH) allows the user to either :

- select one head per preamp (if several preamps are adressed at the same time)

- select one head in one preamp when in read mode but two heads in one preamp when going to write mode.

In that case Head x and Head (x+6) will be selected, with x=0...5. Head x is selected via Reg. 00

9.4 STANDBY mode

The standby mode is selected by programming bits MODE0 and MODE1. (see Reg.09)

The internal write current source, and MR bias current source are deactivated while RDP, RDN and FLT outputs are in a high-impedance state so that they can be OR'd in multiple preamplifiers applications. The device is specially designed for reduced dissipation in this mode. Response time from Standby to Active Read mode is much shorter than from Sleep mode to Active Read. The CMM of RDP and RDN is the same as in Sleep or Active mode. (see Note 2)

Internal fault detectors are powered off.

9.5 SLEEP mode

The sleep mode is selected by programming bits MODE0 and MODE1. (see Reg.09)

In Sleep Mode, the IC is accessible via the Serial Interface. All circuits, other than those of the CMOS Serial Interface and the circuit which forces the data registers to their default values at power up and which fixes the DC level of RDp-RDn (required when operating with more than one amplifier), are inactive. Typical static current consumption is less than one mA, depending on the state of the logic pins where internal pull-up or pull-down resistors are connected. Dynamic current consumption during operation of the Serial Interface in the Sleep mode and owing to external activity at the inputs to the Serial Interface is not included. In all Modes including the Sleep mode, data registers can be programmed. Sleep is the default Mode at power-up. Switching to other modes takes less than 0.1 ms.

The CMM of RDP and RDN is the same as in Standby or Active mode. (see Note)

Internal fault detectors are powered off.

Note 1 : At power-up, as long as DRN pin is LOW, a reset of the Serial Interface registers occurs. Before any register programmation, the user should first force DRN pin to HIGH in order to exit the reset mode and enable a register programmation. See description of DRN function in (10.6).

Note 2 : As a goal, the CMM of RDP and RDN is identical in all operating modes. The term “high-impedance” here means at least 10 to 20 kOhm from RDP or RDN to an internal CMM voltage reference.

10 BIASING OF THE MR ELEMENT

This preamplifier has been designed for SAL and GMR elements. Programming bit GMR in Reg. 01 select either a SAL range (LOW) or a GMR range (HIGH).
By programming bit PORI in Reg. 01, the user can program either a constant current bias (LOW) or a constant power bias (HIGH) for the MR element. The value of the current/power is programmed on 5 bits via Reg. 02.

If bit PORI in Reg. 01 is HIGH, a constant power bias is maintained accross the MR element.

The power is defined as :

$Pw = R_{MR} * I_{MR}^{2}$, where Pw is constant over temperature and process.

In power bias mode, two power ranges are possible :

For SAL heads	1.5mW to 9.25 mW	in steps of 0.25mW
For GMR heads	375uW to 2.3 mW	in steps of 0.0625mW

Note : whatever Power programmation is used, the I_{MR} current flowing into the MR element will be within the min-max range given below.

If bit PORI in Reg.01 is LOW, then the biasing scheme shall revert to constant current instead of constant power. I_{MR} is then constant over temperature and process.

In current bias mode, two current ranges are possible :

For SAL heads :	4 to 10.2 mA in steps of 0.2 mA
For GMR heads :	3 to 6.1 mA in steps of 0.1 mA

Note : In GMR mode, I_{MR} current is guaranted up to 5.1mA
6.1mA can be reached under certain supplies/Rmr conditions.

10.1 MR Head Resistance and Temperature Measurement

By programming RANGE0,RANGE1 bits in Reg. 08, the user can select either a Rmr measurement or a Temperature measurement (junction temperature).

Setting DIGON bit HIGH launch a digitazation
The settling time of the digitization operation is less than TBD µs.

A 5 bit code is then available in Reg. 08, as long as DIGON stays HIGH,
Setting DIGON bit LOW, reset the 5 bit code.

In case of Rmr measurement, the user have access to two Rmr range by programming RANGE0 and RANGE1 bits.

In case of Temperature too high condition (T > 140ºC), during a Temperature measurement, a Fault is triggered on FLT line and a error code is available in Reg. 07.

10.2 Fault Mode

Fault conditions are indicated on the FLT pin (HIGH during write mode and LOW during read mode). The fault condition is coded and stored in Reg. 07 for monitoring purposes. The fault code is cleared on power up, on system reset and on writing to Reg.09

The FLT output is an open collector to an external resistor of 5Kohms connected to +5V.

Table 1: Fault Conditions

Mode	Fault condition	FCOD3	FCOD2	FCOD1	FCOD0
Both	No fault	0	0	0	0
Read	Write current present	0	0	0	1
	Fault code not used	0	0	1	0
	Thermal Asperity detected	0	0	1	1
	Read head open	0	1	0	0
Write	No write current	0	1	0	1
	Write Data frequency to low	0	1	1	0
	Write head open	0	1	1	1
	Write head shorted to GND	1	0	0	0
Both	Rext open or short	1	0	0	1
	Write to read head short	1	0	1	0
	Low Vcc or Low Vee	1	0	1	1
	Fault code not used	1	1	0	0
	Illegal head address	1	1	0	1
	Fault code not used	1	1	1	0
	Temperature too high 140 C	1	1	1	1

The following are valid READ fault conditions which set FLT=LOW

- Rext pin open or shorted to GND or Vcc
- Thermal Asperity detected
- Read Head open
- Power supplies too low (VCC and/or VEE)
- Write current present in read mode
- Illegal head address (i.e. head 12, 13, 14 or 15)
  In this case, besides asserting the fault flag, the MR bias current is diverted to the dummy head.

The following are valid WRITE fault conditions which set FLT=HIGH. An action can eventually be taken :

FAULT	ACTION
• No write current in write mode	Disable write current
• Rext pin open or shorted to GND or Vcc	Disable write current
• Open write head or shorted to GND	Do not disable write current
• Write data frequency too low	Do not disable write current
• Power supplies too low	Disable write current
• Illegal head address (i.e. HD 12, 13, 14, 15)	Disable write current

If the write current is disabled, the writer is powered down. The only way to restart a write sequence is to switch R/$\overline{W}$ high and then to switch R/$\overline{W}$ low again.

Trying to go in Write mode from a sleep or standby mode condition will disable the write current.

If two fault conditions occurs nearly at the same time, the first to occur will be loaded in Reg. 07.

10.3 Serial Interface Address bit Allocation

Register	A7	A6	A5	A4	A3	A2	A1	A0
0	X	0	0	0	0	CS1	CS0	RWN
1	X	0	0	0	1	CS1	CS0	RWN
2	X	0	0	1	0	CS1	CS0	RWN
3	X	0	0	1	1	CS1	CS0	RWN
4	X	0	1	0	0	CS1	CS0	RWN
5	X	0	1	0	1	CS1	CS0	RWN
6	X	0	1	1	0	CS1	CS0	RWN
7	X	0	1	1	1	CS1	CS0	RWN
8	X	1	0	0	0	CS1	CS0	RWN
9	X	1	0	0	1	CS1	CS0	RWN
10	X	1	0	1	0	CS1	CS0	RWN
11	X	1	0	1	1	CS1	CS0	RWN

10.4 Serial Interface Register bit Allocation

Register	D7	D6	D5	D4	D3	D2	D1	D0
0	HS3	HS2	HS1	HS0	SELT	SELF	LCS1	LCS0
1	X	PORI	GMR	RIN1	RIN0	RVORI	WVORI	BFCTL
2	DUMMY	PWR4	PWR3	PWR2	PWR1	PWR0	GAIN1	GAIN0
3	HFZ3	HFZ2	HFZ1	HFZ0	X	X	LFP1	LFP0
4	IW4	IW3	IW2	IW1	IW0	WCP2	WCP1	WCP0
5	TRANGE	TAD	TAC	TAD4	TAD3	TAD2	TAD1	TAD0
6	VEND7	VEND6	VEND5	VEND4	VEND3	VEND2	VEND1	VEND0
7	X	FLT2	FLT1	FLT0	FCOD3	FCOD2	FCOD1	FCOD0
8	M4	M3	M2	M1	M0	RANGE1	RANGE0	DIGON
9	X	X	X	X	SIOLVL	RSTDMY	MODE1	MODE0
10	X	X	X	X	X	X	X	X
11	X	X	X	ENFST	TAU	TACT2	TACT1	TACT0

10.5 Serial Interface Operations

The serial interface communication consists of an adress word of 8 bits followed by a data word of 8 bits. See section 11, page 24 and 25 for timing diagrams.

10.5.1 SERIAL ADDRESSING

When SEN goes HIGH, bits are latched-in at rising edges of SCLK. The first eight bits a7-a0 starting with the LSB, are shifted serially into an address register.
If SEN goes LOW before 16 bits have been found, then the operation is ignored.

When STWn is HIGH; if a1 does not match CS0 or a2 does not match CS1, then the operation is ignored.
When STWn is LOW; if a1 and a2 are not HIGH, then the operation is ignored.
Bits a3 to a6 constitute the register address. Bit a7 is an unused one.

If (a0, a1, a2, STWn) = (0, CS0, CS1, 1)
or if (a0, a1, a2, STWn) = (0, 1, 1, 0)

then a PROGRAMMING sequence starts (see Reg. 09 description for details about preamp addressing)

If (a0, a1, a2, STWn) = (1, CS0, CS1, 1)
or if (a0, a1, a2, STWn) = (1, 1, 1, 0)

then READING data from the pre-amplifier can start. The data read back can be either 3.3V compatible or 5V compatible depending on SIOLV bit in Reg. 09.

10.5.2 PROGRAMMING DATA

During a programming sequence, the last eight bits d0-d7, before SEN goes LOW, are shifted into an input register. When SEN goes LOW, the communication sequence is ended and the data in the input register are copied in parallel to the data register corresponding to the decoded address a6-a3. SEN should go LOW at least 5ns after the last rising edge of SCLK.

10.5.3 READING DATA

Immediately after the IC detects a reading sequence, data from the data register (address a6-a3) are copied in parallel to the input register. The LSB d0 is placed on SDATA line followed by d1 at the next falling edge of SCLK, etc...
If SEN goes LOW before 8 address bits (a7-a0) have been detected, the communication is ignored. If SEN goes LOW before the 8 data bits have been sent out of the IC, the reading sequence is immediately interrupted.

SEN must stay LOW at least 75ns between two adressings.

See Timing diagramms for Serial Adressing on section 11.

10.5.4 BROADCAST MODE

When A1=A2=1 and STWN=LOW, all the preamps will be adressed whatever their CS1/CS0 setup is.
This mode allows parallel programming of any register of the serial interface, and allows STW mode programming (See Reg. 09 description).

10.6 Registers description

Nb	Register Name	Contents
0	Head Select Register	HS3..HS0 = 0,0,0,0 to 1,0,1,1 = H0 to H11 SELT : if HIGH, the multiple selection detector is enabled. Inactive in STW mode SELF : is set HIGH if illegal MDS is detected (read back only bit) (Note 0) LCS1,LCS0 : copy of CS1,CS0 pins state (read back only bits)
1	Control Register	PORI : Select a MR Bias mode. LOW = Current Bias HIGH = Power Bias GMR : select the range to be used in current or power LOW = SAL range HIGH = GMR range RIN1,0 = define the input impedance of the reader. (0,0) = 30Ω (0,1) = 23Ω (1,0) = 18Ω (1,1) = 15Ω RVORI = Reader output buffer mode. LOW = Voltage mode HIGH = Current mode WVORI = Writer data inputs mode. LOW = Voltage mode, HIGH = Current mode (Note 1a) BFCTL = Control of BFAST pin functionality (Note 1b)
2	Reader Bias Register	DUMMY : Dummy head is selected in read mode if LOW PWR4...PWR0 = define Imr current/power. Range according to GMR bit setting Rmr current bias mode : SAL : Imr = 4mA+200uA*(pwr0 + 2 * pwr1 + 4 * pwr2 + 8 * pwr3 + 16 * pwr4) GMR : Imr = 3mA+100uA*(pwr0 + 2 * pwr1 + 4 * pwr2 + 8 * pwr3 + 16 * pwr4) Rmr power bias mode : SAL : Pwr = 1.5mW+250uW*(pwr0 + 2 * pwr1 + 4 * pwr2 + 8 * pwr3 + 16 * pwr4) GMR : Pwr = 375uW+62.5uW*(pwr0 + 2 * pwr1 + 4 * pwr2 + 8 * pwr3 + 16 * pwr4) GAIN1, GAIN0 = read amplifier gain. (0,0) = 44 dB (0,1) = 47 dB (1,0) = 50 dB (1,1) = Differentiator only

3	Reader Bandwith Register	HFZ3, HFZ2, HFZ1, HFZ0 = high frequency gain boost/ differentiator control (Note 3) LFP1, LFP0 = low frequency pole. (0,0) =1 MHz (0,1) =2 MHz (1,0) =3 MHz (1,1) =4 MHz
4	Writer Bias Register	IW4, IW3, IW2, IW1, IW0 = 5 bits to define Iwr current : Iwr = 10mA + 1.3mA*(IW0+2*IW1+4*IW2+8*IW3+16*IW4) WCP2...WCP1 = 3 bits for the write current overshoot (Note 4)
5	Thermal Asperity Detection	TRANGE = if HIGH, the TA detector range is shifted up 3.17mV TAD = if HIGH, the TA detection circuits are enabled TAC = if HIGH, the TA Compression circuits are enabled TAD4..TAD0 = 5 bits for TAD threshold programmation (referred to the input) Vth(mV) = 0.390 + 3.170*TRANGE + 0.177*(TAD0 + 2*TAD1 + 4*TAD2+ 8*TAD3 + 16*TAD4) (Note 5)
6	Vendor Register	VEND7...VEND0 = 8 bits for identification (read back only bits) 7 6 5 4 3 2 1 0 0 0 1 0 0 0 1 1 = rev1 0 1 0 0 0 0 1 1 = rev2
7	Fault Management Register	FLT2...FLT0 = 3 bits to set the reporting of a fault condition : 000 = report all fault detected 001 = Disable low supply fault 010 = Disable temperature too high fault 011 = Disable write head open/short fault 100 = Disable write data frequency too low fault 101 = disable MR power too high fault 110 = Disable TA Detected fault 111 = Disable all faults FCOD3...FCOD0 = 4 bits for encoding the fault conditions (read back only bits) (Note 7)

8	Measurement Register	M4...M0 = 5 bits for Rmr/Temperature digitazation (read back only bits) RANGE1,RANGE0 = 2bits to define which measurement to be done (0,0) RMR measurement for 15Ω < Rmr < 46Ω Rmr = 698 / (15.5 + M0 + 2*M1 + 4*M2 + 8*M3 + 16*M4) (0,1) and (1,0) : RMR measurement for 40Ω < Rmr < 90Ω Rmr = 2094 / (21 + M0 + 2*M1 + 4*M2 + 8*M3 + 16*M4) (1,1) = Temperature measurement Temp = 473K - 4.6K * (M0 + 2*M1 + 4*M2 + 8*M3 + 16*M4) DIGON = is set HIGH to launch a digitazation (Note 8)
9	Operating mode Register	SIOLVL = level of SDATA when reading back a register if LOW, 3.3V compatible. if HIGH, 5.0V compatible. RSTDMY = define functionality of DRN pin (Note 9a) MODE1,MODE0 = 2 power management control bits. (0,0) Sleep Mode (0,1) Standby Mode (1,0) Active Mode or STW one head (1,1) Test Mode or STW two heads (Note 9b)
11	Thermal Asperity Compression	ENFST = when TAC is enable, this bit defines BFAST functionality (Note 11a) TAU = Low Pole Frequency time constant of the TAC LOW = 700 ns HIGH = 70 ns TACT2,TACT1,TACT0 = 3 bits to determine the TAC threshold (0,0,0) = 4.00 mV (0,0,1) = 2.97 mV (0,1,0) = 2.21 mV (0,1,1) = 1.64 mV (1,0,0) = 1.22 mV (1,0,1) = 0.91 mV (1,1,0) = 0.67 mV (1,1,1) = 0.50 mV (Note 11b)

Note 0 : MDS (Multiple Device Selected) detector :

When several preamps are connected in parallel, this function allows the user detection of wrong adressing withing the preamps.
When SELT is high, the selected preamp pull a precise current on FLT pin. If only one preamp has reacted, SELF is LOW. If more than one preamp has reacted, the voltage on FLT pin is lower than a reference voltage and thus SELF is HIGH.

Note 1a : The Write path can be controled by either a voltage or a current input signal.

The signal polarity **is non inverted** from WDP - WDN input to WPx - WNx output

Voltage mode : WDP-WDN > 0 => WPx-WNx > 0 (current flowing externally from WPx to WNx)
Current mode : current has to be pulled from WDP and WDN pins.
The positive side for signal, is the one where the least current is pulled
The negative side for signal, is the one where the most current is pulled
most current pulled from WDN => current flowing externally from WPx to WNx)

Note 1b : BFCTL define BFAST functionality :

BFCTL	BFAST	Function
LOW	LOW	I_{MR} generator ON (Reader ON) during write
LOW	HIGH	I_{MR} generator OFF (Reader OFF) during write
HIGH	LOW	Normal Reader PassBand
HIGH	HIGH	Low Frequency corner increased to 8 MHz

See ENFST bit in Reg. 11 for restrictions of BFAST functionality

Note 3 : For differentiator only (GAIN0 = GAIN1 = 1),
the midrange setting (HFZ3 = 1, HFZ0 = HFZ1 = HFZ2 = 0) have a gain of 44dB at 100 Mhz.
i.e. gain (@100 Mhz)= 80 +10 * (HFZ0 + 2*HFZ1 + 4*HFZ2 + 8*HFZ3)

For gain plus differentiator (other GAIN0, GAIN1 programmation)
the midrange setting (HFZ3=1, HFZ0,1,2=0) create a zero at 300 Mhz independent of the gain bits.
HF Zero @ f = 2400 MHz / (HFZ0 +2*HFZ1 + 4*HFZ2 +8*HFZ3)
i.e. gain = 150 + 75 * (GAIN0 + 2*GAIN1 - 5*GAIN0*GAIN1)

Note 4 : In order to increase performance for high data rate, 3 bits are available to tune the write current waveform.
WCP2 : this bit is used to add a capacitive boost during a transition of the write current.
WCP1,WCP0 : these bits are used to increase the internal swing on the write data signal.
when IW4 is HIGH (Iwr > 30.8 mA), some capacitive compensation is also activated in the write driver.

Note 5 : The threshold range of the TAD can be shifted up by 50% by setting TRANGE HIGH.
In that case the steps are still 177uV,
but the range is shifted from (0.390mV-5.877mV) to (3.560mV-9.047mV)

The relation between the threshold of the TAD programmed in Reg. 05 and the real threshold is a function of the input impedance of the reader and the low corner frequency of the reader.

Formula to link real TAD threshold with LF pole of the reader and programmed input impedance :

$$Vth = Vthprog \times \frac{0.85}{K \times \sqrt{\frac{1 + \left(\frac{fLFP}{(K \times fTA)}\right)^2}{1 + \left(\frac{fLFP}{fTA}\right)^2}}}$$

where : fLFP is the low frequency pole of the read amplifer (1 to 4 MHz, programmable via Reg. 03)
fTA is the frequency of the principal harmonic of the TA signal.

and :

$$K = \frac{RINnom}{RINnom + RMR}$$

where : RINnom is the input impedance of the reader in mid-band (programmable via Reg. 01)

For RINnom = 18Ω, RMR = 66Ω, fTA = 2MHz, Tj = 70°C, we have K = 0.214

and so, Vth(fLFP = 1MHz) = Vthprog * 1.747
Vth(fLFP = 4MHz) = Vthprog * 0.945

Note 7: FAULT code protocol.
When a fault occurs, the FAULT pin is set LOW (if read mode) or HIGH (if write mode) and a 4 bits code is available in Reg. 07 (See Section 10.2 for details).
The FAULT pin is flagged as long as the error remains present. When the error condition is removed, the FAULT pin toggles to a non-error state, but the 4 bits code still remains present in Reg. 07

To Reset the FAULT code, the user should reprogramm Reg. 09.

Some fault detections can be inhibited via FLT2,1,0 bits. If an action is linked to the inhibited detection (for example inhibiting the write current when a low power supply condition occurs), then the action is still taken, but no fault code and no FAULT pin toggling occurs.

Note 8 : R_{MR} and Temperature Digitizer
- RMR digitizer
This measurement can only be done in Read mode, with the head to be measured selected.
the Digitazation is launched when DIGON toggles from LOW to HIGH,
after a maximum of TBD us, a 5 bits code is available in Reg. 08.
The 5 bits code will only be reseted by DIGON toggling from HIGH to LOW.

- Temperature digitizer
This measurement can be done either in Active Read mode or in Active Write mode.

Note 9a : RSTDMY define DRN pin functionality

RSTDMY	DRN	Function
LOW	LOW	Serial Interface register reset
LOW	HIGH	No effect
HIGH	LOW	No effect
HIGH	HIGH	Dummy Head selected in read mode

Note 9b : MODE1,MODE0 power management control bits

A2	A1	Mode1	Mode0	STWN	
CS1	CS0	0	0	x	Sleep
CS1	CS0	0	1	x	Standby
CS1	CS0	1	0	1	Active Read or Write
1	1	1	0	0	Active STW with one head
CS1	CS0	1	1	1	Test mode
1	1	1	1	0	Active STW with 2 heads in write mode
1	1	x	x	1	Forbidden : no change in register

- Test mode is a state where both Reader and Writer are ON when R/$\overline{W}$ pin is LOW : in write mode, reader signal is present at RDP-RDN output pins.
- (A2=A1=1 and STWN=0) is a broadcast mode condition, where all the preamps will treat the data arriving on SDATA line.
- In order to get two write head selected, Head Hx should be programmed in Reg. 00 (x = 0 to 5). In that case Head Hx and Head H(x+6) will be selected in STW (Servo Track Write) 2 heads.

Note 11a : ENFST define BFAST pin functionality when Thermal Asperity Compression is ON

ENFST	BFAST functionality
LOW	inhibit BFAST control of the passband
HIGH	enable BFAST control of the passband

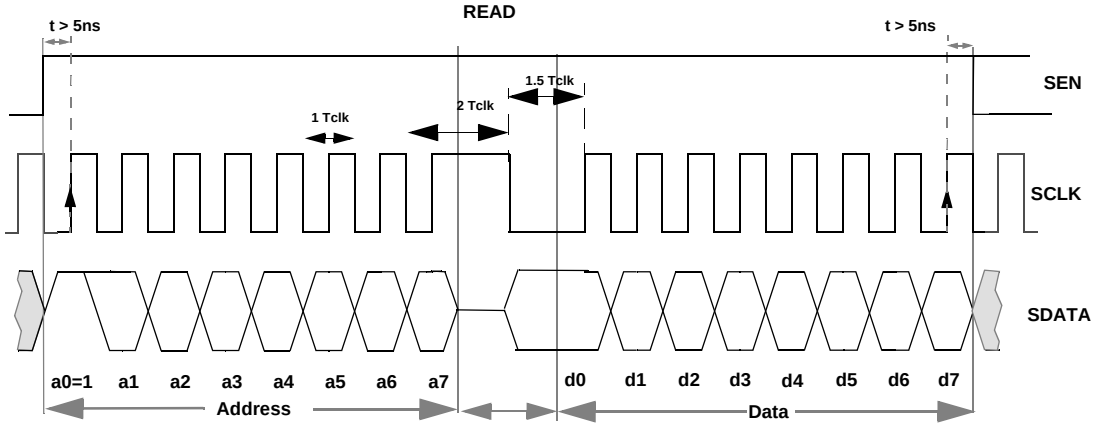
Note 11b : Thermal Asperity Compression (TAC) functionality

When a thermal asperity occurs at the reader input, the reader output signal get superposed with an amplified signal corresponding, to a certain extent, to the thermal asperity.

The aim of the TAC is to limit the amplitude and the duration of the perturbation seen at the reader output. Because thermal asperity amplitude is not constant, the TAC need some threshold programmation to define the sharpness of the response.

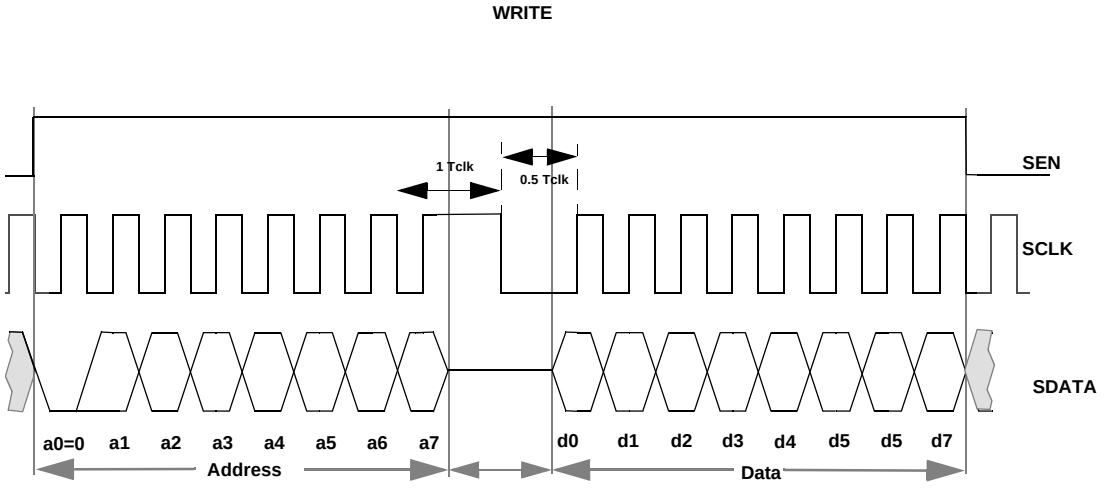
note that reducing the TAC threshold also impact the Low corner frequency value of the read amplifier.

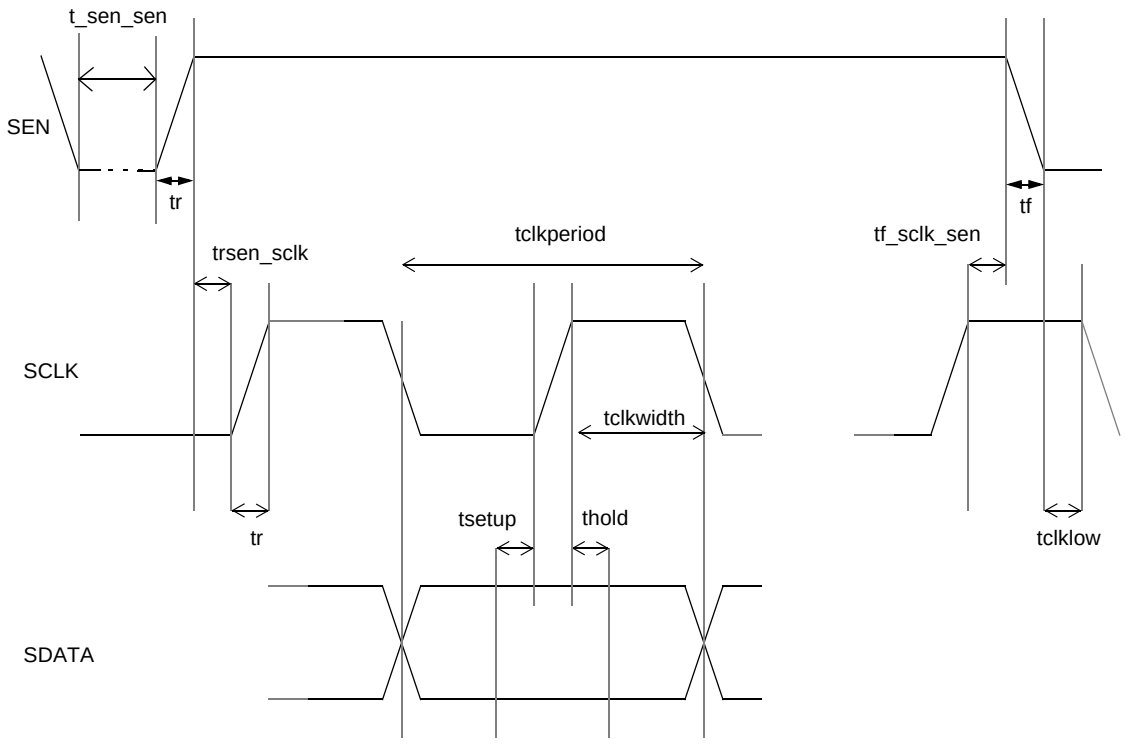
11 SERIAL INTERFACE TIMING



When Fclk > 20 MHz and a register reading is performed, it is necessary to extend the clock period as above

When Fclk < 20 MHz, this is not necessary





SEN timing	Description	Min	Nom	Max	Unit
tr_sen_sclk	90% of SEN to 10% of SCLK	5			ns
tf_sclk_sen	last SCLK to 90% of SEN	5			ns
tr,tf	rise/fall time 10%-90%		2	Tclk/4	ns
t_sen_sen	delay between 2 SEN	75			ns
SCLK timing					
frequency				40	MHz
tr , tf	rise/fall time 10%-90%		2	Tclk/4	ns
tclklow	10% of SEN to CLK state change	5(*)			ns
tclkwidth		TBD			ns
SDATA timing					
tsetup	data setup time before 10% of SCLK	5		Tclk/2	ns
thold	data hold time after 90% of SCLK	5		Tclk/2	ns

(*) either positive or negative, but ABS (tclklow) > 5ns

12 ELECTRICAL PARAMETERS

12.1 DC Characteristics

Unless otherwise specified, recommended operating conditions apply
CS0=CS1=LOW, DRN=HIGH, BFAST=LOW, STWn=HIGH, RIN=18 Ohm, LFP = 1MHz, Imr = 8mA, Rmr = 66 Ohm
Iwr = 30.8mA.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	V_{CC} Supply Current	Read Mode, I_{MR} = 8mA	65	75	85	mA
		Write Mode, I_{WR} = 30.8 mA	100	130	175	mA
		Standby Mode	200	1400	2500	uA
		Sleep Mode	200	700	2000	uA
I_{EE}	V_{EE} Supply Current	Read Mode, I_{MR} = 8mA	-20	-12	-8	mA
		Write Mode, I_{WR} = 30.8 mA	-150	-80	-60	mA
		Standby Mode	-200	-5	0	uA
		Sleep Mode	-200	-5	0	uA
Pw	Power Dissipation (T_J=105°C)	Read Mode, I_{MR} = 8mA	365	435	525	mW
		Write Mode I_{WR} = 30.8 mA	800	1050	1625	mW
V_{IL}	Input Low Voltage	TTL	0		0.8	V
V_{IH}	Input High Voltage	TTL	2.4		5	V
I_{IL}	Input Low Current V_{IL} = 0.8 V	PECL TTL	 -160		50	uA uA
I_{IH}	Input High Current V_{IH} = 2.4V	PECL TTL			50 80	uA uA
V_{OL}	Output Low voltage	SDATA I_{OL} = 4mA			0.4	V
V_{OH}	Output High voltage	SDATA 5V mode SDATA 3.3V mode	3.6 2.4		Vcc 3.6	V V
I_{OH}	Output High Current	FLT V_{OH} = 5.0V			50	uA
V_{OL}	Output Low Voltage	FLT I_{OL} = 4mA			0.4	V
	High level WDP and WDN	PECL (Note 1) Current mode (Note2)	 -0.25		Vcc 0	V mA
	Low level WDP and WDN	PECL (Note 1) Current mode (Note 2)	2.4 - 4		 -1	V mA
	|WDP-WDN| PECL swing	Voltage mode selected peak to peak (Note 1)	 0.4		 1.5	V

	Voltage compliance for WDP and WDN in current mode	CMM of the inputs in current mode	1.5		Vcc -1.7	V
V_{CCTL}	V_{CC} Fault Threshold	Hysteresis=100mV +/- 10%	3.80	4.00	4.20	V
V_{EETL}	V_{EE} Fault Threshold	Hysteresis=100mV +/- 10%	-4.20	-4.00	-3.80	V

12.2 Read Characteristics

Unless otherwise specified, recommended operating conditions apply.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{MR}	MR Current Range	SAL GMR	4 3	8	10.2 6	mA
Pwr	MR Power Range	SAL GMR (Note 3)	1.500 0.375	4.2 1	9.25 2.30	mW mW
	MR Power Tolerance	$3 < I_{MR} < 10mA$	-5		+5	%
	MR Bias Current Overshoot			0		%
	RMR Digitizer Accuracy			5		%
V_{Rext}	Rext Reference Voltage			1.31		V
A_{Vd}	Differential Voltage Gain	V_{IN} = 1mV_{PP} @ 20MHz, R_{Load}dif = 330 Ohm,I_{MR}=8mA, R_{MR} = 66 Ohm, RIN = 18 Ohm, GAIN0=0, GAIN1=1,GMR=0	48	50	52	dB
f_{HR}	Passband Upper -3dB Frequency	R_{MR} = 66Ω;L_{MR}=30nH - 3dB. Without boost.	225			MHz
f_{LR}	Passband Lower -3dB Frequency	R_{MR} = 66Ω; L_{MR} = 30nH; LPF0=0 LPF1=1			3	MHz
IRNV	Input referenced noise voltage (including MR bias current noise, excluding Rmr noise)	R_{MR} = 66Ω; I_{MR}=8mA 10 MHz<f<100 MHz, GMR=0 (Note 4)		0.8		nV/÷sqrt Hz
	MR bias current noise	I_{MR}=8mA 10 MHz<f<100MHz I_{MR}=5mA 10 MHz<f<130MHz		8 5.7		pA/sqrt÷Hz
NF	Noise figure	(Note 5)		1.7		dB
	HF noise +3dB frequency	Preamp noise=head noise		350		MHz
	LF noise +3dB frequency	Preamp noise=head noise		3		MHz

C_{IN}	Differential Input Capacitance				10	pF
R_{IN}	Differential Input Resistance	RIN0=0, RIN1=1		18		Ohm
DR	Dynamic Range	AC input where AVd falls to 90% of its value at@f = 20MHz	TBD			mV_{PP}
CMR	Common Mode Rejection	I_{MR} = 8mA, R_{MR} = 66Ω, 10 Mhz < f < 200 Mhz 1 Mhz < f < 10 Mhz f < 100 KHz, GMR=0, 1mV input signal		 20 40 60		dB
PSR	Power Supply Rejection from a signal on V_{CC}, V_{EE} or any logic pin, to R_{DP}, R_{DN}	300mV_{P-P} on V_{CC} or V_{EE}, I_{MR} = 8mA, R_{MR} =66Ω, 10 Mhz < f < 200 Mhz 1 Mhz < f < 10 Mhz f < 100 KHz, GMR=0		 20 40 60		dB
CS	Channel Separation	Unselected Channels: V_{IN} = 1mV_{PP} 1 < f < 200 MHz	50			dB
V_{OS}	Output Offset Voltage	IMR=8mA, RMR=66Ω, GAIN0=GAIN1=0, GMR=0			100	mV
V_{OCM}	Common Mode Output Voltage			2.45		V
R_{SEO}	Single-Ended Output Resistance			17.5		Ohm
I_O	Output Current	AC Coupled Load, RDP to RDN RVORI = HIGH RVORI = LOW	 TBD 4			 mA
	MR head potential	From any point to GND	-500		+500	mV
THD	Total Harmonic Distortion	First 10 harmonics			0.5	%
I_{DISK}	MR Head-to-Disc Contact Current	Extended contact Maximum Peak Discharge for <20ns C_{DISK}=300pF,R_{DISK} =10MΩ			100 20	uA mA
DV_{OCM}	Common Mode Output Voltage Change	V_{OCM} (READ) - V_{OCM} (WRITE)			100	mV
	TA Detection Response Time	TA occurred to FLT active		20	40	nS

12.3 Write Charateristics

Unless otherwise specified, recommended operating conditions apply,

I_W=50mA, L_H=75nH, R_H = 10Ω, f_{DATA}=5MHz, Ambient temperature.

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
I_{WR}	Write Current Range		10	30.8	50.3	mA_{PK}
$\Delta I_{WR} / I_{WR}$	Write Current Tolerance		-7		7	%
	Differential Head Voltage Swing	Iwr = 50mA	TBD	16		V_{PP}
I_{UH}	Unselected Head Current Glitch	I_W = 50mA			1	mA_{PK}
f_{DATA}	Write Data Frequency for Safe Condition	FLT = Low	1			MHz
R_O	Differential Output Resistance			30	60	Ohm
C_O	Differential Output Capacitance				6	pF
A_{SYM}	Asymmetry (A_{SYM} = |tr-tf|)	Write Data has 50% duty cycle & 0.5ns rise/fall time, load=short			0.1	ns
t_r , t_f	Rise/Fall Time (-0.8 * I_{WR} => +0.8 * I_{WR})	10-90%; I_W = 50mA L_H=75nH, R_H=10Ω			0.84	ns
T_{WSET}	Write Current Settling Time	I_{WR} = 50mA, L_H=75nH, R_H=10Ω			2.5	ns
W_{COV}	Write Current Overshoot	I_W = 50mA, L_H = 75 nH, R_H = 10Ω WCP0,1,2 = 000		20		%

12.4 Switching Characteristics

Unless otherwise specified, recommended operating conditions apply

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SI	Serial Interface timing	(Note 6)				
t_{RW}	R/WN to Write Mode	To 90% of write current			50	ns
	SEN to Write Mode	To 90% of write current			50	ns
t_{WR}	R/WN to Read Mode	Reader outputs loaded with high-pass single ended filters : R=165Ω, C=270pF Writer output shorted (Note 7)		175		ns
t_{CS}	CS to Read Mode	Reader outputs loaded with high-pass single ended filters : R=165Ω, C=270pF			1	us
t_{HS}	Head Switching	Reader outputs loaded with high-pass single ended filters : R=165Ω, C=270pF			1	us
t_{RI}	CS to Unselect	To 10% write current			50	ns
t_{D1}	Safe to Unsafe	50% WDP to 50% FLT when a low frequency condition occurs.			1	us
t_{D2}	Unsafe to Safe	50% WDP to 50% FLT		20		ns
t_{D3}	Head Current Propagation Delay	From 50% of WDP to 50% of write current, load=short			5	ns
T_{RSET}	MR Bias Current Settling Time	I_{MR} = 8mA, R_{MR} =66Ω (Note 8)			1	us

Notes:

1. The differential peak to peak voltage swing could be from 0.4V to 1.5V and the common mode should be such that for any of the two states the maximum High shall be less than Vcc and the minimum LOW shall be more than 2.4V.
2. In current mode, a ratio of at least 5 sould exist between the HIGH and LOW level currents.
3. Whatever constant power is programmed, the value of the Imr current can not exceed the limits given in the constant current mode.
4. The input referred noise voltage, excluding the noise of the MR resistor iis defined as follows :

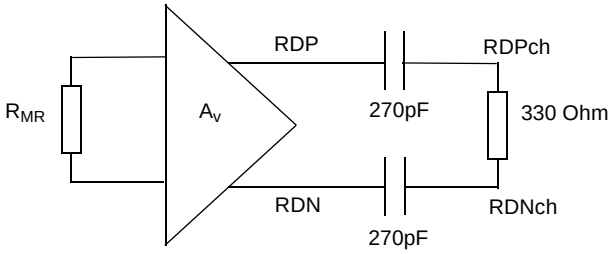
$$vn^2 = \left(\frac{vnout}{Av}\right)^2 - 4 \times k \times T \times RMR$$

5. The noise figure is defined as :

$$NF[dB] = 10xlog[(Vnout/Av)^2 / (4kTxR_{MR})]$$

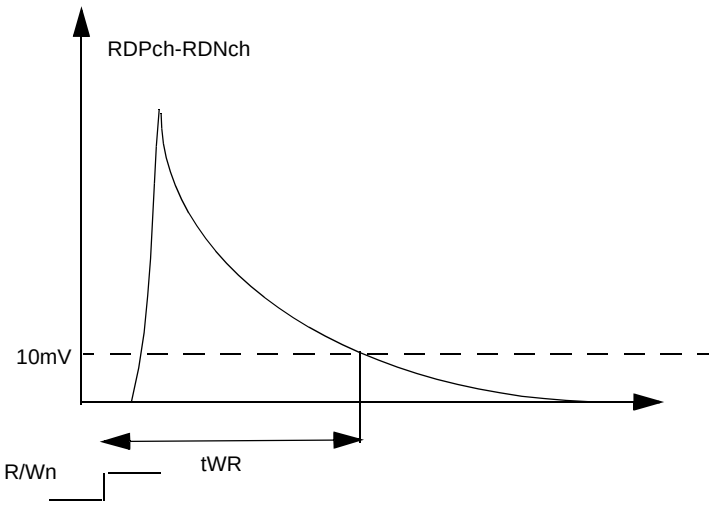
where Av is the gain and Vnout is the noise voltage at the output of the amplifier

6. See Section 11 for Serial Interface timing diagrams
7. This tWR is defined for a specific load on RDP,RDN reader outputs :



tWR is the time between R/Wn going HIGH and the time when :

90% of the signal envelop is present at RDPch-RDNch
AND the differential DC decaying at RDPch-RDNch is below 10mV :



Changing the load of the preamp will change tWR according to the new RC time constant.

8. When changing MR bias current, from SEN to 90% of I_{MR} bias current.

13 LIMITING VALUES / RECOMMENDED OPERATION CONDITIONS

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP	MAX.	UNIT
V_{CC}	Positive Supply voltage range	note1	4.5	5.0	5.5	V
V_{EE}	Negative Supply voltage range	note 2	-4.5	- 5.0	-5.5	V
V_{IH}	High level CMOS input voltage		2.4		V_{CC}	V
V_{IL}	Low level CMOS input voltage		0		0.8	V
$V_{i(dif)(p-p)}$	Differential Peak to Peak input voltage		0.4	0.7	1.5	V
(Writer input)	High level PECL input voltage			3.2	V_{CC}	V
	Low level PECL input voltage		2.4	2.8		V
Imode	Differential Peak to Peak input current		0.4	0.8	1.0	mA
(Writer input)	High level input current		-1.4	-1.2		mA
	Low level input current			-0.4	-0.1	mA
T_{amb}	Ambient temperature		0	55	70	°C
T_j	Junction temperature	when reading		70	110	°C
		when writing			130	
R_{MR}	MR element resistance		46	66	86	Ohm
$L_{l(tot)}$	Total lead inductance to the head	in each lead	-	17		nH
$R_{l(tot)}$	Total lead resistance to the head	in each lead	-	1.5		Ohm
V_{MR}	Voltage accross MR element (RPx-RNx)				1	V
$V_{sig(dif)(p-p)}$	MR head input signal peak to peak voltage	differential	0.4	1	3	mVpp
L_{wh}	Write Head inductance	including lead		75		nH
R_{wh}	Write Head resistance	including lead	-	10		Ohm
C_{wh}	Write head capacitance	including lead	-	TBD		pF
R_{ext}	Reference resistor	Iref=Vref/Rext	9.9	10	10.1	k Ω

Notes

1. A supply by-pass capacitor from V_{CC} to ground or a low pass filter may be used to optimize the PSRR.
2. A supply by-pass capacitor from V_{EE} to ground or a low pass filter may be used to optimize the PSRR

14 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	Positive supply voltage	-0.5	6.0	V
V_{EE}	Negative supply voltage	-6.0	0.5	V
V_{IN}	Digital input voltage	-0.5	V_{CC}+0.3V	V
V_{n1}	Voltage on all pins except V_{CC}, read inputs RPx, RNx, write outputs WPx, WNx (x=0 to 11) and the ones mentionned in this table	-0.5	5.5	V
	but not higher than		V_{CC}+0.5	V
V_{n2}	Voltage on write driver outputs WPx, WNx	V_{EE}	V_{CC}	V
	but not larger than	V_{EE}-0.5	V_{CC}+0.5	V
V_{n3}	Read inputs RPx, RNx	-1	1	V
T_{stg}	IC Storage temperature range	-65	150	°C
T_j	Junction temperature range		150	°C

Pre-Amplifier for Hard Disk Drive with MR-Read / Inductive Write Heads

TDA5360

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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