INTEGRATED CIRCUITS

DATA SHEET

TDA6120Q
Video output amplifier

Preliminary specification
Supersedes data of 1997 Jul 17
File under Integrated Circuits, IC02

1997 Aug 27

Philips
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FEATURES

- High large signal bandwidth of 32 MHz (typ.) at 125 V (p-p)
- High small signal bandwidth of 47 MHz (typ.) at 60 V (p-p)
- Rise/fall time of 12.5 ns for 125 V (p-p)
- High slew rate of 10 V/ns
- Low static power dissipation of 2.5 W at 200 V supply voltage
- High maximum output voltage
- Bandwidth independent of voltage gain
- Maximum overall voltage gain over 46 dB
- High Power Supply Rejection Ratio (PSRR)
- Fast cathode current measurement output for dark current control loop
- Differential voltage input.

GENERAL DESCRIPTION

The TDA6120Q is a single 30 MHz, 125 V (p-p) video output amplifier contained in a plastic DIL-bent-SIL power package. The device uses high-voltage DMOS technology and is intended to drive the cathodes of a CRT in High Definition TVs (HDTVs) or monitors.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6120Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm)	SOT141-8

BLOCK DIAGRAM

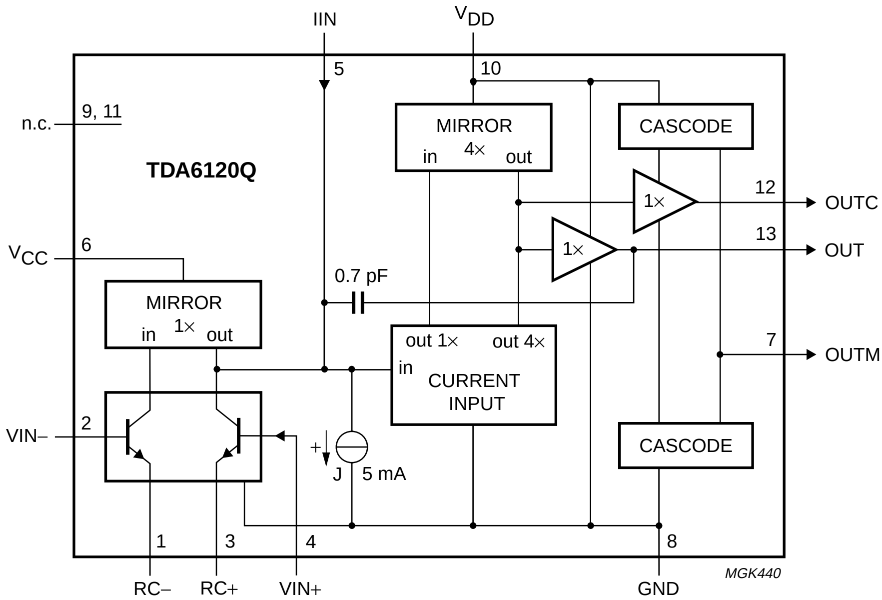


Fig.1 Block diagram.

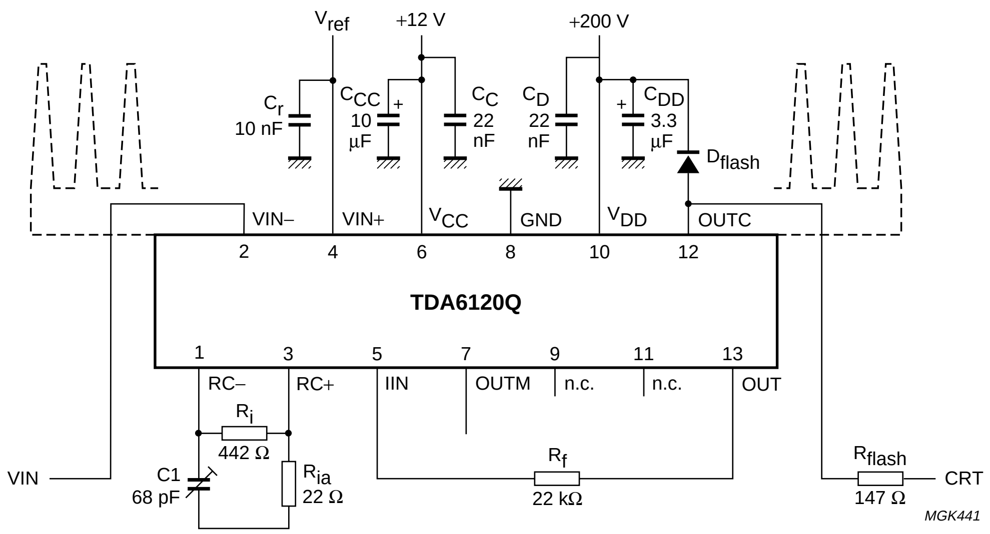


Fig.2 Top view.

PINNING

SYMBOL	PIN	DESCRIPTION
RC–	1	inverting input pre-emphasis network
VIN–	2	inverting voltage input
RC+	3	non-inverting input pre-emphasis network
VIN+	4	non-inverting voltage input
IIN	5	feedback current input
V_{CC}	6	low supply voltage (12 V)
OUTM	7	cathode current measurement output
GND	8	power ground and heatsink
n.c.	9	not connected
V_{DD}	10	high supply voltage (200 V)
n.c.	11	not connected
OUTC	12	cathode output
OUT	13	feedback output

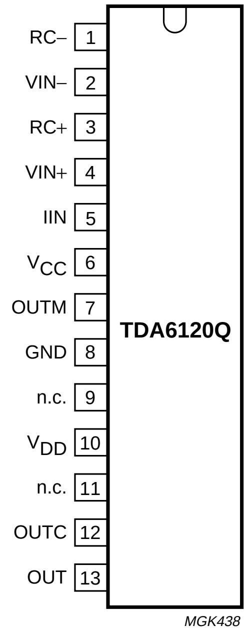


Fig.3 Pin configuration.

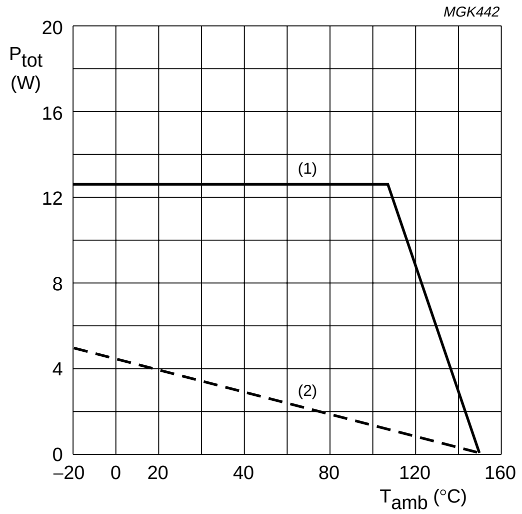
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	high supply voltage		0	280	V
V_{CC}	low supply voltage		0	20	V
V_i	input voltage (pins 2 and 4)		0	V_{CC}	V
$V_{i(dif)}$	differential mode input voltage (pins 2 and 4)		$-V_{CC}$	V_{CC}	V
$V_{i(pe)}$	pre-emphasis input voltage (pins 1 and 3)		0	V_{CC}	V
$V_{i(dif)(pe)}$	differential mode pre-emphasis input voltage (pins 1 and 3)		$-V_{CC}$	V_{CC}	V
V_{IIN}	input voltage (pin 5)		0	$2V_{BE}$	V
V_{OUTM}	measurement output voltage		0	20	V
V_o	output voltage (pins 12 and 13)		0	V_{DD}	V
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+150	°C
V_{ESD}	voltage peak human body model	note 1	–	2000	V
	voltage peak machine model		–	300	V

Note

1. 1250 V for IIN (pin 5).



(1) Infinite heatsink.
(2) No heatsink.

Fig.4 Power derating curve.

QUALITY SPECIFICATION

Quality specification in accordance with *“SNW-FQ-611 part E”*.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case	3.0	K/W

CHARACTERISTICS

Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V; V_{CC} = 10.8 to 13.2 V; V_{OUTM} = 4 to 20 V; V_{VIN-} = 1.5 to 5 V; V_{VIN+} = 1.5 to 5 V.

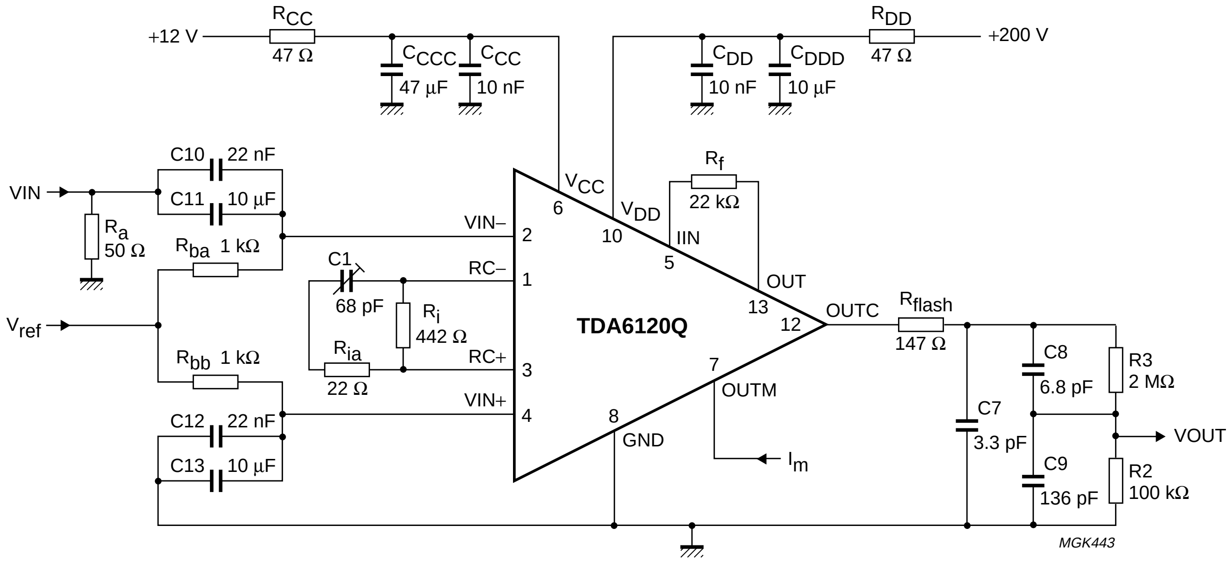
Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V; V_{CC} = 12 V; V_{VIN+} = 3 V; V_{OUTM} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\ h}$ = 4 K/W; test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(q)}$	quiescent high voltage supply current	V_{OUTC} = 100 V	8	10	12	mA
$I_{CC(q)}$	quiescent low voltage supply current	$V_{VIN-} = V_{VIN+}$	25	31	39	mA
I_{bias}	input bias current (pins 2 and 4)	V_{OUTC} = 100 V	–	30	–	μA
V_{OUTC}	DC output voltage (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	70	100	130	V
$\Delta V_{OUTC(T)}$	DC output voltage temperature drift (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	–	–	5	V
$I_{(offset)OUTM}$	offset current of measurement output	note 1	–40	+20	+120	μA
$\Delta I_{OUTM}/\Delta I_{OUTC}$	linearity of current transfer	–50 μA < I_{OUTC} < +50 μA; note 1	–	1.0	–	
C_i	input capacitance (pins 2 and 4)	$V_{OUTC} = V_{OUTC(max)}$	–	3	–	pF
$I_{OUTC(max)}$	maximum dynamic peak output current (pin 12)	20 V < V_{OUTC} < V_{DD} – 20 V	–	100	–	mA
$V_{OUTC(min)}$	minimum output voltage (pin 12)		–	4	10	V
$V_{OUTC(max)}$	maximum output voltage (pin 12)		V_{DD} – 10	V_{DD} – 6	–	V
G_{int}	internal gain		1.68	1.87	2.08	
B_s	small signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 60 V (p-p); $V_{OUTC(DC)}$ = 100 V	40	47	–	MHz
B_l	large signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V	28	32	–	MHz
t_{pd}	cathode output propagation time 50% input to 50% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	10	–	15	ns
$t_{o(r)}$	cathode output rise time 10% output to 90% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.6	10	14	18	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{o(f)}$	cathode output fall time 90% output to 10% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.7	10	12.5	15	ns
t_{st}	settling time 50% input to (99% < output < 101%) (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	–	250	ns
SR_r	slew rate rise between 30 V to (V_{DD} – 30 V) (pin 12)	V_{VIN-} = 2 V (p-p) square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns	–	8	–	V/ns
SR_f	slew rate fall between (V_{DD} – 30 V) to 30 V (pin 12)	V_{VIN-} = 2 V (p-p) square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns;	–	10	–	V/ns
O_{Vr}	cathode output voltage overshoot rise (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	5	–	%
O_{Vf}	cathode output voltage overshoot fall (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	20	–	%
PSRRh	high voltage power supply rejection ratio	f < 50 kHz; note 2	–	44	–	dB
PSRRl	low voltage power supply rejection ratio	f < 50 kHz; note 2	–	48	–	dB

Notes

1. The operating range of the measurement output OUTM is 4 to 20 V. Below 4 V, OUTM acts as a voltage source with an output resistance such that the maximum current input from OUTM is 2 mA.
   a) The linearity of the current transfer is guaranteed until a junction temperature of 125 °C.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.



$$\text{Overall gain} = G_{int} \times \frac{R_f}{R_i}$$

Fig.5 Test circuit with gain of 40 dB.

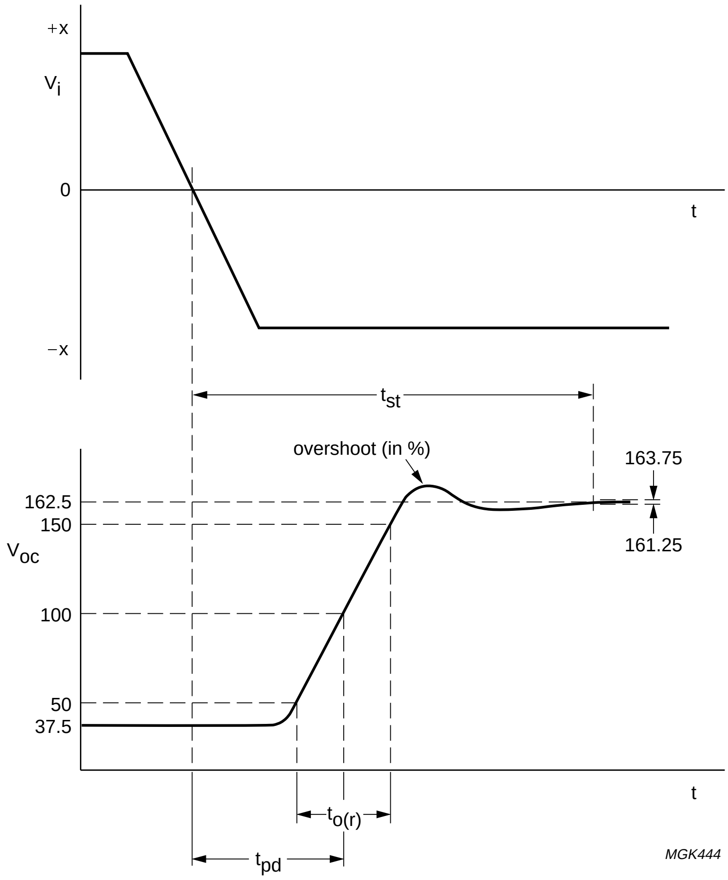


Fig.6 Output (pins 12 and 13; rising edge) as a function of input signal.

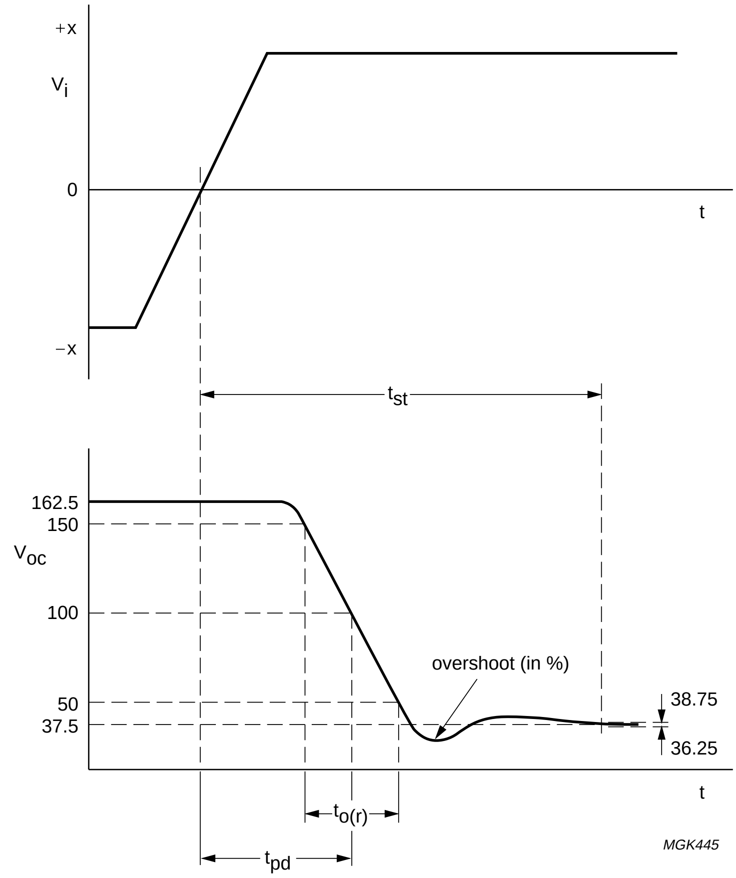


Fig.7 Output (pins 12 and 13; falling edge) as a function of input signal.

FLASHOVER PROTECTION

The TDA6120Q does NOT include protection diodes that clamp the cathode output pin to the high voltage supply pin during a CRT flashover discharge. Therefore an external high voltage reverse biased diode has to be connected between the OUTC pin and the V_{DD} pin. An external 147 Ω carbon high-voltage resistor in combination with a 2 kV spark gap between the cathode and ground will limit the maximum clamp current (for this resistor value, the CRT has to be connected to the main printed-circuit board).

This external network causes an increase in the rise and fall times and a decrease in the overshoot.

Pin 10 must be decoupled to pin 8:

- By a capacitor >22 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pin 10 and pin 8; definitely within 5 mm.
- By a capacitor >3.3 µF on the picture tube base printed circuit board (common for three output stages).

TEST AND APPLICATION INFORMATION

Dissipation

Regarding dissipation, distinction must be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency). The static dissipation of the TDA6120Q is due to supply currents, and currents in the feedback network and CRT.

The static dissipation is given by the following equation:

$$P_{stat} = V_{CC} \times I_{CC} + V_{DD} \times I_{DD} - V_{OUTC} \times \frac{V_{OUTC}}{R_f - I_{OUTC}}$$

Where:

R_f = feedback resistance

I_{OUTC} = DC cathode current.

The dynamic dissipation is given by the following equation:

$$P_{dyn} = V_{DD} \times (C_L + C_{int}) \times f \times V_{OUTC(p-p)} \times b$$

Where:

C_L = load capacitance

C_{int} = effective internal load capacitance (approximately 7 pF)

f = frequency

$V_{OUTC(p\text{-}p)}$ = output voltage (peak-to-peak value)

b = non-blanking duty cycle (0.8).

The IC must be mounted on the picture tube base printed-circuit board to minimize the load capacitance C_L.

Switch-off

The voltage at output pins OUT and OUTC will be pulled to ground when the low voltage supply voltage (V_{CC}) is switched off.

INTERNAL PIN CONFIGURATION

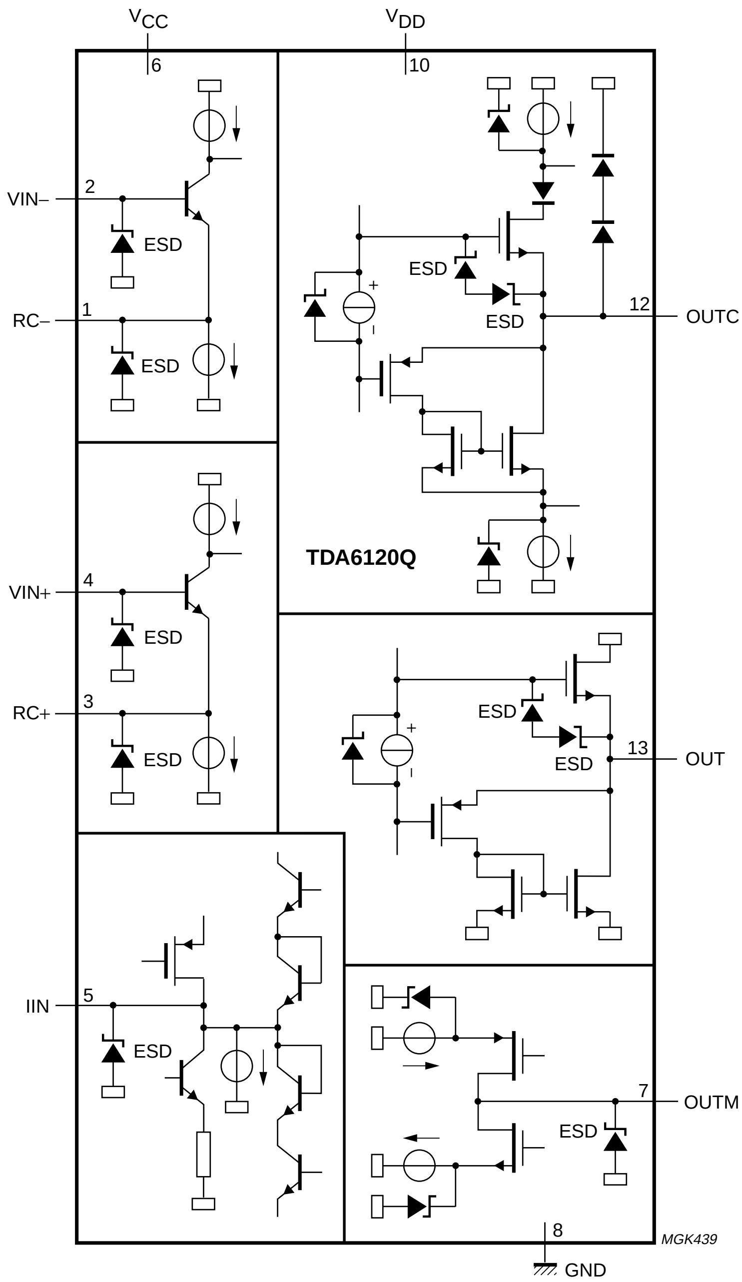
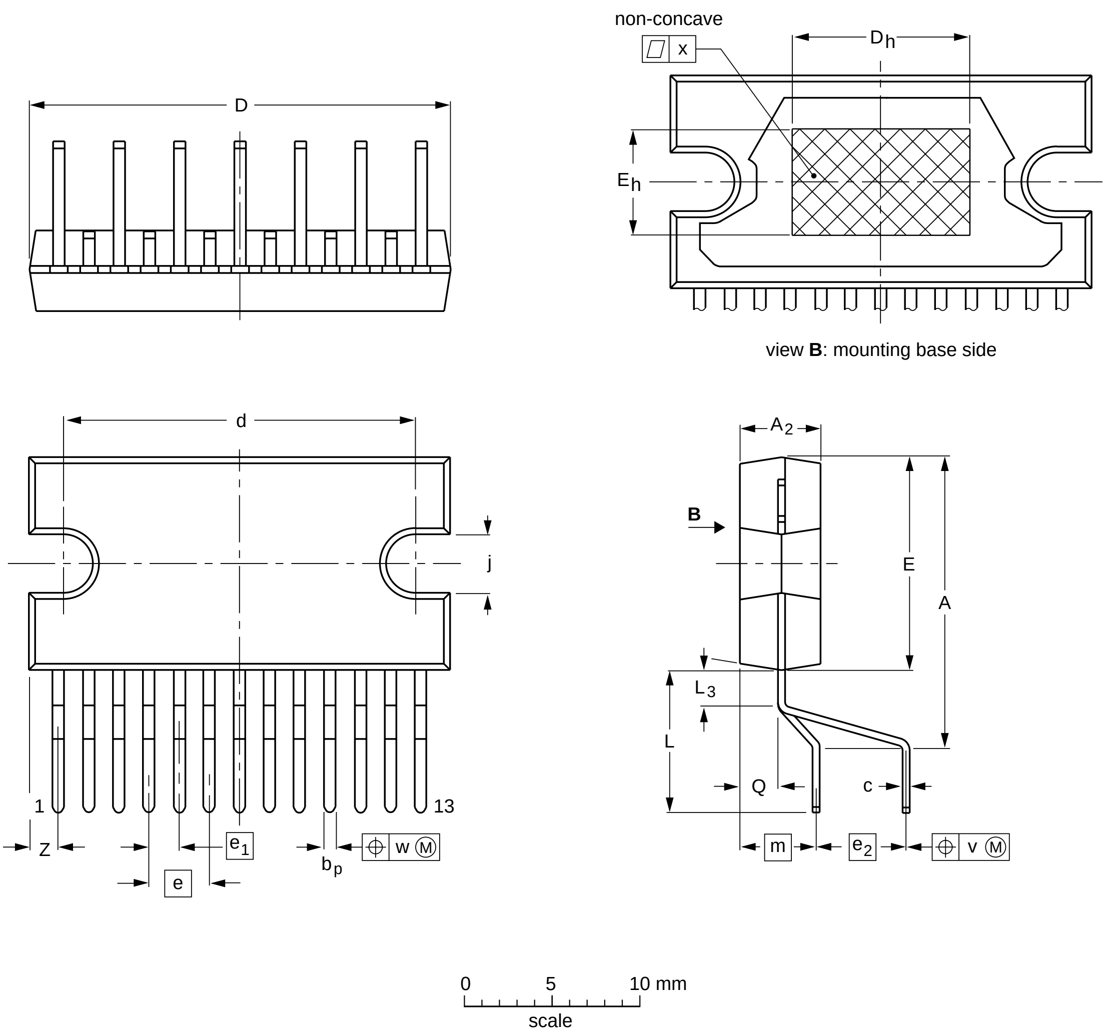


Fig.8 Internal pin diagram.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm) **SOT141-8**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-8						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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