DATA SHEET

TDA6502; TDA6502A; TDA6503; TDA6503A

5 V mixers/oscillators and synthesizers for cable TV and VCR 2-band tuners

Preliminary specification
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CONTENTS

1 FEATURES

- Single-chip 5 V mixer/oscillator and synthesizer for cable TV and VCR tuners
- Pin-to-pin compatible with TDA6402, TDA6402A, TDA6403 and TDA6403A
- Universal bus protocol (I^2C-bus or 3-wire bus)
  - Bus protocol for 18 or 19-bit transmission (3-wire bus)
  - Extra protocol for 27-bit transmission (test modes and features for 3-wire bus)
  - Address + 4 data bytes transmission (I^2C-bus 'write' mode)
  - Address + 1 status byte (I^2C-bus 'read' mode)
  - 4 independent I^2C-bus addresses.
- 1 PMOS buffer for UHF band selection (25 mA)
- 3 PMOS buffers for general purpose, e.g. 2 VHF sub-bands, FM sound trap (25 mA)
- 33 V tuning voltage output
- In-lock detector
- 5-step analog-to-digital converter (3 bits in I^2C-bus mode)
- 15-bit programmable divider
- Programmable reference divider ratio (64, 80 or 128)
- Programmable charge pump current (60 or 280 μA)
- Varicap drive disable
- Balanced mixer with a common emitter input for VHF (single input)
- Balanced mixer with a common base input for UHF (balanced input)
- 2-pin common emitter oscillator for VHF
- 4-pin common emitter oscillator for UHF
- IF preamplifier with asymmetrical 75 Ω output impedance able to drive loads from 75 Ω upwards
- Low power
- Low radiation
- Small size
- The TDA6502A and TDA6503A differ from the TDA6502 and TDA6503 by the UHF port protocol in the I^2C-bus mode (see Tables 3 and 4).

2 APPLICATIONS

- Cable tuners for TV and VCR (switched concept for VHF).

3 GENERAL DESCRIPTION

The TDA6502, TDA6502A, TDA6503 and TDA6503A are programmable 2-band mixers/oscillators and synthesizers intended for VHF/UHF TV and VCR tuners (see Fig.1).

Partitioning of the bands is the responsibility of the customer providing VHF is below 500 MHz and UHF is below 900 MHz.

The devices include two double balanced mixers and two oscillators for the VHF and UHF band respectively, an IF amplifier and a PLL synthesizer. The VHF band can be split-up into two sub-bands using a proper oscillator application and a switchable inductor.

Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling.

The port register provides four PMOS ports. Band selection is provided by port register UHF. When port register UHF is 'on', the UHF mixer-oscillator is active and the VHF band is switched off. When port register UHF is 'off', the VHF mixer-oscillator is active and the UHF band is off. Port registers VHFL and VHFH are used to select the VHF sub-bands. Port register FMST is a general purpose port, that can be used to switch an FM sound trap. When the ports are used, the sum of the drain currents has to be limited to 30 mA.

The synthesizer consists of a 15-bit programmable divider, a crystal oscillator and its programmable reference divider and a phase comparator (phase/frequency detector) combined with a charge pump which drives the tuning amplifier, including the 33 V output at pin VT. Depending on the reference divider ratio (64, 80 or 128), the phase comparator operates at 62.5, 50 or 31.25 kHz with a 4 MHz crystal.

Depending on the voltage applied to pin SW (see Table 2) the device is operating in the I²C-bus mode or 3-wire bus mode.

In the 3-wire bus mode, pin LOCK/ADC is the 'lock' output of the PLL and is at LOW level when the PLL is locked. Lock detector bit FL of the status byte is set to logic 1 when the loop is locked and is read on the SDA line during a READ operation in I²C-bus mode only.

In the I²C-bus mode only, pin LOCK/ADC is the ADC input for digital AFC control. The ADC code is read during a READ operation on the I²C-bus.

In the test mode, in both I²C-bus mode and 3-wire bus mode, pin LOCK/ADC is used as a test output for f_{REF} and $\frac{1}{2}f_{DIV}$.

3.1 I²C-bus format

Five serial bytes (including the address byte) are required to address the device, select the VCO frequency, program the four ports, set the charge pump current and set the reference divider ratio. The device has four independent I²C-bus addresses which can be selected by applying a specific voltage to pin CE/AS.

3.2 3-wire bus format

Data is transmitted to the device during a HIGH level on pin CE/AS (enable line). The device is accessible with 18-bit and 19-bit data formats (see Figs 4 and 5). The first four bits are used to program the PMOS ports and the remaining bits control the programmable divider. A 27-bit data format (see Fig.6) may also be used to set the charge pump current, the reference divider ratio and the test modes.

It is not allowed to address the device with words whose length is different from 18, 19 or 27 bits.

Table 1 Data word length for 3-wire bus format

DATA WORD	REFERENCE DIVIDER(1)	FREQUENCY STEP
18-bit	64	62.50 kHz
19-bit	128	31.25 kHz
27-bit	programmable	programmable

Note

1. The selection of the reference divider is given by an automatic identification of the data word length. When the 27-bit format is used, the reference divider is controlled by bits RSA and RSB (see Table 8). More details are given in Section 8.3.

4 QUICK REFERENCE DATA

Measured over full voltage and temperature ranges.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	operating	4.5	5	5.5	V
I_{CC}	supply current	all PMOS ports are off; V_{CC} = 5V	–	71	–	mA
f_{XTAL}	crystal oscillator frequency		–	4.0	–	MHz
$I_{o(PMOS)}$	PMOS port output current	note 1	–	–	30	mA
P_{tot}	total power dissipation	note 2	–	–	520	mW
T_{stg}	IC storage temperature		–40	–	+150	°C
T_{amb}	ambient temperature		–20	–	+85	°C
f_{RF}	RF frequency	VHF band	40	–	800	MHz
		UHF band	200	–	900	MHz
G_V	voltage gain	VHF band	–	20	–	dB
		UHF band	–	32	–	dB
NF	noise figure	VHF band	–	7.5	–	dB
		UHF band	–	7	–	dB
V_o	output voltage (causing 1% cross modulation in channel)	VHF band	–	110	–	dBµV
		UHF band	–	110	–	dBµV

Notes

1. One buffer ‘on’, I_o = 25 mA; two buffers ‘on’, maximum sum of I_o = 30 mA.
2. The power dissipation is calculated as follows:

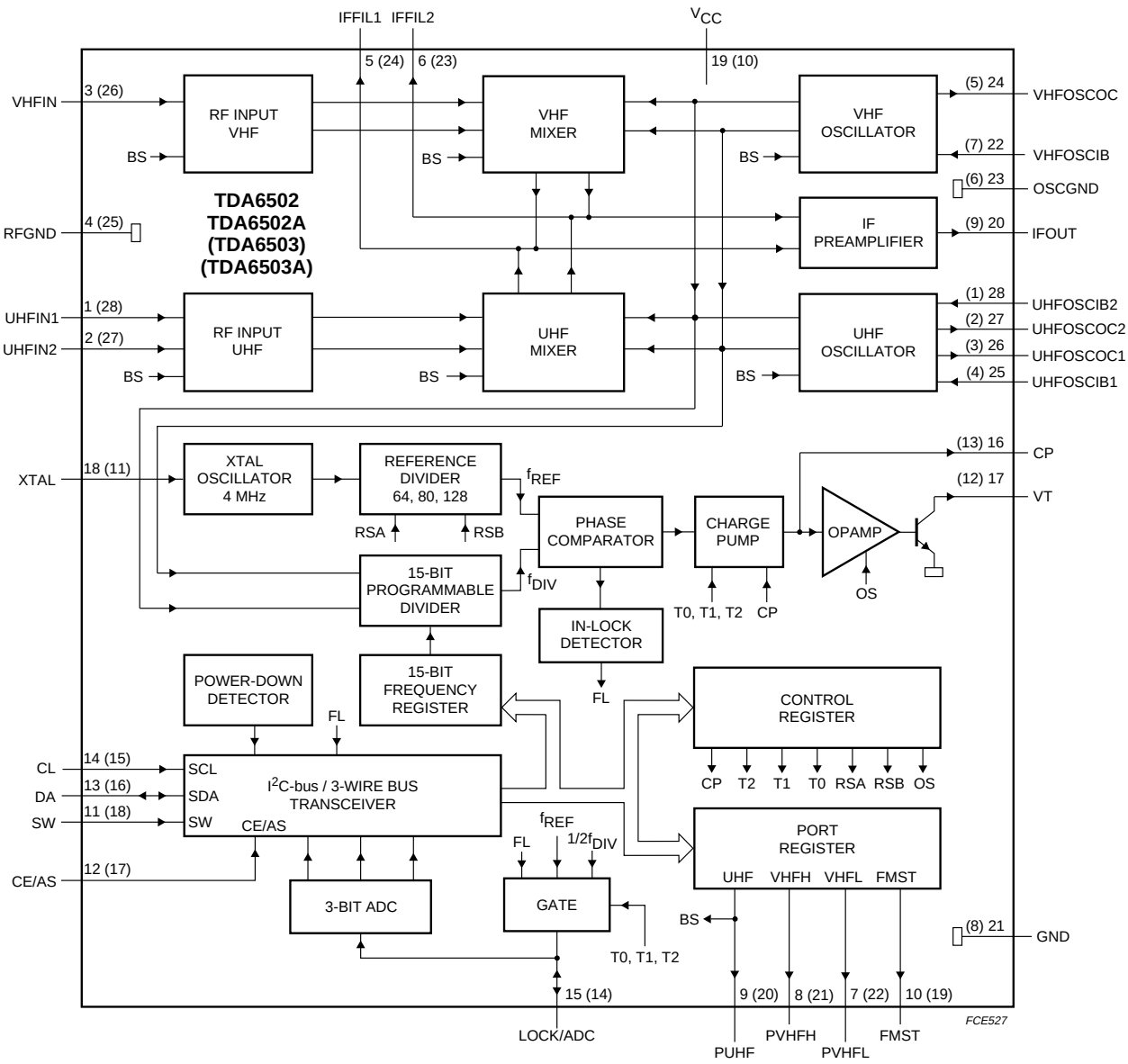
$$P_{tot} = V_{CC} \times (I_{CC} - I_o) + V_{P(sat)} \times I_o + \frac{(0.5 \times 33V)^2}{22\ k\Omega}$$

where:
$V_{P(sat)}$ = output saturation voltage on the buffer output
I_o = source current for one buffer output.

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6502; TDA6502A; TDA6503; TDA6503A	SSOP28	plastic shrink small outline package; 28 leads; body width 5.3 mm	SOT341-1

6 BLOCK DIAGRAM



The pin numbers in parenthesis represent the TDA6503 and TDA6503A.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN		DESCRIPTION
	TDA6502; TDA6502A	TDA6503; TDA6503A	
UHFIN1	1	28	UHF RF input 1
UHFIN2	2	27	UHF RF input 2
VHFIN	3	26	VHF RF input
RFGND	4	25	RF ground
IFFIL1	5	24	IF filter output 1
IFFIL2	6	23	IF filter output 2
PVHFL	7	22	PMOS port output, general purpose (e.g. VHF low sub-band)
PVHFH	8	21	PMOS port output, general purpose (e.g. VHF high sub-band)
PUHF	9	20	PMOS port output, UHF band
FMST	10	19	PMOS port output, general purpose (e.g. FM sound trap)
SW	11	18	bus format selection input: I^2C-bus mode or 3-wire bus mode
CE/AS	12	17	chip enable input in 3-wire bus mode or address selection input in I^2C-bus mode
DA	13	16	serial data input/output
CL	14	15	serial clock input
LOCK/ADC	15	14	lock detector output in 3-wire bus mode or ADC input in I^2C-bus mode
CP	16	13	charge pump output
VT	17	12	tuning voltage output
XTAL	18	11	crystal oscillator input
V_{CC}	19	10	supply voltage
IFOUT	20	9	IF output
GND	21	8	digital ground
VHFOSCIB	22	7	VHF oscillator input base
OSCGND	23	6	oscillator ground
VHFOSCOC	24	5	VHF oscillator output collector
UHFOSCIB1	25	4	UHF oscillator input 1 (base)
UHFOSCOC1	26	3	UHF oscillator output 1 (collector)
UHFOSCOC2	27	2	UHF oscillator output 2 (collector)
UHFOSCIB2	28	1	UHF oscillator input 2 (base)

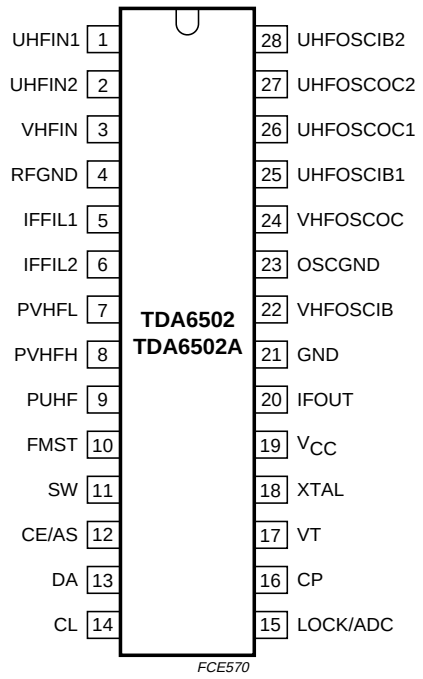


Fig.2 Pin configuration for TDA6502 and TDA6502A.

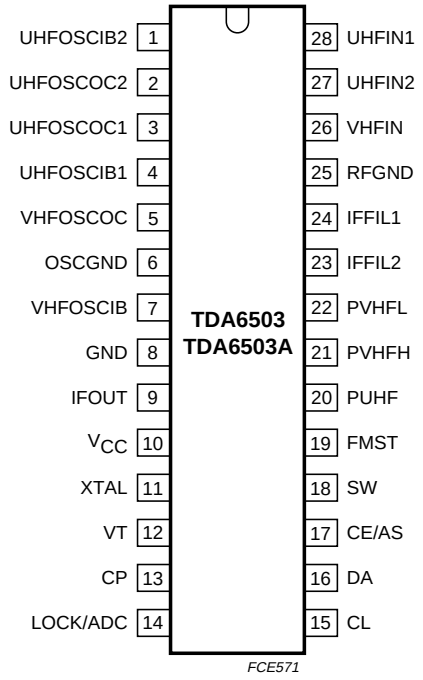


Fig.3 Pin configuration for TDA6503 and TDA6503A.

8 FUNCTIONAL DESCRIPTION

8.1 Control mode selection

The device is controlled via the I²C-bus or the 3-wire bus, depending on the voltage applied to pin SW (see Table 2).

A LOW level on pin SW enables the I²C-bus: pins CE/AS, DA and CL are used as address selection (AS), serial data (SDA) and serial clock (SCL) input respectively.

A HIGH level on pin SW enables the 3-wire bus: pins CE/AS, DA and CL are used as chip enable (CE), data and clock inputs respectively.

Table 2 Bus format selection

PIN			I²C-BUS MODE	3-WIRE BUS MODE
SYMBOL	TDA6502; TDA6502A	TDA6503; TDA6503A		
SW	11	18	LOW-level voltage or ground	HIGH-level voltage or open-circuit
CE/AS	12	17	address selection input	enable input
DA	13	16	serial data input	data input
CL	14	15	serial clock input	clock input
LOCK/ADC	15	14	ADC input or test output	lock detector output or test output

8.2 I²C-bus data format

8.2.1 I²C-BUS ADDRESS SELECTION

The module address contains programmable address bits MA1 and MA0 (see Tables 3, 4 and 9) which offer the possibility of having several synthesizers (up to 4) in one system by applying a specific voltage on pin CE/AS. The relationship between bits MA1 and MA0 and the input voltage applied to pin CE/AS is given in Table 6.

8.2.2 WRITE MODE

The write mode is defined by the address byte ADB with bit R/$\overline{W}$ = 0 (see Tables 3 and 4).

Data bytes can be sent to the device after the address transmission (first byte). Four data bytes are needed to fully program the device.

The bus transceiver has an auto-increment facility which permits the programming of the device within one single transmission (address byte + 4 data bytes). The device can also be partially programmed providing that the first data byte following the address byte is divider byte DB1 or the control byte CB.

The first bit of byte DB1 indicates whether frequency data (first bit = 0) or control and band-switch data (first bit = 1) will follow. Until an I²C-bus STOP command is sent by the controller, additional data bytes can be entered without the need to re-address the device.

The frequency register is loaded after the 8th clock pulse of byte DB2, the control register is loaded after the 8th clock pulse of the byte CB and the band-switch register is loaded after the 8th clock pulse of byte BB.

Table 3 I²C-bus data format for write mode of TDA6502 and TDA6503

NAME	BYTE	BITS							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	OS
Band-switch byte	BB	X	X	X	X	**FMST**	**PUHF**	PVHFH	PVHFL

Table 4 I²C-bus data format for write mode of TDA6502A and TDA6503A

NAME	BYTE	BIT							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0
Divider byte 1	DB1	0	N14	N13	N12	N11	N10	N9	N8
Divider byte 2	DB2	N7	N6	N5	N4	N3	N2	N1	N0
Control byte	CB	1	CP	T2	T1	T0	RSA	RSB	OS
Band-switch byte	BB	X	X	X	X	**PUHF**	**FMST**	PVHFH	PVHFL

Table 5 Description of the bits used in Tables 3 and 4

BIT	DESCRIPTION
MA1 and MA0	programmable address bits (see Table 6)
R/$\overline{W}$	logic 0 for write mode
N14 to N0	programmable divider bits: N = N14 $\times$ 2^{14} + N13 $\times$ 2^{13} + ... + N1 $\times$ 2^{1} + N0
CP	charge pump current control bit: logic 0: charge pump current is 60 μA logic 1: charge pump current is 280 μA (default)
T2, T1 and T0	test bits (see Table 7)
RSA and RSB	reference divider ratio select bits (see Table 8)
OS	tuning amplifier control bit: logic 0: tuning voltage is ‘on’ (during normal operating) logic 1: tuning voltage is ‘off’; high-impedance output of pin VT (default)
PVHFL, PVHFH, PUHF and FMST	PMOS ports control bits: logic 0: corresponding buffer is ‘off’ (default) logic 1: corresponding buffer is ‘on’
X	don’t care

Table 6 Address selection bits (I^2C-bus mode)

MA1	MA0	VOLTAGE APPLIED TO PIN CE/AS
0	0	0 V to 0.1V_{CC}
0	1	0.2V_{CC} to 0.3V_{CC} or open-circuit
1	0	0.4V_{CC} to 0.6V_{CC}
1	1	0.9V_{CC} to 1.0V_{CC}

Table 7 Test mode bits

T2	T1	T0	TEST MODE
0	0	0	normal mode
0	0	1	normal mode (note 1)
0	1	X	charge pump is off
1	1	0	charge pump is sinking current
1	1	1	charge pump is sourcing current
1	0	0	f_{REF} is available on pin LOCK/ADC (note 2)
1	0	1	$\frac{1}{2}f_{DIV}$ is available on pin LOCK/ADC (note 2)

Notes

1. This is the default mode at Power-on reset.
2. The ADC input cannot be used when these test modes are active; see Section 8.2.3 for more information.

Table 8 Reference divider ratio select bits

RSA	RSB	REFERENCE DIVIDER RATIO	FREQUENCY STEP (kHz)
X	0	80	50
0	1	128	31.25
1	1	64	62.5

8.2.3 READ MODE

The read mode is defined by the address byte ADB with bit R/$\overline{W}$ = 1 (see Table 9).

After the slave address has been recognized, the device generates an acknowledge pulse and status byte SB is transferred on the SDA line (MSB first). Data is valid on the SDA line during a HIGH level of the SCL line. A second data byte can be read from the device if the microcontroller generates an acknowledge on the SDA line (master acknowledge).

End of transmission will occur if no master acknowledge occurs. The device will then release the data line to allow the microcontroller to generate a STOP condition.

Bit POR is set to logic 1 at power-on. The bit is reset when an end-of-data is detected by the device (end of a read sequence). Control of the loop is made possible with bit FL which indicates when the loop is locked (bit FL = 1)

A built-in ADC input is available on pin LOCK/ADC (I^2C-bus mode only). This converter can be used to apply AFC information to the microcontroller of the IF section of the television.

Table 9 Read data format

NAME	BYTE	BIT							
		MSB(1)							**LSB**
Address byte	ADB	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 1
Status byte	SB	POR	FL	R	1	1	A2	A1	A0

Note

1. MSB is transmitted first.

Table 10 Description of the bits used in Table 9

BIT	DESCRIPTION
MA1 and MA0	programmable address bits (see Table 6)
R/$\overline{W}$	logic 1 for read mode
POR	Power-on reset flag: logic 0: at power-off logic 1: at power-on
FL	in-lock flag: logic 0: loop is not locked logic 1: loop is locked
R	ready flag: logic 0: mode after Power-on reset (bit T2 = 0, bit T1 = 0 and bit T0 = 1) **and** the PLL is locked logic 1: in other conditions
A2, A1 and A0	digital outputs of the 5-level ADC (see Table 11)

Table 11 Digital outputs for analog input levels (note 1)

A2	A1	A0	VOLTAGE APPLIED TO PIN LOCK/ADC
0	0	0	0 to $0.15V_{CC}$
0	0	1	$0.15V_{CC}$ to $0.30V_{CC}$
0	1	0	$0.30V_{CC}$ to $0.45V_{CC}$
0	1	1	$0.45V_{CC}$ to $0.60V_{CC}$
1	0	0	$0.60V_{CC}$ to $1.00V_{CC}$

Note

1. Accuracy is $\pm 0.03 \times V_{CC}$.

8.2.4 POWER-ON RESET

The power-on detection threshold voltage V_{POR} is set to 3.2 V at room temperature. Below this threshold the device is reset to the power-on state.

At power-on state the following actions take place:

- The charge pump current is set to 280 μA
- The tuning voltage output is disabled
- The test bits T2, T1 and T0 are set to logic ‘001’
- The divider bit RSB is set to logic 1
- Port register UHF is ‘off’, which means that the UHF oscillator and the UHF mixer are switched off. Consequently, the VHF oscillator and the VHF mixer are switched on. Port registers VHFL and VHFH are ‘off’, which means that the VHF tank circuit is operating in the VHF low sub-band. The tuning amplifier is switched off until the first transmission. In that case, the tank circuit is supplied with the maximum tuning voltage. The oscillator is therefore operating at the end of the VHF low sub-band.

Table 12 Default setting of the bits at Power-on reset

NAME	BYTE	BITS							
		MSB							LSB
Address byte	ADB	1	1	0	0	0	MA1	MA0	X
Divider byte 1	DB1	0	X	X	X	X	X	X	X
Divider byte 2	DB2	X	X	X	X	X	X	X	X
Control byte	CB	1	1	0	0	1	X	1	1
Band switch byte	BB	X	X	X	X	0	0	0	0

8.3 3-wire bus data format

During a HIGH level on pin CE/AS (enable line), the data is clocked into the data register at the HIGH-to-LOW transition of the clock (see Figs 4 and 5).

The first four bits control the PMOS ports and are loaded into the internal band-switch register on the 5th rising edge of the clock pulse.

The frequency bits are loaded into the frequency register at the HIGH-to-LOW transition of the enable line when an 18-bit or 19-bit data word is transmitted. When a 27-bit data word is transmitted, the frequency bits are loaded into the frequency register on the 20th rising edge of the clock pulse and the control bits at the HIGH-to-LOW transition of the enable line (see Fig.6).

In this control mode the reference divider is given by bits RSA and RSB (see Table 8).

The test bits T2, T1 and T0, the charge pump bit CP, the ratio select bit RSB and bit OS can only be selected or changed with a 27-bit transmission. They remain programmed if an 18-bit or 19-bit transmission occurs. Only bit RSA is controlled by the transmission length when the 18-bit or 19-bit format is used. When an 18-bit data word is transmitted, the most significant bit of the divider (bit N14) is internally set to logic 0 and bit RSA is set to logic 1. When a 19-bit data word is transmitted, bit RSA is set to logic 0.

It is not allowed to address the devices with words whose length is different from 18, 19 or 27 bits. A data word of less than 18 bits will not affect the frequency register of the device.

The definition of the bits is unchanged compared to the I^2C-bus mode.

8.3.1 POWER-ON RESET

The power-on detection threshold voltage V_{POR} is set to 3.2 V at room temperature. Below this threshold the device is reset to the power-on state.

At power-on state the following actions take place:

- The charge pump current is set to 280 μA
- The test bits T2, T1 and T0 are set to logic ‘001’
- The divider bit RSB is set to logic 1
- The tuning voltage output is disabled
- The tuning amplifier control bit OS is automatically reset to logic 0 in 18-bit and 19-bit modes when the first data word is received to allow normal operation
- Port register UHF is ‘off’, which means that the UHF oscillator and the UHF mixer are switched off. Consequently, the VHF oscillator and the VHF mixer are switched on. Port registers VHFL and VHFH are ‘off’, which means that the VHF tank circuit is operating in the VHF low sub-band. The tuning amplifier is switched off until the first transmission. In that case, the tank circuit is supplied with the maximum tuning voltage. The oscillator is therefore operating at the end of the VHF low sub-band
- The reference divider ratio is set to 64 or 128 if the first sequence to the device has 18 bits or 19 bits; if the sequence has 27 bits, the reference divider ratio is set by bits RSA and RSB (see Table 8).

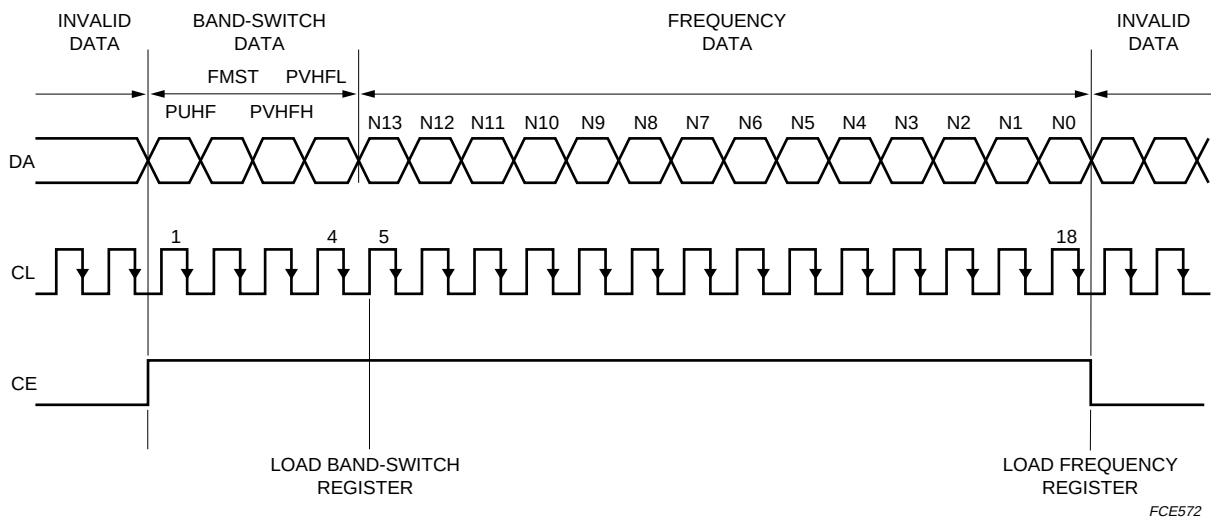


Fig.4 18-bit data format (bit RSA = 1).

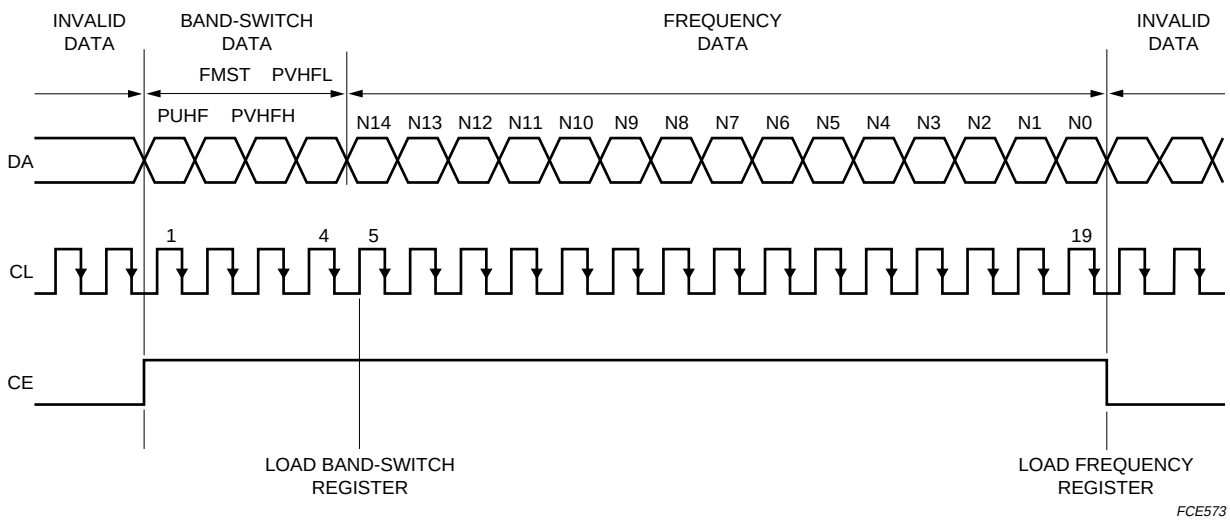


Fig.5 19-bit data format (bit RSA = 0).

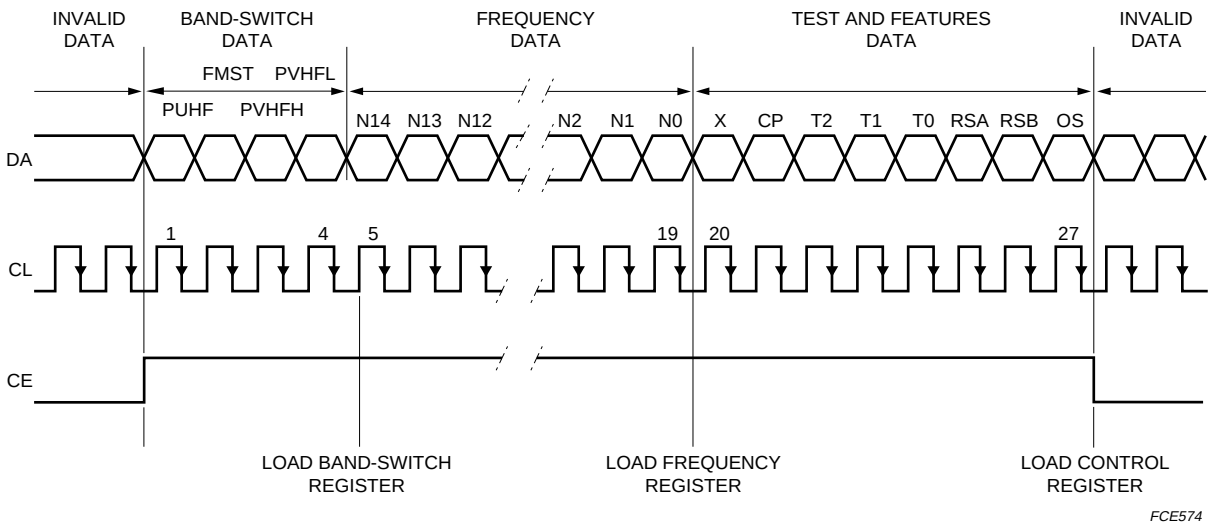


Fig.6 27-bit data format; test and features mode.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); note 1.

SYMBOL	PIN		PARAMETER	MIN.	MAX.	UNIT
	TDA6502; TDA6502A	TDA6503; TDA6503A				
V_{CC}	19	10	DC supply voltage	–0.3	+6	V
			OVS pulse time is 1 s; maximum current is 1 A	–	8	V
V_{Pn}	7 to 10	19 to 22	PMOS port output voltage	–0.3	V_{CC} +0.3	V
I_{Pn}	7 to 10	19 to 22	PMOS port output current	–1	+30	mA
V_{CP}	16	13	charge pump output voltage	–0.3	V_{CC} +0.3	V
V_{SW}	11	18	bus format selection input voltage	–0.3	V_{CC}+ 0.3	V
V_{VT}	17	12	tuning voltage output	–0.3	+35	V
$V_{LOCK/ADC}$	15	14	lock/ADC output/input voltage	–0.3	V_{CC} +0.3	V
V_{CL}	14	15	serial clock input voltage	–0.3	+6	V
V_{DA}	13	16	serial data input/output voltage	–0.3	+6	V
I_{DA}	13	16	data output current (I^2C-bus mode)	–1	+10	mA
$V_{CE/AS}$	12	17	chip enable/address selection input voltage	–0.3	+6	V
V_{XTAL}	18	11	crystal input voltage	–0.3	V_{CC} +0.3	V
$I_{O(n)}$	1 to 6, 19 to 28	1 to 10, 23 to 28	output current of each pin to ground	–	–10	mA
$t_{sc(max)}$	–	–	maximum short-circuit time (all pins to V_{CC} and all pins to GND, OSCGND and RFGND)	–	10	s
T_{stg}	–	–	storage temperature	–40	+150	°C
T_{amb}	–	–	ambient temperature	–20	+85	°C
T_j	–	–	junction temperature	–	150	°C

Note

1. Maximum ratings can not be exceeded, not even momentarily without causing irreversible IC damage. Maximum ratings can not be accumulated.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	110	K/W

11 CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply; T_{amb} = 25 °C						
V_{CC}	supply voltage		4.5	5.0	5.5	V
I_{CC}	supply current	at V_{CC} = 5 V				
		all PMOS ports 'off'	–	71	78	mA
		one PMOS port 'on' and sourcing 25 mA	–	103	113	mA
		one PMOS port 'on' and sourcing 25 mA; a second port 'on' and sourcing 5 mA	–	111	122	mA
PLL part; V_{CC} = 4.5 to 5.5 V; T_{amb} = −20 to +85 °C; unless otherwise specified						
FUNCTIONAL RANGE						
V_{POR}	power-on reset supply voltage	below this supply voltage power-on reset becomes active	–	3.2	–	V
N	divider ratio	15-bit frequency word	64	–	32767	
		14-bit frequency word	64	–	16383	
f_{XTAL}	crystal oscillator frequency	R_{XTAL} = 25 to 300 Ω	–	4.0	–	MHz
$\lvert Z_{XTAL} \rvert$	input impedance (absolute value)	f_{XTAL} = 4 MHz	600	1200	–	Ω
PMOS PORTS: PINS PUHF, PVHFL, PVHFH AND FMST						
$I_{Pn(off)}$	leakage current	V_{CC} = 5.5 V; V_{Pn} = 0 V	−10	–	–	µA
$V_{Pn(sat)}$	output saturation voltage	$V_{Pn(sat)} = V_{CC} - V_{Pn}$; one buffer output is 'on' and sourcing 25 mA	–	0.25	0.4	V
LOCK OUTPUT: PIN LOCK/ADC (IN 3-WIRE BUS MODE)						
I_{UNLOCK}	output current when the PLL is out-of-lock	V_{CC} = 5.5 V; V_O= 5.5 V	–	–	200	µA
V_{UNLOCK}	output saturation voltage when the PLL is out-of-lock	$V_{UNLOCK} = V_{CC} - V_O$; I_O = 200 µA	–	0.4	0.8	V
V_{LOCK}	output voltage	the PLL is locked	–	0.2	0.40	V
ADC INPUT: PIN LOCK/ADC (IN I^2C-BUS MODE)						
V_{ADC}	ADC input voltage	see Table 11	0	–	V_{CC}	V
$I_{ADC(H)}$	HIGH-level input current	$V_{ADC} = V_{CC}$	–	–	10	µA
$I_{ADC(L)}$	LOW-level input current	V_{ADC} = 0 V	−10	–	–	µA
BUS FORMAT SELECTION: PIN SW						
$V_{SW(L)}$	LOW-level input voltage		0	–	1.5	V
$V_{SW(H)}$	HIGH-level input voltage		3	–	V_{CC}	V
$I_{SW(H)}$	HIGH-level input current	$V_{SW} = V_{CC}$	–	–	10	µA
$I_{SW(L)}$	LOW-level input current	V_{SW} = 0 V	−100	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHIP ENABLE/ADDRESS SELECTION INPUT: PIN CE/AS						
$V_{CE/AS(L)}$	LOW-level input voltage		0	–	1.5	V
$V_{CE/AS(H)}$	HIGH-level input voltage		3	–	5.5	V
$I_{CE/AS(H)}$	HIGH-level input current	$V_{CE/AS}$ = 5.5 V	–	–	10	µA
$I_{CE/AS(L)}$	LOW-level input current	$V_{CE/AS}$ = 0 V	–10	–	–	µA
CLOCK AND DATA INPUTS: PINS CL AND DA						
$V_{CL(L)}$, $V_{DA(L)}$	LOW-level input voltage		0	–	1.5	V
$V_{CL(H)}$, $V_{DA(H)}$	HIGH-level input voltage		3	–	5.5	V
$I_{CL(H)}$, $I_{DA(H)}$	HIGH-level input current	V_{BUS} = 5.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{BUS} = 5.5 V; V_{CC} = 5.5 V	–	–	10	µA
$I_{CL(L)}$, $I_{DA(L)}$	LOW-level input current	V_{BUS} = 1.5 V; V_{CC} = 0 V	–	–	10	µA
		V_{BUS} = 0 V; V_{CC} = 5.5 V	–10	–	–	µA
DATA OUTPUT: PIN DA (IN I^2C-BUS MODE ONLY)						
$I_{DA(H)}$	HIGH-level output current	V_{DA} = 5.5 V	–	–	10	µA
$V_{DA(H)}$	HIGH-level output voltage	I_{DA} = 3 mA (sink current)	–	–	0.4	V
CLOCK FREQUENCY (I^2C-BUS MODE)						
f_{clk}	clock frequency		–	–	400	kHz
CHARGE PUMP OUTPUT: PIN CP						
$\lvert I_{CP(H)} \rvert$	HIGH-level input current (absolute value)	CP = 1	–	280	–	µA
$\lvert I_{CP(L)} \rvert$	LOW-level input current (absolute value)	CP = 0	–	60	–	µA
$I_{CP(leak)}$	off-state leakage current	T2 = 0; T1 = 1	–15	–0.5	+15	nA
TUNING VOLTAGE OUTPUT: PIN VT						
$I_{VT(off)}$	leakage current when switched-off	OS = 1; tuning supply is 33 V	–	–	10	µA
V_{VT}	output voltage when the loop is closed	OS = 0; T2 = 0; T1 = 0; T0 = 1; R_L = 27 kΩ; tuning supply is 33 V	0.2	–	32.7	V
Mixer/oscillator part; V_{CC} = 5 V; T_{amb} = 25 °C; measurements related to the measurement circuit (see Fig.19)						
VHF MIXER (INCLUDING IF PREAMPLIFIER)						
$f_{RF(o)}$	RF operational frequency		40		800	MHz
f_{RF}	RF frequency	note 1	55.25	–	361.25	MHz
G_v	voltage gain	f_{RF} = 57.5 MHz; see Fig.12	17.5	20	22.5	dB
		f_{RF} = 363.5 MHz; see Fig.12	17.5	20	22.5	dB
NF	noise figure	f_{RF} = 50 MHz; see Figs 13 and 14	–	7.5	10	dB
		f_{RF} = 150 MHz; see Figs 13 and 14	–	7.5	10	dB
		f_{RF} = 300 MHz; see Fig.14	–	7.5	10	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_o	output voltage (causing 1% cross modulation in channel)	f_{RF} = 55.25 MHz; see Fig.15	107	110	–	dBμV
		f_{RF} = 361.25 MHz; see Fig.15	107	110	–	dBμV
V_i	input voltage (causing pulling-in channel at 750 Hz)	f_{RF} = 361.25 MHz; note 2	–	83	–	dBμV
g_{os}	optimum source conductance for noise figure	f_{RF} = 50 MHz	–	0.7	–	mS
		f_{RF} = 150 MHz	–	0.9	–	mS
		f_{RF} = 300 MHz	–	1.5	–	mS
g_i	input conductance	f_{RF} = 55.25 MHz; see Fig.7	–	0.3	–	mS
		f_{RF} = 361.25 MHz; see Fig.7	–	0.4	–	mS
C_i	input capacitance	f_{RF} = 57.5 to 357.5 MHz; see Fig.7	–	1.35	–	pF
VHF OSCILLATOR						
$f_{OSC(o)}$	oscillator operational frequency		60		600	MHz
f_{OSC}	oscillator frequency	note 3	101	–	407	MHz
$\Delta f_{OSC(V)}$	oscillator frequency variation with supply voltage	ΔV_{CC} = 5%; note 4	–	60	–	kHz
		ΔV_{CC} = 10%; note 4	–	110	–	kHz
$\Delta f_{OSC(T)}$	oscillator frequency variation with temperature	ΔT = 25 °C; with compensation; note 5	–	1600	–	kHz
$\Delta f_{OSC(t)}$	oscillator frequency drift	5 s to 15 min after switch-on; note 6	–	400	–	kHz
Φ_{OSC}	phase noise, carrier-to-noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	105	–	dBc/Hz
RSC	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V; worst case in the frequency range; ripple frequency 500 kHz; note 7	15	30	–	mV
UHF MIXER (INCLUDING IF PREAMPLIFIER)						
$f_{RF(o)}$	RF operational frequency		200		900	MHz
f_{RF}	RF frequency	note 1	367.25	–	801.25	MHz
G_v	voltage gain	f_{RF} = 369.5 MHz; see Fig.16	29	32	35	dB
		f_{RF} = 803.5 MHz; see Fig.16	29	32	35	dB
NF	noise figure (not corrected for image)	f_{RF} = 369.5 MHz; see Fig.17	–	7	9	dB
		f_{RF} = 803.5 MHz; see Fig.17	–	7	9	dB
V_o	output voltage (causing 1% cross modulation in channel)	f_{RF} = 367.25 MHz; see Fig.18	107	110	–	dBμV
		f_{RF} = 801.25 MHz; see Fig.18	107	110	–	dBμV
V_i	input voltage (causing pulling in channel at 750 Hz)	f_{RF} = 801.25 MHz; note 2	–	85	–	dBμV

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Z_i	input impedance ($R_S + jL_S\omega$)	R_S at f_{RF} = 367.25 MHz; see Fig.8	–	26	–	Ω
		R_S at f_{RF} = 801.25 MHz; see Fig.8	–	28	–	Ω
		L_S at f_{RF} = 367.25 MHz; see Fig.8	–	8.5	–	nH
		L_S at f_{RF} = 801.25 MHz; see Fig.8	–	8	–	nH
UHF OSCILLATOR						
$f_{OSC(o)}$	oscillator operational frequency		300		1000	MHz
f_{OSC}	oscillator frequency	note 3	413	–	847	MHz
$\Delta f_{OSC(V)}$	oscillator frequency variation with supply voltage	ΔV_{CC} = 5%; note 4	–	35	–	kHz
		ΔV_{CC} = 10%; note 4	–	100	–	kHz
$\Delta f_{OSC(T)}$	oscillator frequency variation with temperature	ΔT = 25 °C; with compensation; note 5	–	500	–	kHz
$\Delta f_{OSC(t)}$	oscillator frequency drift	5 s to 15 min after switching on; note 6	–	120	–	kHz
Φ_{OSC}	phase noise, carrier-to-noise sideband	±100 kHz frequency offset; worst case in the frequency range	–	105	–	dBc/Hz
RSC	ripple susceptibility of V_{CC} (peak-to-peak value)	V_{CC} = 5 V; worst case in the frequency range; ripple frequency 500 kHz; note 7	15	30	–	mV
IF PREAMPLIFIER						
IF	IF operational frequency		30		60	MHz
S_{22}	output reflection coefficient	magnitude; see Fig.9	–	–12.8	–	dB
		phase; see Fig.9	–	0.2	–	degree
Z_o	output impedance ($R_S + jL_S\omega$)	R_S at 43.5 MHz; see Fig.9	–	80	–	Ω
		L_S at 43.5 MHz; see Fig.9	–	0.5	–	nH
REJECTION AT THE IF OUTPUT						
INT_{div}	level of divider interferences in the IF signal	worst case; note 8	–	16	20	dBμV
INT_{xtal}	crystal oscillator interferences rejection	V_{IF} = 100 dBμV; worst case in the frequency range; note 9	60	–	–	dBc
INT_{ref}	reference frequency rejection	V_{IF} = 100 dBμV; worst case in the frequency range; f_{REF} = 62.5 kHz; note 10	60	–	–	dBc
INT_{ch6}	channel 6 beat	$V_{RF(pix)} = V_{RF(snd)}$ = 80 dBμV; note 11	tbf	54	–	dBc
INT_{chA-5}	channel A-5 beat	$V_{RF(pix)}$ = 80 dBμV; note 12	tbf	60	–	dBc

Notes

1. The RF frequency range is defined by the oscillator frequency range and the IF frequency.
2. This is the level of the RF signal (100% amplitude modulated with 11.89 kHz) that causes a 750 Hz frequency deviation on the oscillator signal; it produces sidebands 30 dB below the level of the oscillator signal.
3. Limits are related to the tank circuits used in Fig.19; frequency bands may be adjusted by the choice of external components.

4. The frequency shift is defined as a change in oscillator frequency when the supply voltage varies from V_{CC} = 5 to 4.75 V (4.5 V) or from V_{CC} = 5 to 5.25 V (5.5 V). The oscillator is free running during this measurement.
5. The frequency drift is defined as a change in oscillator frequency when the ambient temperature varies from T_{amb} = 25 to 50 °C or from T_{amb} = 25 to 0 °C. The oscillator is free running during this measurement.
6. Switch-on drift is defined as the change in oscillator frequency between 5 s and 15 min after switch-on. The oscillator is free running during this measurement.
7. The ripple susceptibility is measured for a 500 kHz ripple at the IF output using the measurement circuit of Fig.19; the level of the ripple signal is increased until a difference of 53.5 dB occurs between the IF carrier fixed at 100 dBµV and the sideband components.
8. This is the level of divider interferences close to the IF frequency. For example channel C: f_{OSC} = 179 MHz, $\frac{1}{4} f_{OSC}$ = 44.75 MHz. The VHFIN input must be left open (i.e. not connected to any load or cable); The UHFIN1 and UHFIN2 inputs are connected to a hybrid.
9. Crystal oscillator interference means the 4 MHz sidebands caused by the crystal oscillator. The rejection has to be greater than 60 dB for an IF output signal of 100 dBµV.
10. The reference frequency rejection is the level of reference frequency sidebands related to the sound sub-carrier.
11. Channel 6 beat is the interfering product of $f_{RF(pix)} + f_{RF(snd)} - f_{OSC}$ of channel 6 at 42 MHz.
12. Channel A-5 beat is the interfering product of $f_{RF(pix)}$, f_{IF} and f_{OSC} of channel A-5: f_{beat} = 45.5 MHz. The possible mechanisms are: $f_{OSC} - 2 \times f_{IF}$ or $2 \times f_{RF(pix)} - f_{OSC}$. For the measurement: V_{RF} = 80 dBµV.

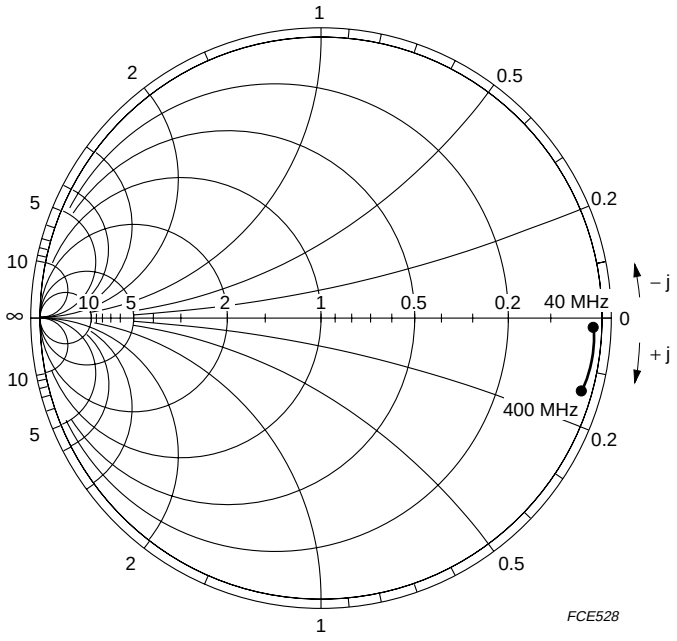


Fig.7 Input admittance (S_{11}) of the VHF mixer input (40 to 400 MHz); Y_0 = 20 mS.

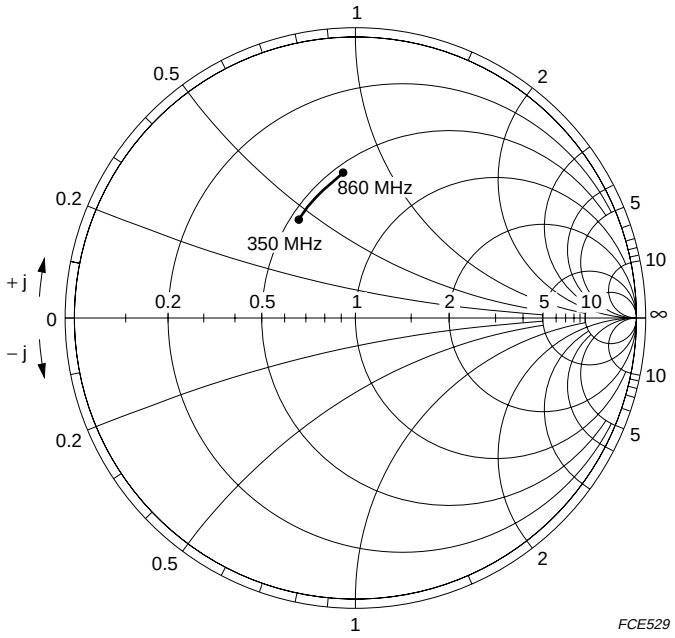


Fig.8 Input impedance (S_{11}) of the UHF mixer input (350 to 860 MHz); Z_0 = 50 Ω.

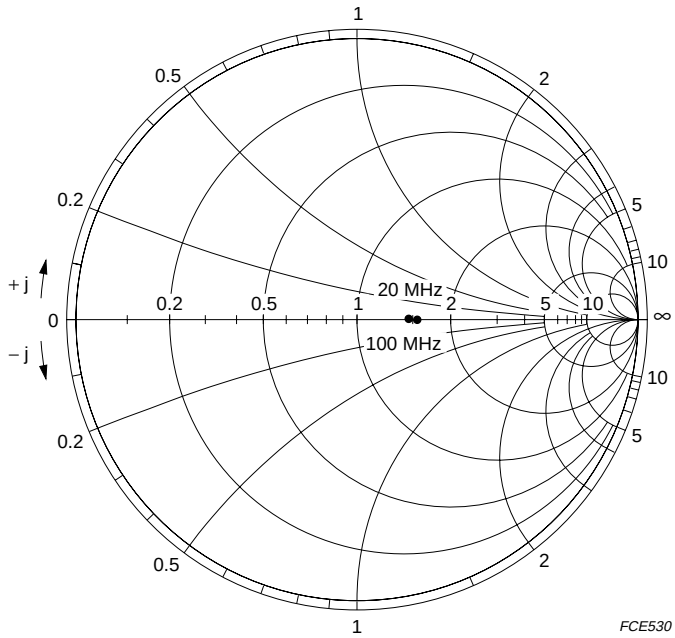


Fig.9 Output impedance (S_{22}) of the IF amplifier (20 to 60 MHz); Z_0 = 50 Ω.

12 TIMING CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN.	UNIT
3-wire bus timing				
t_{HIGH}	clock HIGH time	see Fig.10	2	µs
$t_{SU;DA}$	data set-up time	see Fig.10	2	µs
$t_{HD;DA}$	data hold time	see Fig.10	2	µs
$t_{SU;ENCL}$	enable-to-clock set-up time	see Fig.10	10	µs
$t_{HD;ENDA}$	enable-to-data hold time	see Fig.10	2	µs
t_{EN}	enable time between two transmissions	see Fig.11	10	µs
$t_{HD;ENCL}$	enable-to-clock active edge hold time	see Fig.11	6	µs

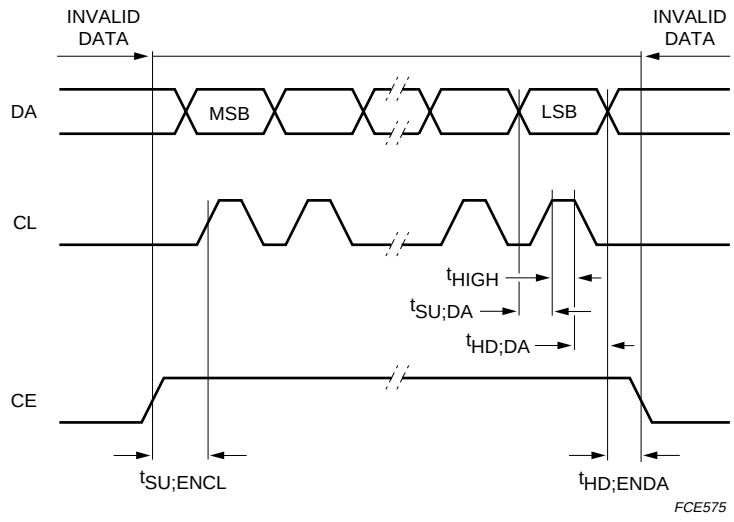


Fig.10 Timing diagram for 3-wire bus; DA, CL and CE.

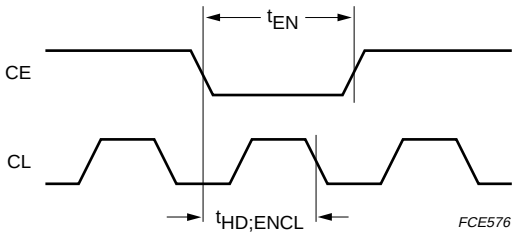
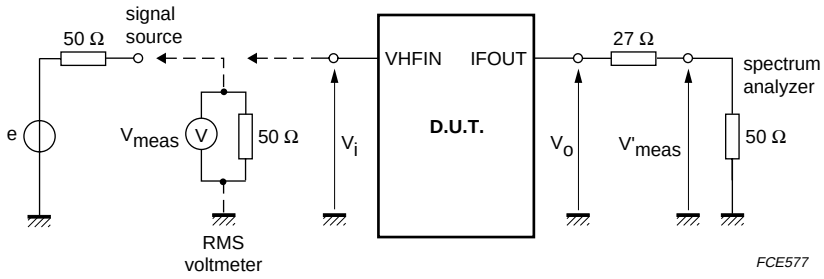


Fig.11 Timing diagram for 3-wire bus; CE and CL.

13 TEST AND APPLICATION INFORMATION

13.1 Test circuits



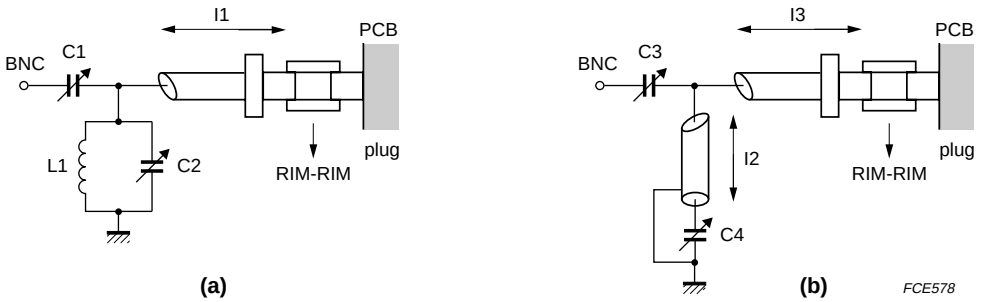
$Z_i >> 50\ \Omega \Rightarrow V_i = 2 \times V_{meas} = 80\ dB\mu V$

$V_i = V_{meas} + 6\ dB = 80\ dB\mu V$

$V_o = V'_{meas} \times \frac{50 + 27}{50}$

$G_v = 20 \log \frac{V_o}{V_i}$

Fig.12 Gain measurement in VHF band.



(a) For f_{RF} = 50 MHz:

mixer A frequency response measured = 57 MHz, loss = 0 dB

image suppression = 16 dB

C1 = 9 pF

C2 = 15 pF

L1 = 7 turns (∅ 5.5 mm, wire ∅ = 0.5 mm)

l1 = semi rigid cable (RIM) of 5 cm long (semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

(b) For f_{RF} = 150 MHz:

mixer A frequency response measured = 150.3 MHz, loss = 1.3 dB

image suppression = 13 dB

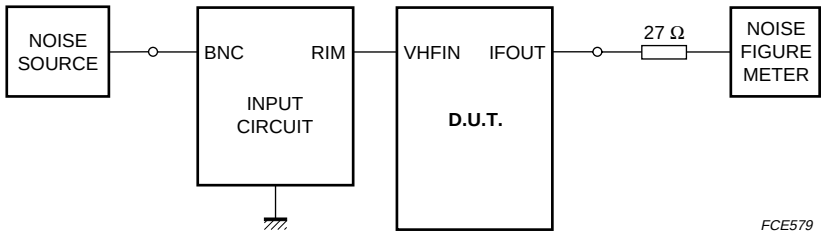
C3 = 5 pF

C4 = 25 pF

l2 = semi rigid cable (RIM): 30 cm long

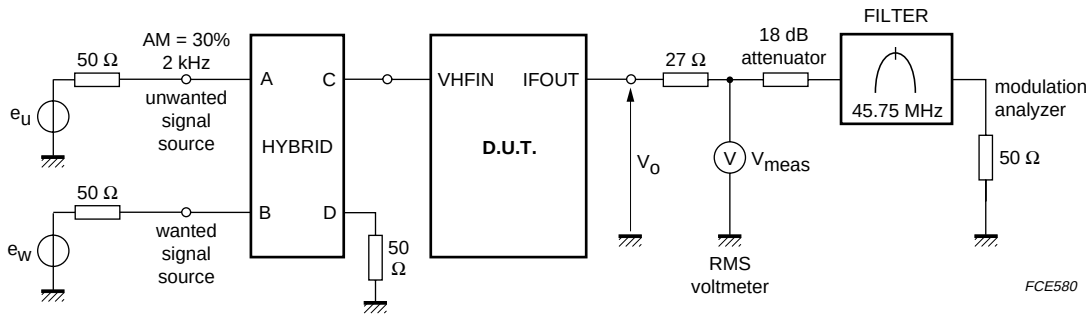
l3 = semi rigid cable (RIM) of 5 cm long (semi rigid cable (RIM); 33 dB/100 m; 50 Ω; 96 pF/m).

Fig.13 Input circuit for optimum noise figure in VHF band.



NF = NF_{meas} – loss (of input circuit) (dB).

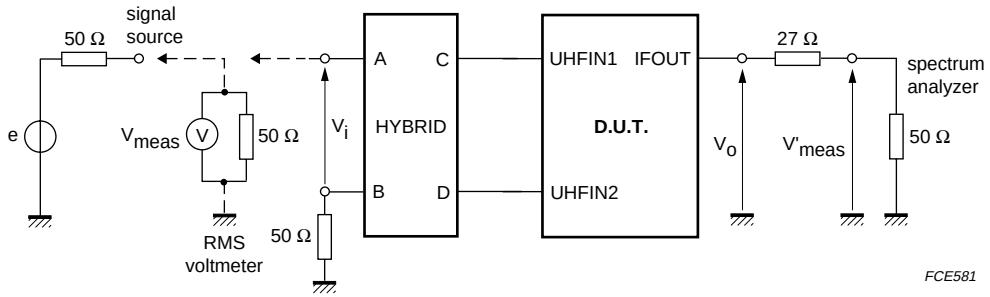
Fig.14 Noise figure (NF) measurement in VHF band.



$V_o = V_{meas} \times \frac{50 + 27}{50}$

Wanted output signal at $f_{RF(w)}$ = 55.25 (361.25) MHz; $V_{o(w)}$ = 100 dBμV.
Measuring the level of the unwanted output signal $V_{o(u)}$ causing 0.3% AM modulation in the wanted output signal; $f_{RF(u)}$ = 59.75 (366.75) MHz.
f_{OSC} = 101 (407) MHz.
Filter characteristics: f_c = 45.75 MHz, $f_{-3\ dB(BW)}$ = 1.4 MHz, $f_{-30\ dB(BW)}$ = 3.1 MHz.

Fig.15 Cross modulation measurement in VHF band.



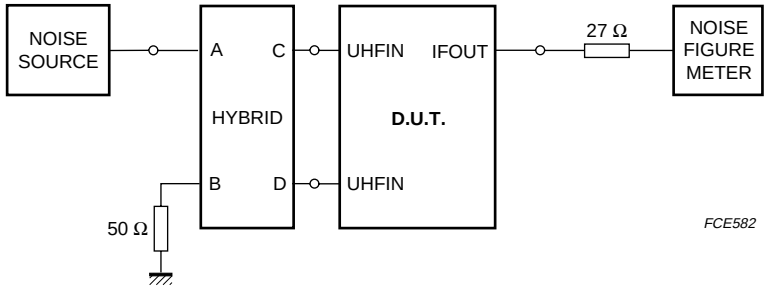
Loss (in hybrid) = 1 dB.

$V_i = V_{meas}$ – loss (in hybrid) = 70 dBμV.

$$V_o = V'_{meas} \times \frac{50 + 27}{50}$$

$$G_v = 20 \log \frac{V_o}{V_i}$$

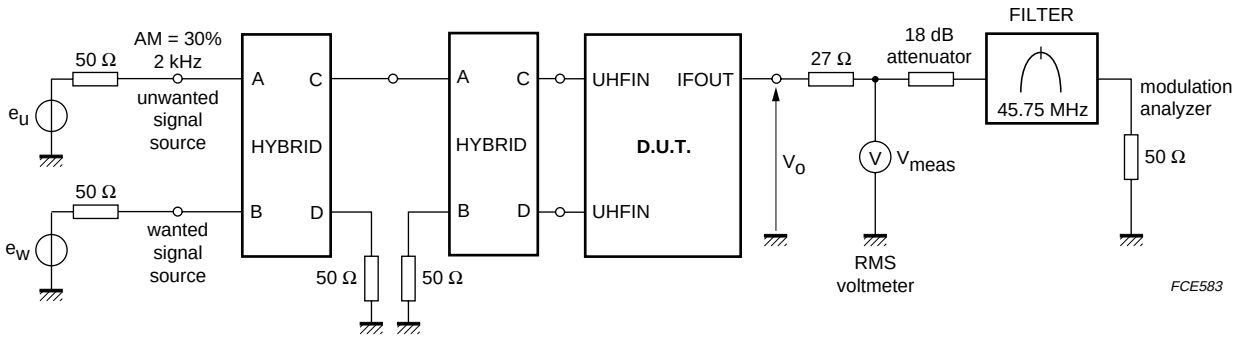
Fig.16 Gain (G_v) measurement in UHF band.



Loss (in hybrid) = 1 dB.

$NF = NF_{meas}$ – loss (in hybrid).

Fig.17 Noise figure (NF) measurement in bands UHF.



$$V_o = V_{meas} \times \frac{50 + 27}{50}$$

Wanted output signal at $f_{RF(w)}$ = 367.25 (801.25) MHz; $V_{o(w)}$ = 100 dBμV.
Measuring the level of the unwanted output signal $V_{o(u)}$ causing 0.3% AM modulation in the wanted output signal; $f_{RF(u)}$ = 371.25 (805.75) MHz.
f_{OSC} = 413 (847) MHz.
Filter characteristics: f_c = 45.75 MHz, $f_{-3\ dB(BW)}$ = 1.4 MHz, $f_{-30\ dB(BW)}$ = 3.1 MHz.

Fig.18 Cross modulation measurement in UHF band.

13.2 Measurement circuit

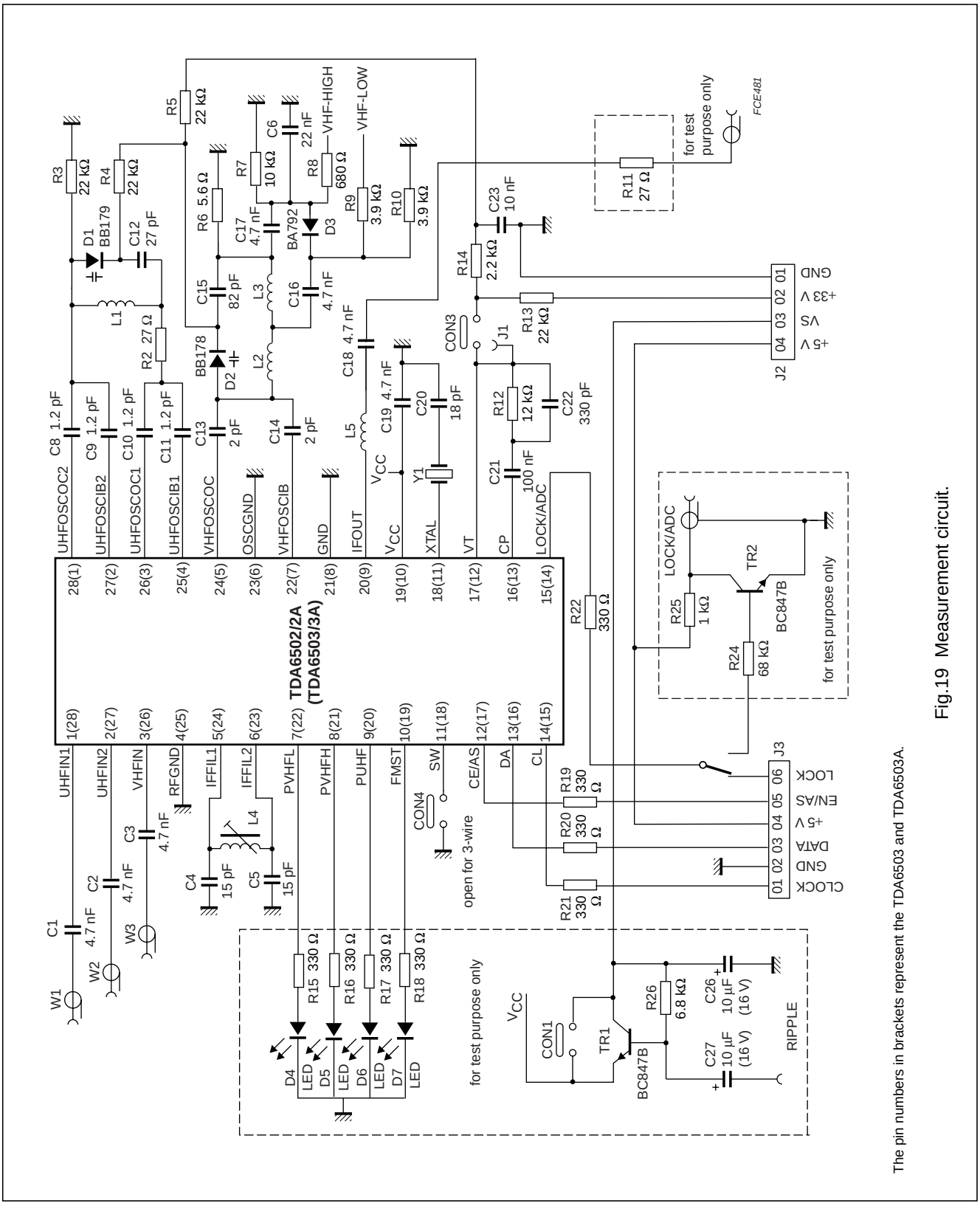


Fig.19 Measurement circuit.

Table 13 Capacitors (all SMD and NP0)

COMPONENT	VALUE
C1	4.7 nF
C2	4.7 nF
C3	4.7 nF
C4	15 pF
C5	15 pF
C6	22 nF
C8	1.2 pF (N750)
C9	1.2 pF (N750)
C10	1.2 pF(N750)
C11	1.2 pF (N750)
C12	27 pF (N750)
C13	2 pF (N750)
C14	2 pF (N750)
C15	82 pF (N750)
C16	4.7 nF
C17	4.7 nF
C18	4.7 nF
C19	4.7 nF
C20	18 pF
C21	100 nF
C22	330 pF
C23	10 nF
C26	10 μF (16 V, electrolytic)
C27	10 μF (16 V, electrolytic)

Table 14 Resistors (all SMD)

COMPONENT	VALUE
R2	27 Ω
R3	22 kΩ
R4	22 kΩ
R5	22 kΩ
R6	5.6 Ω
R7	10 kΩ
R8	680 Ω
R9	3.9 kΩ
R10	3.9 kΩ
R11	27 Ω
R12	12 kΩ
R13	22 kΩ
R14	2.2 kΩ
R15	330 Ω
R16	330 Ω
R17	330 Ω
R18	330 Ω
R19	330 Ω
R20	330 Ω
R21	330 Ω
R22	330 Ω
R24	68 kΩ
R25	1 kΩ
R26	6.8 kΩ

Table 15 Diodes and ICs

COMPONENT	VALUE
D1	BB179
D2	BB178
D3	BA792
IC	TDA6502; TDA6502A TDA6503; TDA6503A

Table 16 Coils (note 1)

COMPONENT	VALUE
L1	1.5 turns; diameter 1.5 mm
L2	2.5 turns; diameter 2.5 mm
L3	7.5 turns; diameter 3.0 mm
L5	2.5 turns; diameter 2.5 mm

Note

1. Wire size is 0.4 mm.

Table 17 Transformer (note 1)

COMPONENT	VALUE
L4	2 x 5 turns

Note

1. Coil type: TOKO 7kN; material: 113 kN; screw core: 03-0093; pot core: 04-0026.

Table 18 Crystal

COMPONENT	VALUE
Y1	4 MHz

Table 19 Transistors

COMPONENT	VALUE
TR1	BC847B
TR2	BC847B

13.3 Tuning amplifier

The tuning amplifier is capable of driving the varicap voltage without an external transistor. The tuning voltage output must be connected to an external load of 27 kΩ which is connected to the tuning voltage supply rail. The loop filter design depends on the oscillator characteristics and the selected reference frequency.

13.4 Crystal oscillator

The crystal oscillator uses a 4 MHz crystal connected in series with an 18 pF capacitor thereby operating in the series resonance mode. Connecting the crystal to the ground is preferred, but it can also be connected to the supply voltage.

13.5 Examples of I²C-bus data format sequences for TDA6502 and TDA6503

Tables 20 to 24 show the various write sequences where:

S = START bit

A = acknowledge bit

P = STOP bit.

Conditions:

f_{xtal} = 4 MHz

N = 1600

f_{osc} = 100 MHz

f_{step} = 62.5 kHz

Port register VHFL is ‘on’ to switch-on band VHF low

Port register FMST is ‘on’ to switch-on an FM sound trap

I_{CP} = 280 μA.

13.5.1 Write sequences to register C2

Table 20 Complete sequence with first the divider bytes (first data bit = 0)

START	ADDRESS BYTE	ACK	DIVIDER BYTE 1	ACK	DIVIDER BYTE 2	ACK	CONTROL BYTE	ACK	BAND-SWITCH BYTE	ACK	STOP
S	C2	A	06	A	40	A	CE	A	09	A	P

Table 21 Complete sequence with first the control and band-switch bytes (first data bit = 1)

START	ADDRESS BYTE	ACK	CONTROL BYTE	ACK	BAND-SWITCH BYTE	ACK	DIVIDER BYTE 1	ACK	DIVIDER BYTE 2	ACK	STOP
S	C2	A	CE	A	09	A	06	A	40	A	P

Table 22 Sequence with divider bytes only (first data bit = 0)

START	ADDRESS BYTE	ACK	DIVIDER BYTE 1	ACK	DIVIDER BYTE 2	ACK	STOP
S	C2	A	06	A	40	A	P

Table 23 Sequence with control and band-switch bytes only (first data bit = 1)

START	ADDRESS BYTE	ACK	CONTROL BYTE	ACK	BAND-SWITCH BYTE	ACK	STOP
S	C2	A	CE	A	09	A	P

Table 24 Sequence with control byte only (first data bit = 1)

START	ADDRESS BYTE	ACK	CONTROL BYTE	ACK	STOP
S	C2	A	CE	A	P

13.5.2 READ SEQUENCES FROM REGISTER C3

Tables 25 and 26 show the various read sequences where:

S = START bit

A = acknowledge bit

XX = read status byte

X = no acknowledge from the master means end of sequence

P = STOP bit

Table 25 One status byte acquisition

START	ADDRESS BYTE	ACK	STATUS BYTE	ACK	STOP
S	C3	A	XX	X	P

Table 26 Two status bytes acquisition

START	ADDRESS BYTE	ACK	STATUS BYTE	ACK	STATUS BYTE	ACK	STOP
S	C3	A	XX	A	XX	X	P

13.6 Examples of 3-wire bus data format sequences for TDA6502 and TDA6503

13.6.1 18-BIT SEQUENCE

Conditions:

f_{osc} = 800 MHz

Port register PUHF is ‘on’.

Table 27 18-bit sequence

PUHF	FMST	PVHFH	PVHFL	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
1	0	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0

The reference divider is automatically set to 64 assuming that bit RSB has been set to logic 1 at power-on. If bit RSB has been set to logic 0, in a previous 27-bit sequence, the reference divider will still be set at 80. In this event, the 18-bit sequence has to be adapted to the 80 divider ratio.

13.6.2 19-BIT SEQUENCE

Conditions:

f_{osc} = 650 MHz

Port register PUHF is ‘on’.

Table 28 19-bit sequence

PUHF	FMST	PVHFH	PVHFL	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
1	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0	0

The reference divider is automatically set to 128 assuming that bit RSB has been set to logic 1 at power-on. If bit RSB has been set to logic 0 in a previous 27-bit sequence, the reference divider will still be set at 80. In this event, the 19-bit sequence has to be adapted to the 80 divider ratio.

13.6.3 27-BIT SEQUENCE

Conditions:

f_{osc} = 750 MHz

Port register PUHF is ‘on’

Reference divider is set at 80

I_{CP} = 60 μA

No test function.

Table 29 27-bit sequence

PORT BITS				FREQUENCY DATA BITS														CONTROL DATA BITS							
				14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	X	CP	T2	T1	T0	RSA	RSB	OS
1	0	0	0	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0

To change the oscillator frequency to 600 MHz in 50 kHz steps a 19-bit sequence or an 18-bit sequence can be used. The charge pump current remains at 60 μA.

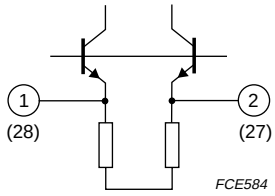
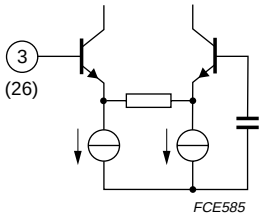
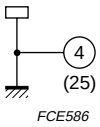
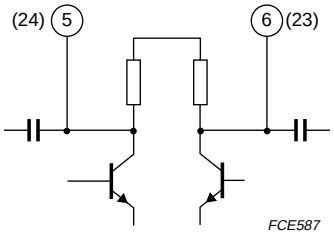
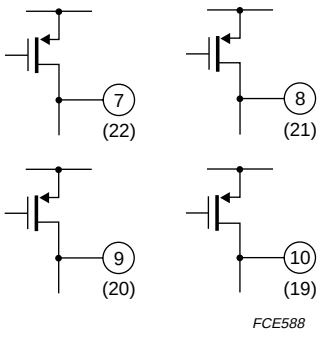
Table 30 Changing frequency with a 19-bit sequence

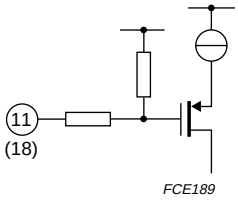
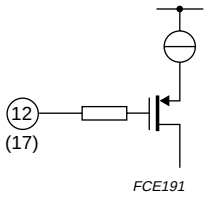
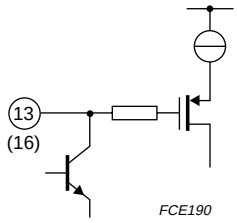
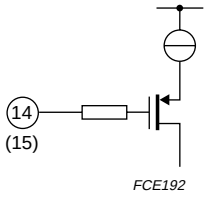
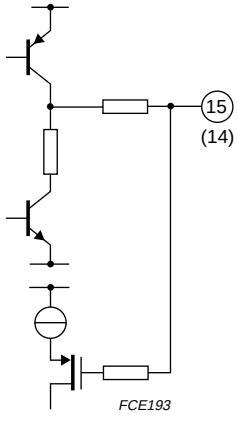
PORT BITS				FREQUENCY DATA BITS														
				14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0

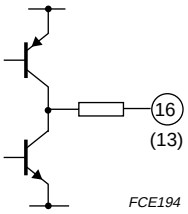
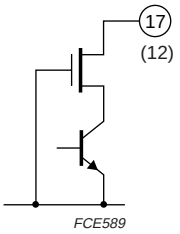
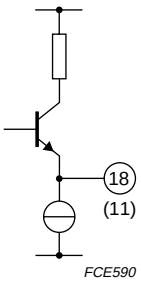
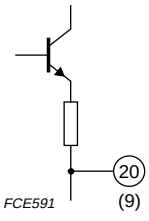
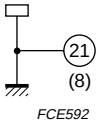
Table 31 Changing frequency with an 18-bit sequence

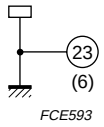
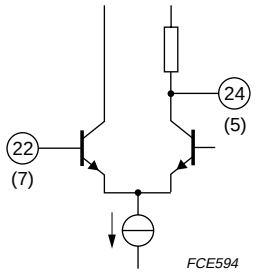
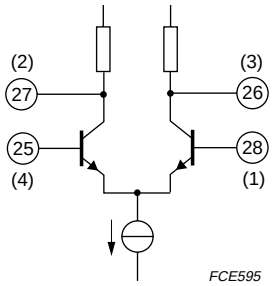
PORT BITS				FREQUENCY DATA BITS														
				13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	0	0	0	1	0	1	1	1	0	1	1	1	0	0	0	0	0	

14 INTERNAL PIN CONFIGURATION

SYMBOL	PIN		DC VOLTAGE (AVERAGE VALUE)(2)		EQUIVALENT CIRCUIT(1)
	TDA6502; TDA6502A	TDA6503; TDA6503A	VHF	UHF	
UHFIN1	1	28	–	1.0 V	
UHFIN2	2	27	–	1.0 V	
VHFIN	3	26	–	–	
RFGND	4	25	0.0 V	0.0 V	
IFFIL1	5	24	3.6 V	3.6 V	
IFFIL2	6	23	3.6 V	3.6 V	
PVHFL	7	22	n.a. or 4.8 V	n.a.	
PVHFH	8	21	4.8 V or n.a.	n.a.	
PUHF	9	20	n.a.	4.8 V	
FMST	10	19	n.a. or 4.8 V	n.a. or 4.8 V	

SYMBOL	PIN		DC VOLTAGE (AVERAGE VALUE)(2)		EQUIVALENT CIRCUIT(1)
	TDA6502; TDA6502A	TDA6503; TDA6503A	VHF	UHF	
SW	11	18	5.0 V	5.0 V	
CE/AS	12	17	1.25 V	1.25 V	
DA	13	16	–	–	
CL	14	15	–	–	
LOCK/ADC	15	14	4.6 V	4.6 V	

SYMBOL	PIN		DC VOLTAGE (AVERAGE VALUE)(2)		EQUIVALENT CIRCUIT(1)
	TDA6502; TDA6502A	TDA6503; TDA6503A	VHF	UHF	
CP	16	13	1 V	1 V	
VT	17	12	V_{VT}	V_{VT}	
XTAL	18	11	2.6 V	2.6 V	
V_{CC}	19	10	5.0 V	5.0 V	supply voltage
IFOUT	20	9	2.1 V	2.1 V	
GND	21	8	0.0 V	0.0 V	

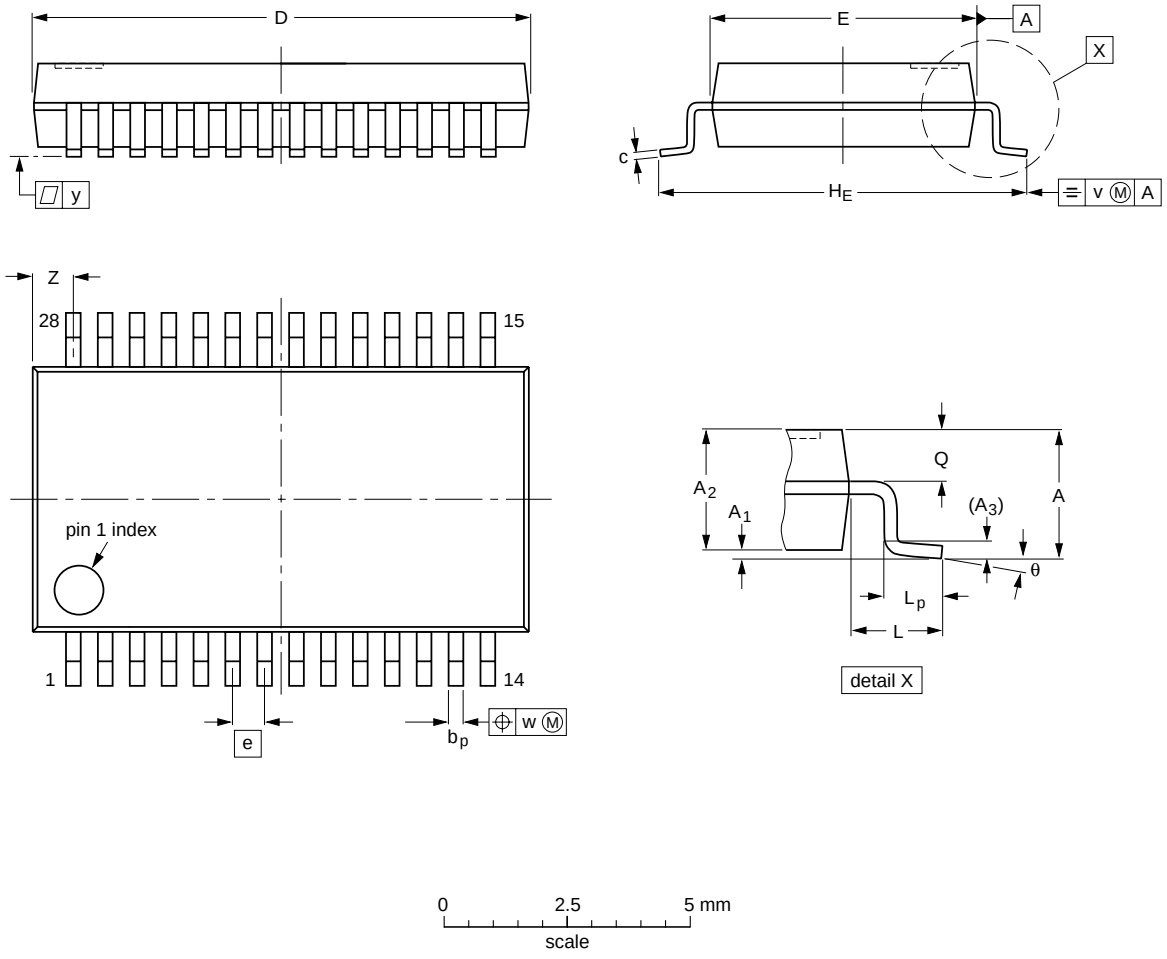
SYMBOL	PIN		DC VOLTAGE (AVERAGE VALUE)(2)		EQUIVALENT CIRCUIT(1)
	TDA6502; TDA6502A	TDA6503; TDA6503A	VHF	UHF	
OSCGND	23	6	0.0 V	0.0 V	
VHFOSCIB	22	7	1.8 V	–	
VHFOSCOC	24	5	3.0 V	–	
UHFOSCIB1	25	4	–	1.9 V	
UHFOSCOC1	26	3	–	2.9 V	
UHFOSCOC2	27	2	–	2.9 V	
UHFOSCIB2	28	1	–	1.9 V	

Notes

1. The pin numbers in parenthesis represent the TDA6503 and TDA6503A.
2. Measured in circuit of Fig.19.

15 PACKAGE OUTLINE

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150				~~95-02-04~~ 99-12-27

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

19 PURCHASE OF PHILIPS I²C COMPONENTS

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NOTES

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