

INTEGRATED CIRCUITS

DATA SHEET

TDA7057Q

**2 x 3 W stereo BTL audio output
amplifier**

Objective specification
File under Integrated Circuits, IC01

May 1992

2 x 3 W stereo BTL audio output amplifier

TDA7057Q

FEATURES

- No external components
- No switch-on and off clicks
- Good overall stability
- Low power consumption
- Short-circuit proof
- Low HF radiation
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA7057Q is a stereo output amplifier in a 13 pin power package. The device is designed for battery-fed portable stereo recorders and radios, but also suitable for mains-fed applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
P_O	output power	$V_P = 11\text{ V}; R_L = 16\ \Omega$	–	3	–	W
G_V	voltage gain		39	40	41	dB
I_P	total quiescent current	$V_P = 11\text{ V}; R_L = \infty$	–	10	14	mA
THD	total harmonic distortion	$P_O = 0.5\text{ W}$	–	0.25	1	%

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PIN	PIN POSITION	MATERIAL	CODE
TDA7057Q	13	SBD	plastic	SOT141 ⁽¹⁾

Note

1. SOT141-6; 1996 September 9.

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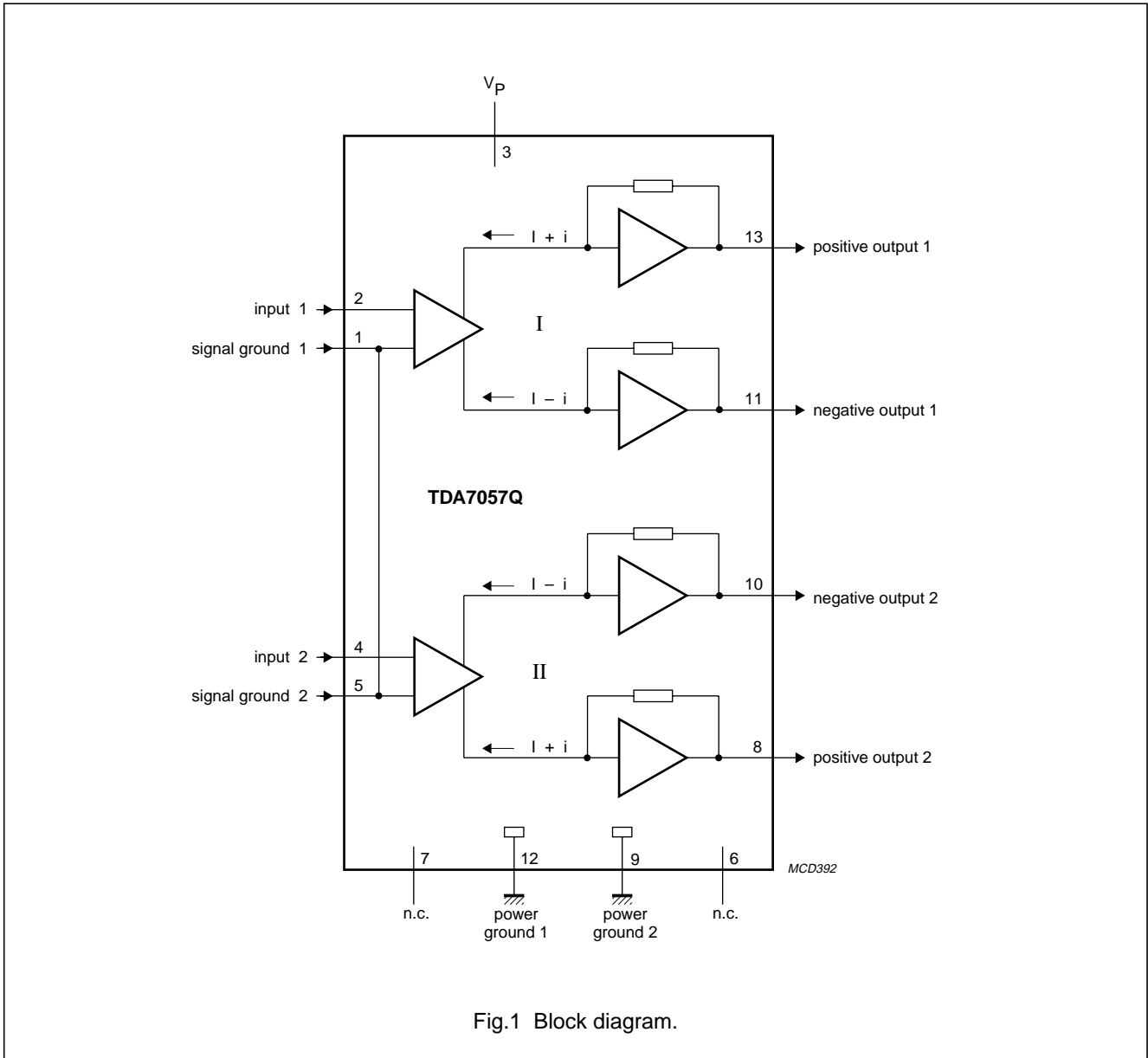


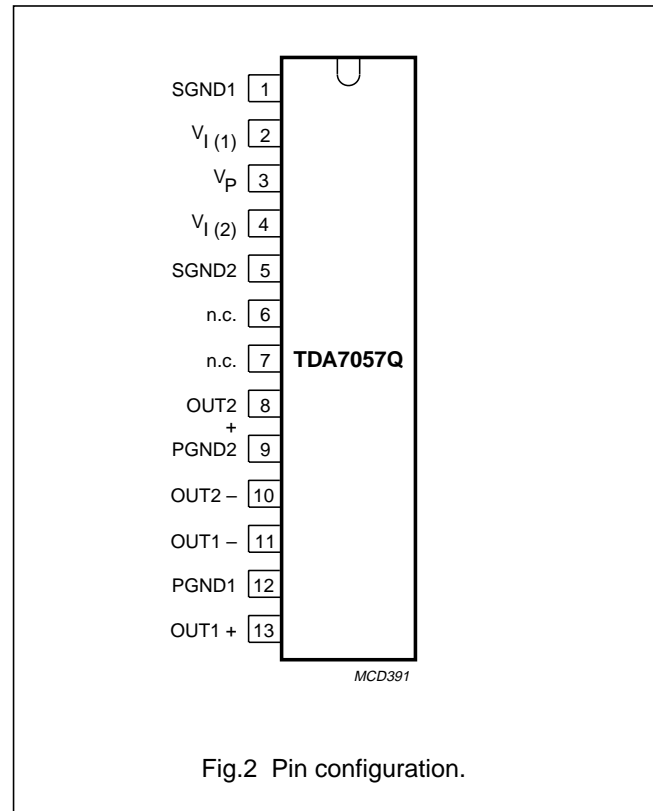
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
SGND1	1	signal ground 1
$V_{I(1)}$	2	voltage input 1
V_P	3	positive supply voltage
$V_{I(2)}$	4	voltage input 2
SGND2	5	signal ground 2
n.c.	6	not connected
n.c.	7	not connected
OUT2+	8	positive output 2
PGND2	9	power ground 2
OUT2-	10	negative output 2
OUT1-	11	negative output 1
PGND1	12	power ground 1
OUT1+	13	positive output 1



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FUNCTIONAL DESCRIPTION

The TDA7057Q is a stereo output amplifier, designed for battery-fed applications e.g. portable radios, but also suitable for mains fed applications. The gain is internally fixed at 40 dB.

For space reason there is a trend to decrease the number of battery cells. This means a decrease in supply voltage, resulting in a reduction of output power at conventional output stages. The latter is not preferred. Using the BTL principle increases the output power. The TDA7057Q can deliver an output power of 3 W in a speaker load of 16 Ω with 11 V supply.

The circuit is designed such that no external components are required. Special attention is given to switch-on and off clicks, low HF radiation and a good overall stability. The load can be short-circuited at all input conditions.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	positive supply voltage range		–	18	V
I_{ORM}	repetitive peak output current		–	1	A
I_{OSM}	non repetitive peak output current		–	1.5	A
P_{tot}	total power dissipation	$T_{case} < 60\text{ }^\circ\text{C}$	–	9	W
T_{stg}	storage temperature range		–55	+150	$^\circ\text{C}$
T_{vj}	virtual junction temperature		–	+150	$^\circ\text{C}$
T_{sc}	short-circuit time	see note 1	–	1	hr

Note to the limiting values

- The load can be short-circuited at all input conditions.

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient in free air	45 K/W
$R_{th\ j-c}$	from junction to case	8 K/W

Note to the thermal resistance

$V_P = 11\text{ V}$; $R_L = 16\ \Omega$; The maximum sine-wave dissipation is $= 3\text{ W}$; $T_{amb\ (max)} = 60\text{ }^\circ\text{C}$; $R_{th\ vj-a} = (150 - 60)/3 = 30\text{ K/W}$

$$R_{th\ vj-a} = R_{th\ vj-c} + R_{th\ c-HS} + R_{th\ HS}$$

$$R_{th\ c-HS} + R_{th\ HS} = 30 - 8 = 22\text{ K/W}$$

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CHARACTERISTICS $V_P = 11\text{ V}$; $f = 1\text{ kHz}$; $R_L = 16\ \Omega$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$; unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	positive supply voltage range		3.0	11	18	V
I_{ORM}	repetitive peak output current		–	–	0.6	A
Operating position						
I_P	total quiescent current	$R_L = \infty$; note 1	–	10	14	mA
P_O	output power	THD = 10%	2.5	3	–	W
THD	total harmonic distortion	$P_O = 0.5\text{ W}$	–	0.25	1	%
G_V	voltage gain		39	40	41	dB
$V_{\text{no(rms)}}$	noise output voltage (RMS value)	note 2	–	180	300	μV
$V_{\text{no(rms)}}$	noise output voltage (RMS value)	note 3	–	60	–	μV
B	bandwidth		–	20 Hz to 20 kHz	–	
SVRR	supply voltage ripple rejection	note 4	36	60	–	dB
$ V_{\text{off}} $	DC output offset voltage	$R_S = 5\text{ k}\Omega$	–	–	200	mV
Z_I	input impedance		–	100	–	$\text{k}\Omega$
I_{bias}	input bias current		–	100	300	nA
α	channel separation	$R_S = 5\text{ k}\Omega$	40	–	–	dB
$ G_V $	channel balance		–	–	1	dB

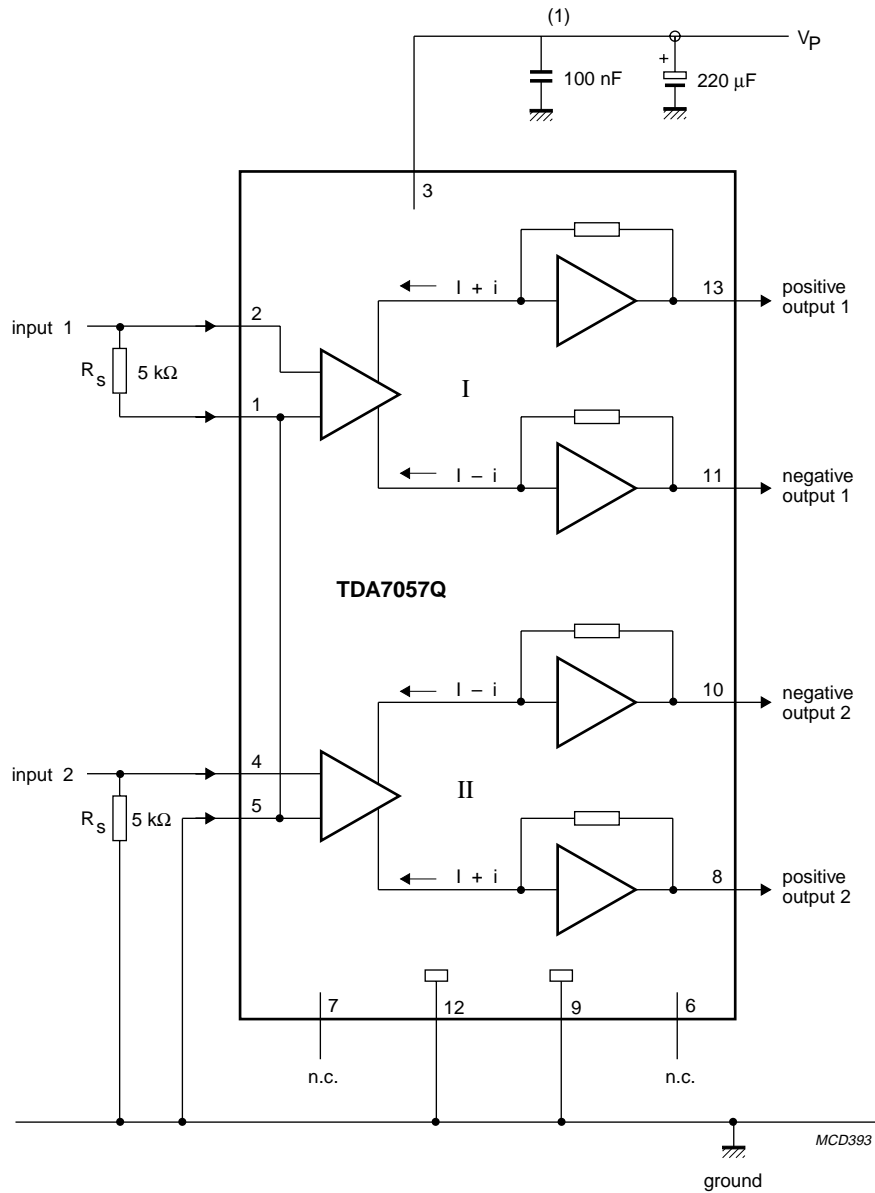
Notes to the characteristics

1. With a load connected to the outputs the quiescent current will increase, the maximum value of this increase being equal to the DC output offset voltage divided by R_L .
2. The noise output voltage (RMS value) is measured with $R_S = 5\text{ k}\Omega$ unweighted (20 Hz to 20 kHz).
3. The noise output voltage (RMS value) at $f = 500\text{ kHz}$ is measured with $R_S = 0\ \Omega$ and bandwidth = 5 kHz. With a practical load ($R_L = 16\ \Omega$, $L = 200\ \mu\text{H}$) the noise output current is only 50 nA.
4. The ripple rejection is measured with $R_S = 0\ \Omega$ and $f = 100\text{ Hz}$ to 10 kHz. The ripple voltage of 200 mV (RMS value) is applied to the positive supply rail.

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APPLICATION INFORMATION



(1) This capacitor can be omitted if the 220 μF electrolytic capacitor is connected close to pin 3.

Fig.3 Test and application diagram.

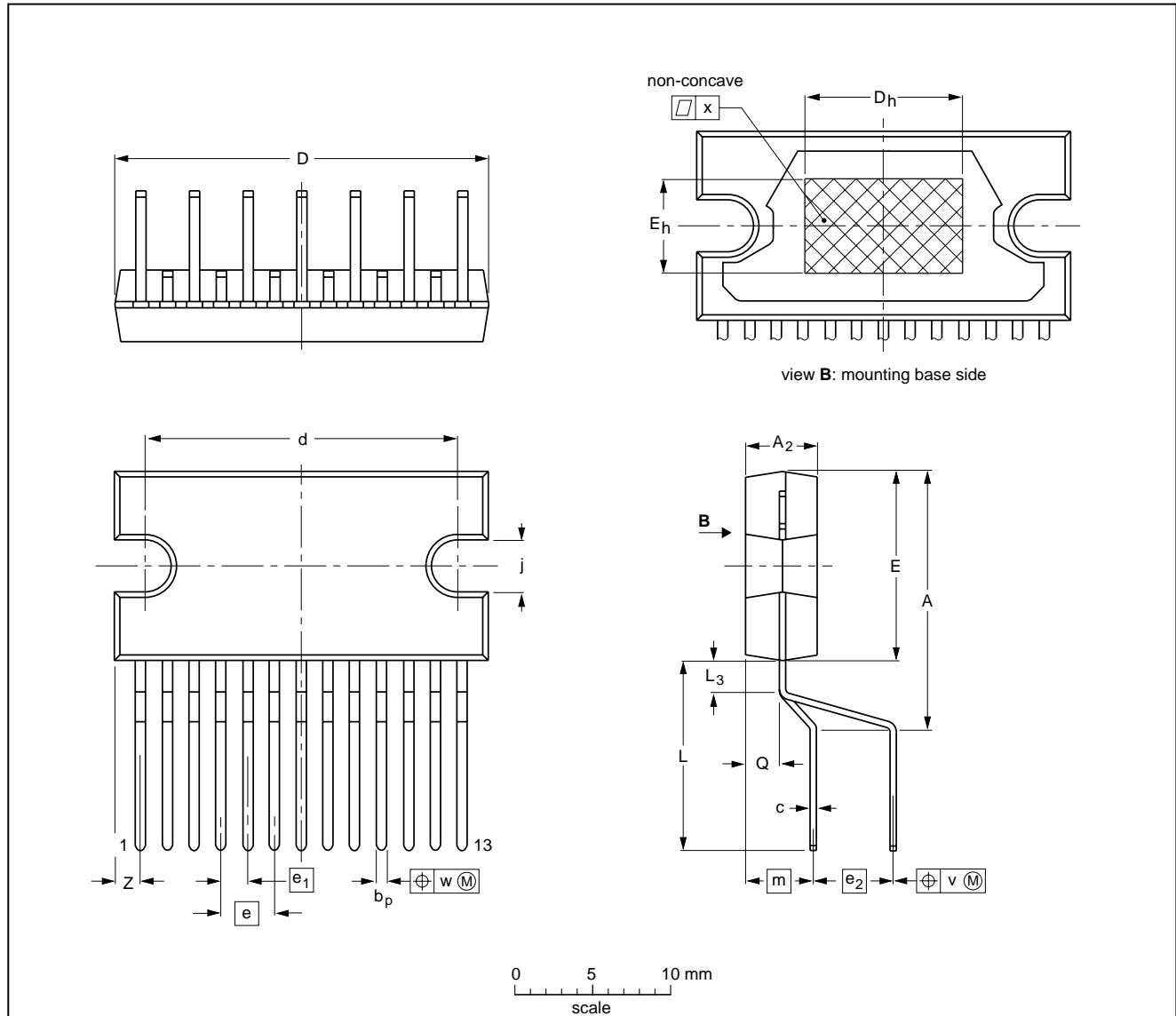
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PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 12 mm)

SOT141-6



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₂	b _p	c	D ⁽¹⁾	d	D _h	E ⁽¹⁾	e	e ₁	e ₂	E _h	j	L	L ₃	m	Q	v	w	x	Z ⁽¹⁾
mm	17.0 15.5	4.6 4.2	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	12.4 11.0	2.4 1.6	4.3	2.1 1.8	0.8	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT141-6					92-11-17 95-03-11

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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