



# TDA7439

## THREE BANDS DIGITALLY CONTROLLED AUDIO PROCESSOR

### 1 FEATURES

- INPUT MULTIPLEXER
  - 4 STEREO INPUTS
  - SELECTABLE INPUT GAIN FOR OPTIMAL ADAPTATION TO DIFFERENT SOURCES
- ONE STEREO OUTPUT
- TREBLE, MIDDLE AND BASS CONTROL IN 2.0dB STEPS
- VOLUME CONTROL IN 1.0dB STEPS
- TWO SPEAKER ATTENUATORS:
  - TWO INDEPENDENT SPEAKER CONTROL IN 1.0dB STEPS FOR BALANCE FACILITY
  - INDEPENDENT MUTE FUNCTION
- ALL FUNCTION ARE PROGRAMMABLE VIA SERIAL BUS

Figure 1. Package



Table 1. Order Codes

Part Number	Package
TDA7439	SDIP30

### 2 DESCRIPTION

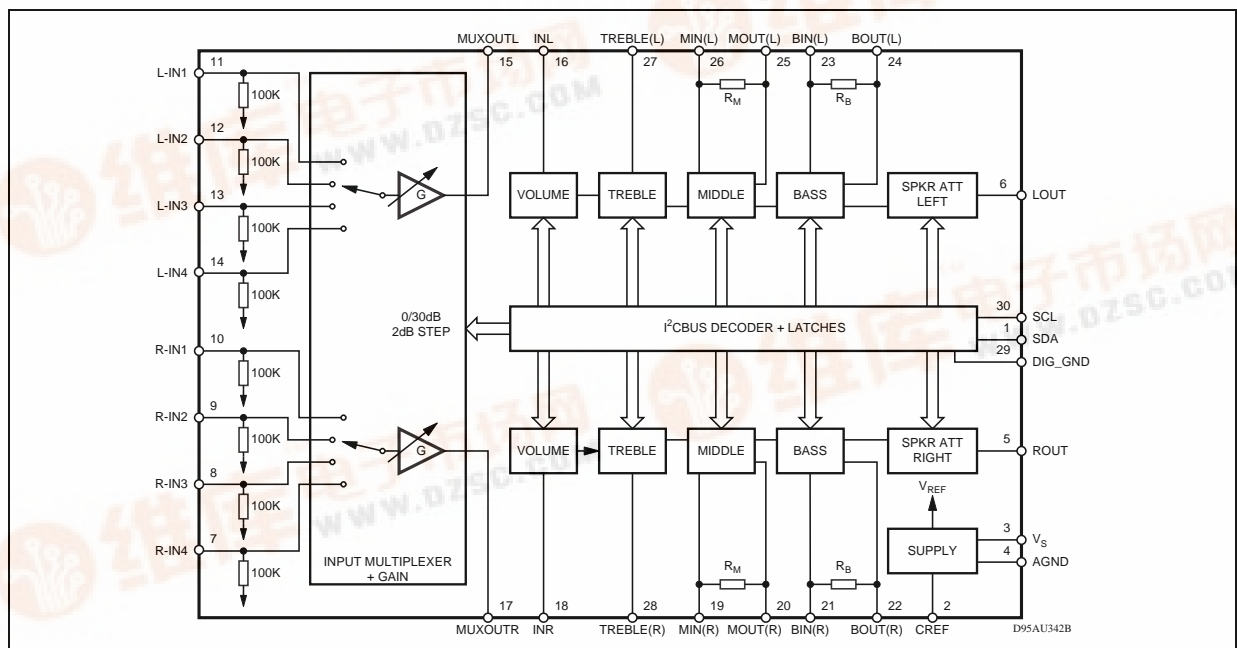
The TDA7439 is a volume tone (bass, middle and treble) balance (Left/Right) processor for quality

audio applications in car-radio and Hi-Fi systems. Selectable input gain is provided. Control of all the functions is accomplished by serial bus.

The AC signal setting is obtained by resistor networks and switches combined with operational amplifiers.

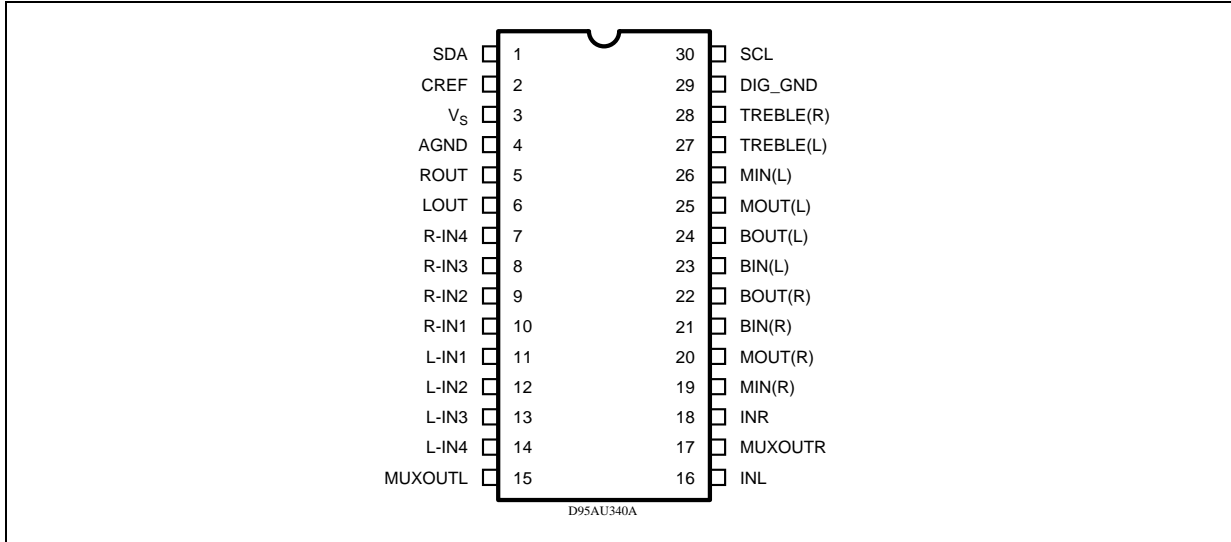
Thanks to the used BIPOLAR/CMOS Technology, Low Distortion, Low Noise and DC stepping are obtained

Figure 2. Block Diagram



# TDA7439

**Figure 3. PIN CONNECTION**



**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_S$	Operating Supply Voltage	10.5	V
$T_{amb}$	Operating Ambient Temperature	0 to 70	°C
$T_{stg}$	Storage Temperature Range	-55 to 150	°C

**Table 3. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{th\ j-pin}$	Thermal Resistance Junction-pins	85	°C/W

**Table 4. QUICK REFERENCE DATA**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_S$	Supply Voltage	6	9	10.2	V
$V_{CL}$	Max. input signal handling	2			Vrms
THD	Total Harmonic Distortion $V = 1V_{rms}$ $f = 1KHz$		0.01	0.1	%
S/N	Signal to Noise Ratio $V_{out} = 1V_{rms}$ (mode = OFF)		106		dB
$S_C$	Channel Separation $f = 1KHz$		90		dB
	Input Gain in (2dB step)	0		30	dB
	Volume Control (1dB step)	-47		0	dB
	Treble Control (2dB step)	-14		+14	dB
	Middle Control (2dB step)	-14		+14	dB
	Bass Control (2dB step)	-14		+14	dB
	Balance Control 1dB step	-79		0	dB
	Mute Attenuation		100		dB

**Table 5. Electrical Characteristics** (refer to the test circuit  $T_{amb} = 25^{\circ}\text{C}$ ,  $V_S = 9\text{V}$ ,  $R_L = 10\text{K}\Omega$ ,  $R_G = 600\Omega$ , all controls flat ( $G = 0\text{dB}$ ), unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
<b>SUPPLY</b>						
$V_S$	Supply Voltage		6	9	10.2	V
$I_S$	Supply Current		4	7	10	mA
SVR	Ripple Rejection		60	90		dB
<b>INPUT STAGE</b>						
$R_{IN}$	Input Resistance		70	100	130	$\text{K}\Omega$
$V_{CL}$	Clipping Level	THD = 0.3%	2	2.5		V <sub>rms</sub>
$S_{IN}$	Input Separation	The selected input is grounded through a $2.2\mu$ capacitor	80	100		dB
$G_{inmin}$	Minimum Input Gain		-1	0	1	dB
$G_{inmax}$	Maximum Input Gain		29	30	31	dB
$G_{step}$	Step Resolution		1.5	2	2.5	dB
<b>VOLUME CONTROL</b>						
$R_i$	Input Resistance		20	33	50	$\text{K}\Omega$
$C_{RANGE}$	Control Range		45	47	49	dB
$A_{VMAX}$	Max. Attenuation		45	47	49	dB
$A_{STEP}$	Step Resolution		0.5	1	1.5	dB
$E_A$	Attenuation Set Error	$A_V = 0$ to $-24\text{dB}$	-1.0	0	1.0	dB
		$A_V = -24$ to $-47\text{dB}$	-1.5	0	1.5	dB
$E_T$	Tracking Error	$A_V = 0$ to $-24\text{dB}$		0	1	dB
		$A_V = -24$ to $-47\text{dB}$		0	2	dB
$V_{DC}$	DC Step	adjacent attenuation steps from $0\text{dB}$ to $A_V$ max		0 0.5	3	mV mV
$A_{mute}$	Mute Attenuation		80	100		dB
<b>BASS CONTROL (1)</b>						
$G_b$	Control Range	Max. Boost/cut	$\pm 12.0$	$\pm 14.0$	$\pm 16.0$	dB
$B_{STEP}$	Step Resolution		1	2	3	dB
$R_B$	Internal Feedback Resistance		33	44	55	$\text{K}\Omega$
<b>TREBLE CONTROL (1)</b>						
$G_t$	Control Range	Max. Boost/cut	$\pm 13.0$	$\pm 14.0$	$\pm 15.0$	dB
$T_{STEP}$	Step Resolution		1	2	3	dB
<b>MIDDLE CONTROL (1)</b>						
$G_m$	Control Range	Max. Boost/cut	$\pm 12.0$	$\pm 14.0$	$\pm 16.0$	dB
$M_{STEP}$	Step Resolution		1	2	3	dB
$R_M$	Internal Feedback Resistance		18.75	25	31.25	$\text{K}\Omega$

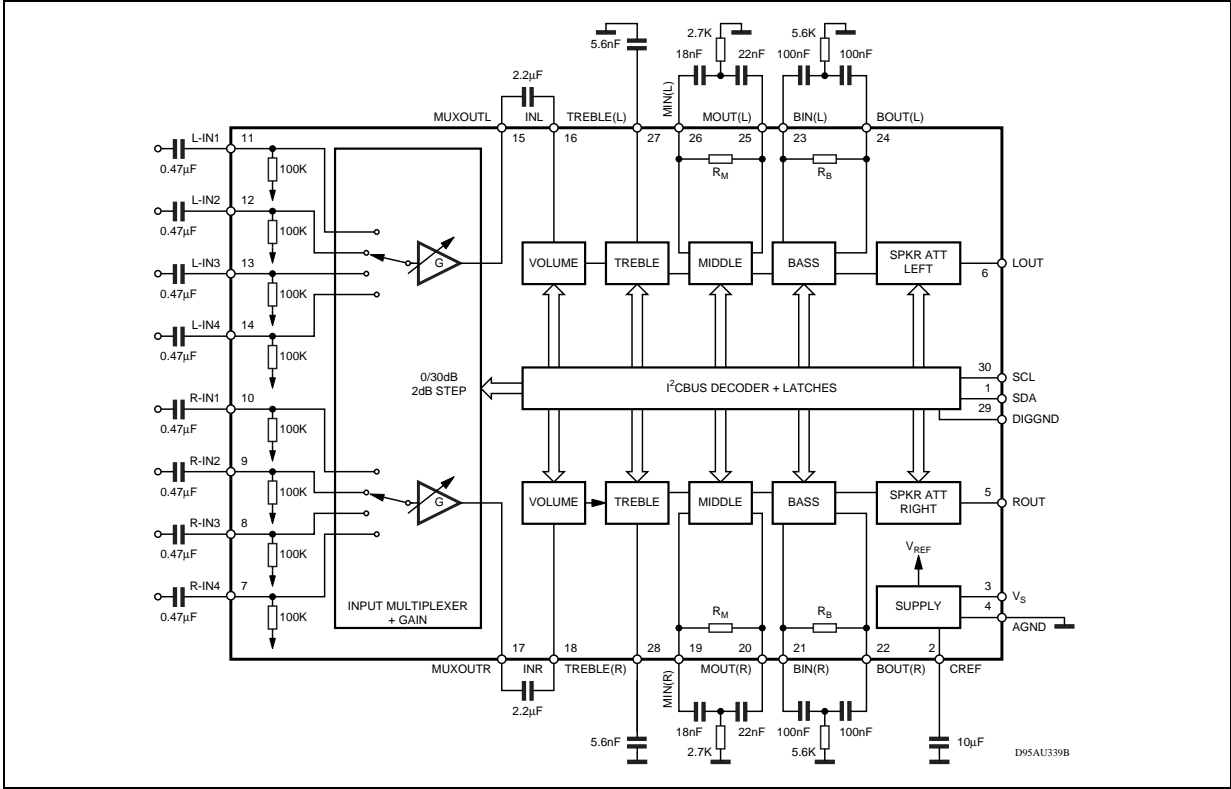
Table 5. Electrical Characteristics (continued)

SPEAKER ATTENUATORS						
C <sub>RANGE</sub>	Control Range		70	76	82	dB
S <sub>STEP</sub>	Step Resolution		0.5	1	1.5	dB
E <sub>A</sub>	Attenuation Set Error	A <sub>V</sub> = 0 to -20dB	-1.5	0	1.5	dB
		A <sub>V</sub> = -20 to -56dB	-2	0	2	dB
V <sub>DC</sub>	DC Step	adjacent attenuation steps		0	3	mV
A <sub>mute</sub>	Mute Attenuation		80	100		dB
AUDIO OUTPUTS						
V <sub>CLIP</sub>	Clipping Level	d = 0.3%	2.1	2.6		V <sub>RMS</sub>
R <sub>L</sub>	Output Load Resistance		2			KΩ
R <sub>O</sub>	Output Impedance		10	40	70	Ω
V <sub>DC</sub>	DC Voltage Level		3.5	3.8	4.1	V
GENERAL						
E <sub>NO</sub>	Output Noise	All gains = 0dB; BW = 20Hz to 20KHz flat		5	15	μV
E <sub>t</sub>	Total Tracking Error	A <sub>V</sub> = 0 to -24dB		0	1	dB
		A <sub>V</sub> = -24 to -47dB		0	2	dB
S/N	Signal to Noise Ratio	All gains 0dB; V <sub>O</sub> = 1V <sub>RMS</sub> ;	95	106		dB
S <sub>C</sub>	Channel Separation Left/Right		80	100		dB
d	Distortion	A <sub>V</sub> = 0; V <sub>I</sub> = 1V <sub>RMS</sub> ;		0.01	0.08	%
BUS INPUT						
V <sub>IL</sub>	Input Low Voltage				1	V
V <sub>IH</sub>	Input High Voltage		3			V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0.4V	-5	0	5	μA
V <sub>O</sub>	Output Voltage SDA Acknowledge	I <sub>O</sub> = 1.6mA		0.4	0.8	V

Notes: 1. The device is functionally good at V<sub>s</sub> = 5V. a step down, on V<sub>s</sub>, to 4V doesn't reset the device.

2. BASS, MIDDLE and TREBLE response: The center frequency and the response quality can be chosen by the external circuitry.

Figure 4. TEST CIRCUIT



**3 APPLICATION SUGGESTIONS**

The first and the last stages are volume control blocks. The control range is 0 to -47dB (mute) for the first one, 0 to -79dB (mute) for the last one.

Both of them have 1dB step resolution. The very high resolution allows the implementation of systems free from any noisy acoustical effect. The TDA7439 audioprocessor provides 3 bands tones control.

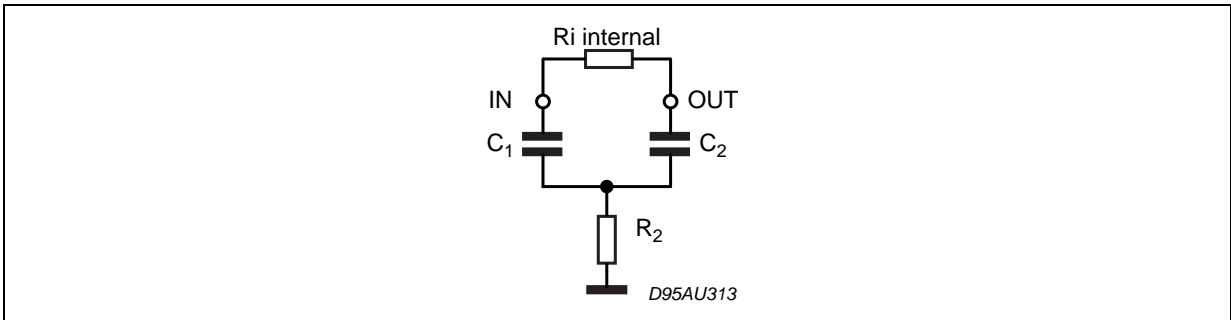
**3.1 Bass, Middle Stages**

The Bass and the middle cells have the same structure. The Bass cell has an internal resistor  $R_i = 44K\Omega$  typical.

The Middle cell has an internal resistor  $R_i = 25K\Omega$  typical.

Several filter types can be implemented, connecting external components to the Bass/Middle IN and OUT pins.

Figure 5.



The fig.5 refers to basic T Type Bandpass Filter starting from the filter component values (R1 internal and R2,C1,C2 external) the centre frequency  $F_c$ , the gain  $A_v$  at max. boost and the filter Q factor are computed as follows:

$$F_c = \frac{1}{2 \cdot \pi \cdot \sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}$$

$$A_v = \frac{R2C2 + R2C1 + RiC1}{R2C1 + R2C2}$$

$$Q = \frac{\sqrt{R1 \cdot R2 \cdot C1 \cdot C2}}{R2C1 + R2C2}$$

Viceversa, once  $F_c$ ,  $A_v$ , and  $R_i$  internal value are fixed, the external components values will be:

$$C1 = \frac{A_v - 1}{2 \cdot \pi \cdot F_c \cdot R_i \cdot Q} \qquad C2 = \frac{Q^2 \cdot C1}{A_v - 1 - Q^2}$$

$$R2 = \frac{A_v - 1 - Q^2}{2 \cdot \pi \cdot C1 \cdot F_c \cdot (A_v - 1) \cdot Q}$$

### 3.2 Treble Stage

The treble stage is a high pass filter whose time constant is fixed by an internal resistor (25KΩ typical) and an external capacitor connected between treble pins and ground Typical responses are reported in Figg. 10 to 13.

### 3.3 CREF

The suggested 10μF reference capacitor (CREF) value can be reduced to 4.7μF if the application requires faster power ON.

Figure 6. THD vs. frequency

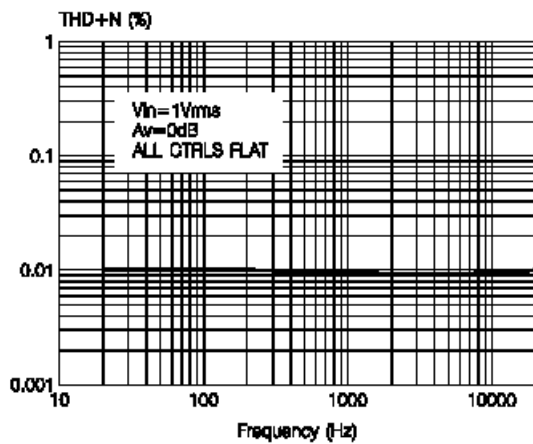


Figure 7. THD vs. RLOAD

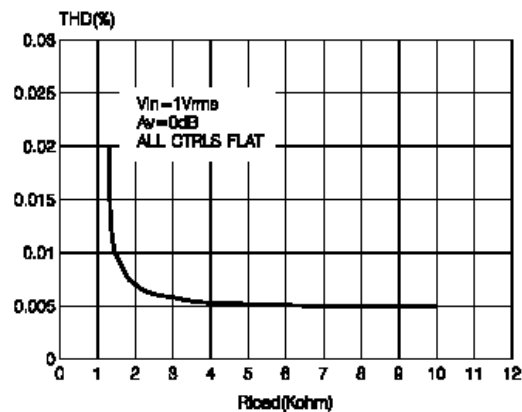


Figure 8. Channel separation vs. frequency

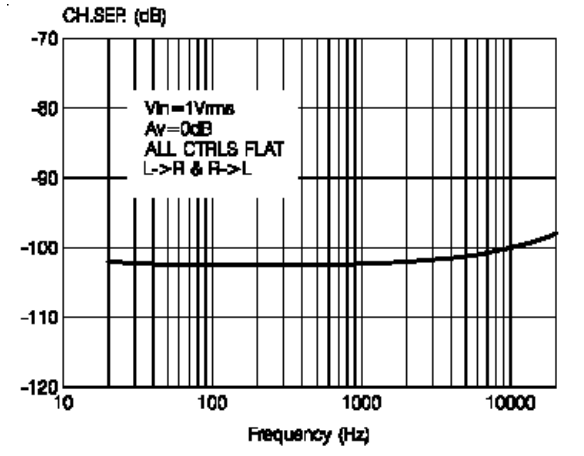


Figure 11. Middle response

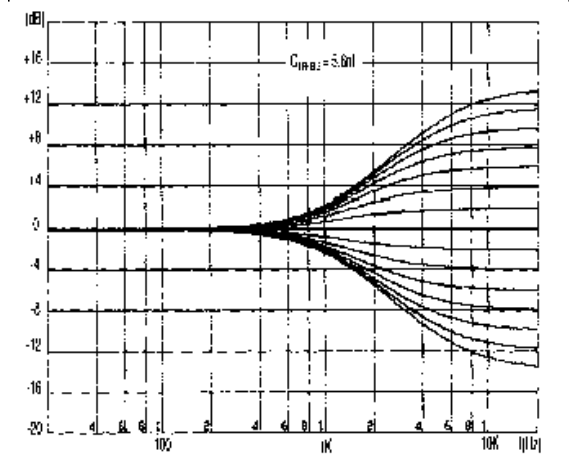


Figure 9. Bass response

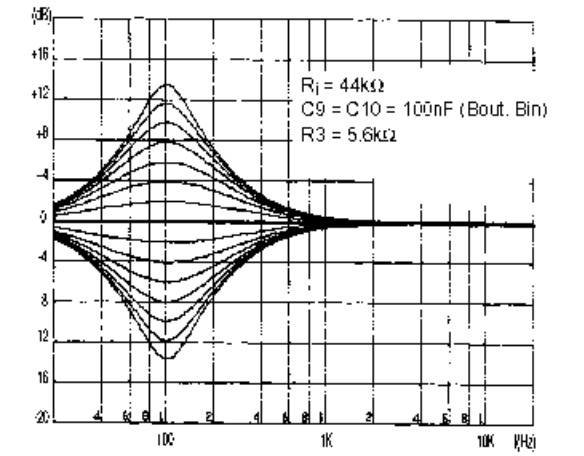


Figure 12. Typical tone response

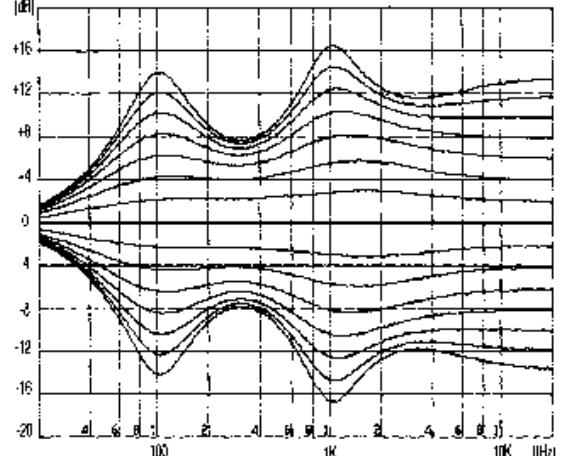
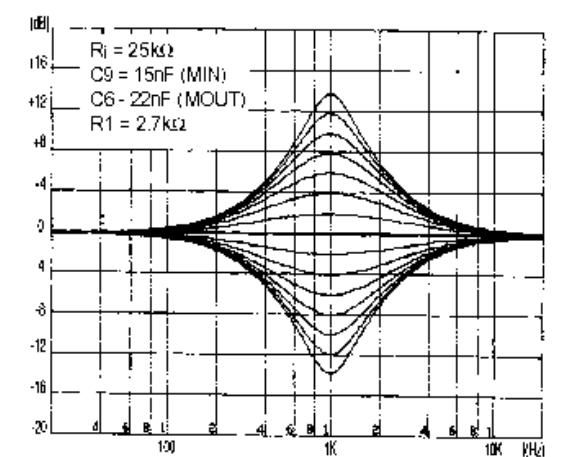


Figure 10. Treble response



## 4 I<sup>2</sup>C BUS INTERFACE

Data transmission from microprocessor to the TDA7439 and vice versa takes place through the 2 wires I<sup>2</sup>C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

### 4.1 Data Validity

As shown in fig. 13, the data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

### 4.2 Start and Stop Conditions

As shown in fig.14 a start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

### 4.3 Byte Format

Every byte transferred on the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

### 4.4 Acknowledge

The master ( $\mu$ P) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse (see fig. 15). The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during this clock pulse.

The audio processor which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at the HIGH level during the ninth clock pulse time. In this case the master transmitter can generate the STOP information in order to abort the transfer.

### 4.5 Transmission without Acknowledge

Avoiding to detect the acknowledge of the audio processor, the mP can use a simpler transmission: simply it waits one clock without checking the slave acknowledging, and sends the new data. This approach of course is less protected from misworking.

Figure 13. Data Validity on the I<sup>2</sup>CBUS

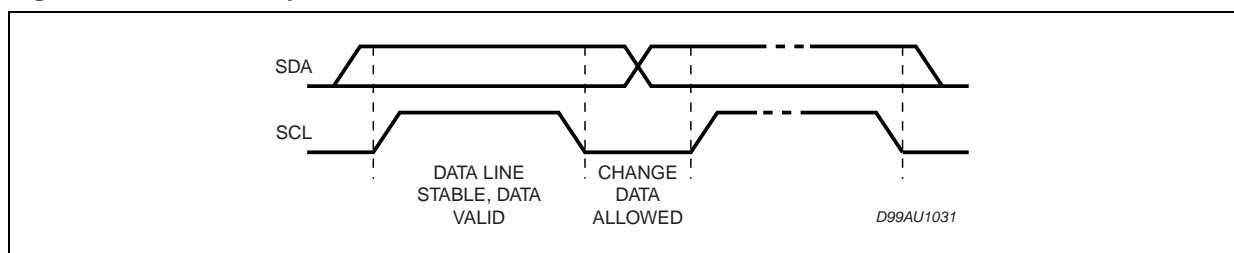


Figure 14.

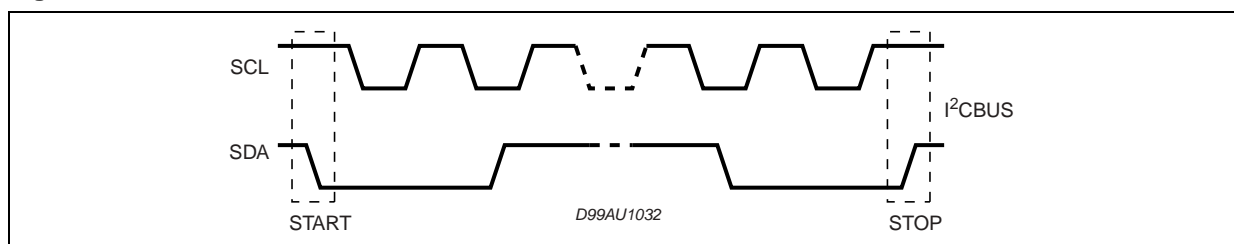
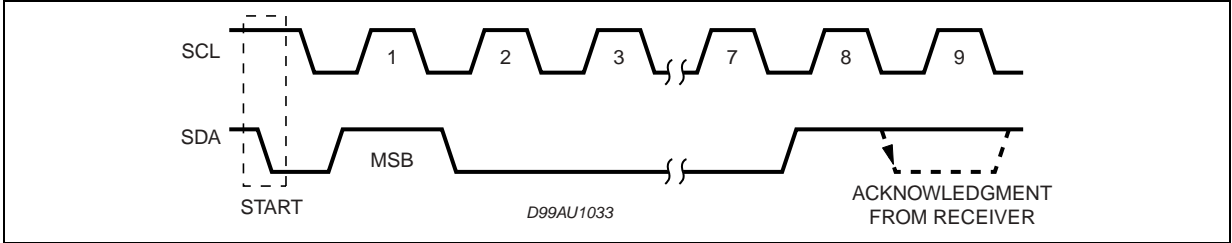




Figure 15.



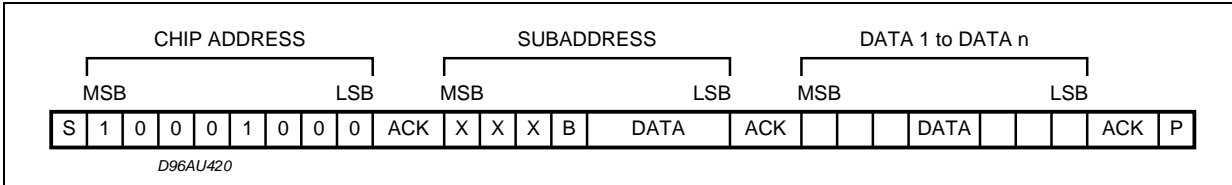
5 SOFTWARE SPECIFICATION

5.1 Interface Protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte, containing the TDA7439 address
- A subaddress bytes
- A sequence of data (N byte + acknowledge)
- A stop condition (P)

Figure 16.



ACK = Acknowledge

S = Start

P = Stop

A = Address

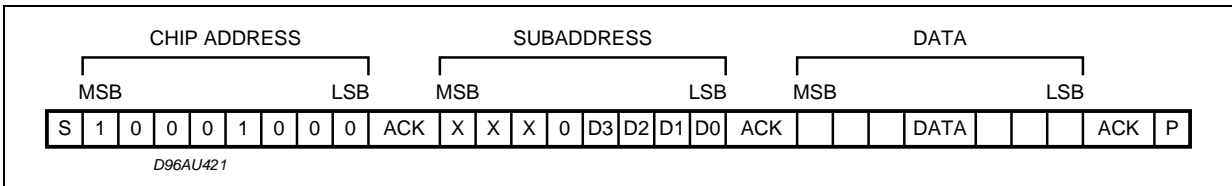
B = Auto Increment

6 EXAMPLES

6.1 No Incremental Bus

The TDA7439 receives a start condition, the correct chip address, a subaddress with the B = 0 (no incremental bus), N-data (all these data concern the subaddress selected), a stop condition.

Figure 17.

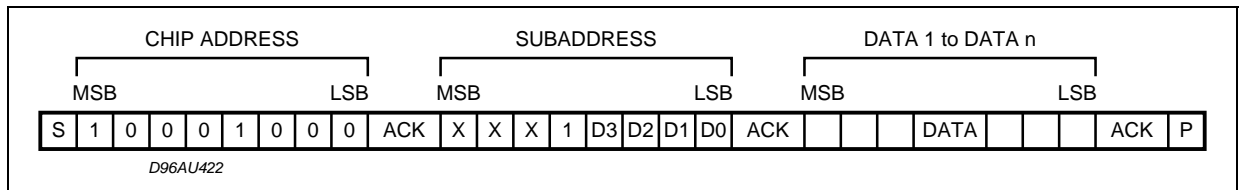


**6.2 Incremental Bus**

The TDA7439 receive a start conditions, the correct chip address, a subaddress with the B = 1 incremental bus): now it is in a loop condition with an autoincrease of the subaddress whereas SUBADDRESS from "XXX1000" to "XXX1111" of DATA are ignored.

The DATA 1 concern the subaddress sent, and the DATA 2 concern the subaddress sent plus one in the loop etc, and at the end it receives the stop condition.

**Figure 18.**



**Table 6. POWER ON RESET CONDITION**

INPUT SELECTION	IN2
INPUT GAIN	28dB
VOLUME	MUTE
BASS	0dB
MIDDLE	2dB
TREBLE	2dB
SPEAKER	MUTE

**7 DATA BYTES**

Address = 88 HEX (ADDR:OPEN).

**Figure 19. FUNCTION SELECTION: First byte (subaddress)**

MSB				LSB				SUBADDRESS
D7	D6	D5	D4	D3	D2	D1	D0	
X	X	X	B	0	0	0	0	INPUT SELECT
X	X	X	B	0	0	0	1	INPUT GAIN
X	X	X	B	0	0	1	0	VOLUME
X	X	X	B	0	0	1	1	BASS
X	X	X	B	0	1	0	0	MIDDLE
X	X	X	B	0	1	0	1	TREBLE
X	X	X	B	0	1	1	0	SPEAKER ATTENUATE "R"
X	X	X	B	0	1	1	1	SPEAKER ATTENUATE "L"

B = 1: INCREMENTAL BUS ACTIVE

B = 0: NO INCREMENTAL BUS

X = DON'T CARE

Table 7. INPUT SELECTION

MSB							LSB		INPUT MULTIPLEXER
D7	D6	D5	D4	D3	D2	D1	D0		
X	X	X	X	X	X	0	0	IN4	
X	X	X	X	X	X	0	1	IN3	
X	X	X	X	X	X	1	0	IN2	
X	X	X	X	X	X	1	1	IN1	

Table 8. INPUT GAIN SELECTION

MSB							LSB		INPUT GAIN
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS	
				0	0	0	0	0dB	
				0	0	0	1	2dB	
				0	0	1	0	4dB	
				0	0	1	1	6dB	
				0	1	0	0	8dB	
				0	1	0	1	10dB	
				0	1	1	0	12dB	
				0	1	1	1	14dB	
				1	0	0	0	16dB	
				1	0	0	1	18dB	
				1	0	1	0	20dB	
				1	0	1	1	22dB	
				1	1	0	0	24dB	
				1	1	0	1	26dB	
				1	1	1	0	28dB	
				1	1	1	1	30dB	

GAIN = 0 to 30dB

Table 9. VOLUME SELECTION

MSB					LSB			VOLUME
D7	D6	D5	D4	D3	D2	D1	D0	1dB STEPS
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	X	1	1	1	X	X	X	MUTE

VOLUME = 0 to 47dB/MUTE

Table 10. BASS SELECTION

MSB					LSB			BASS
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 11. MIDDLE SELECTION

MSB							LSB	MIDDLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 12. TREBLE SELECTION

MSB							LSB	TREBLE
D7	D6	D5	D4	D3	D2	D1	D0	2dB STEPS
				0	0	0	0	-14dB
				0	0	0	1	-12dB
				0	0	1	0	-10dB
				0	0	1	1	-8dB
				0	1	0	0	-6dB
				0	1	0	1	-4dB
				0	1	1	0	-2dB
				0	1	1	1	0dB
				1	1	1	1	0dB
				1	1	1	0	2dB
				1	1	0	1	4dB
				1	1	0	0	6dB
				1	0	1	1	8dB
				1	0	1	0	10dB
				1	0	0	1	12dB
				1	0	0	0	14dB

Table 13. SPEAKER ATTENUATE SELECTION

MSB					LSB			SPEAKER ATTENUATION
D7	D6	D5	D4	D3	D2	D1	D0	1dB
					0	0	0	0dB
					0	0	1	-1dB
					0	1	0	-2dB
					0	1	1	-3dB
					1	0	0	-4dB
					1	0	1	-5dB
					1	1	0	-6dB
					1	1	1	-7dB
	0	0	0	0				0dB
	0	0	0	1				-8dB
	0	0	1	0				-16dB
	0	0	1	1				-24dB
	0	1	0	0				-32dB
	0	1	0	1				-40dB
	0	1	1	0				-48dB
	0	1	1	1				-56dB
	1	0	0	0				-64dB
	1	0	0	1				-72dB
	1	1	1	1	X	X	X	MUTE

SPEAKER ATTENUATION = 0 to -79dB/MUTE

Figure 20. PINS: 2

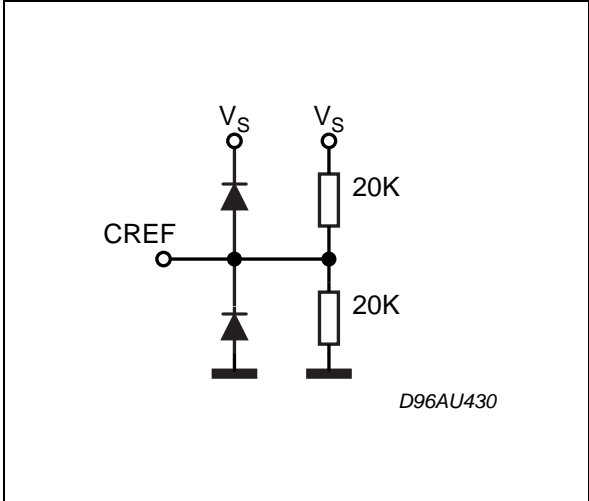


Figure 23. PINS 15, 17

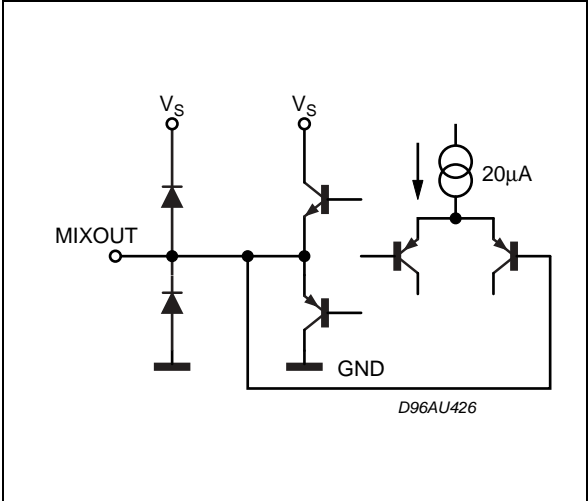


Figure 21. PINS: 5, 6

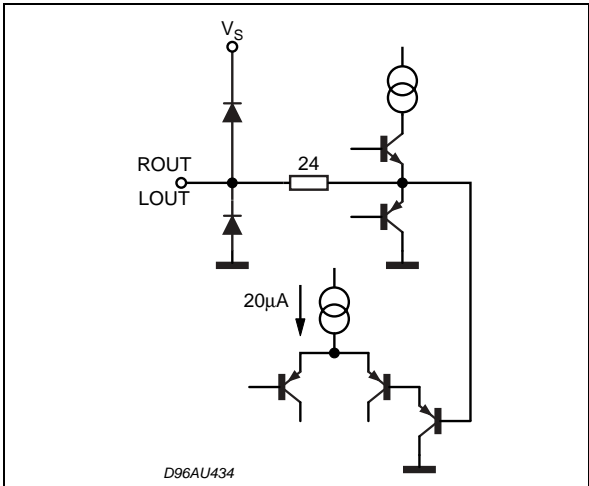


Figure 24. PINS 16, 18

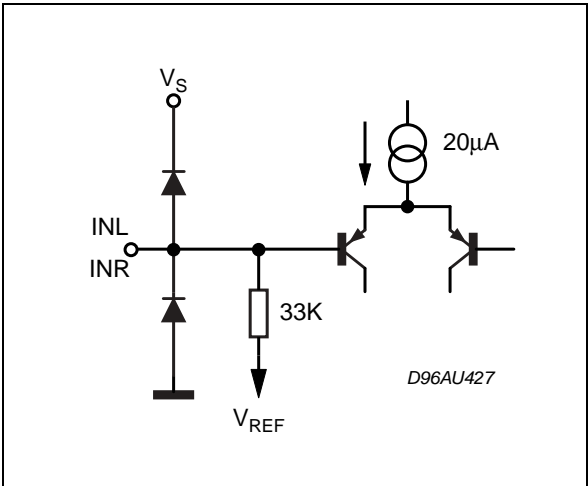


Figure 22. PINS 7, 8, 9, 10, 11, 12, 13, 14

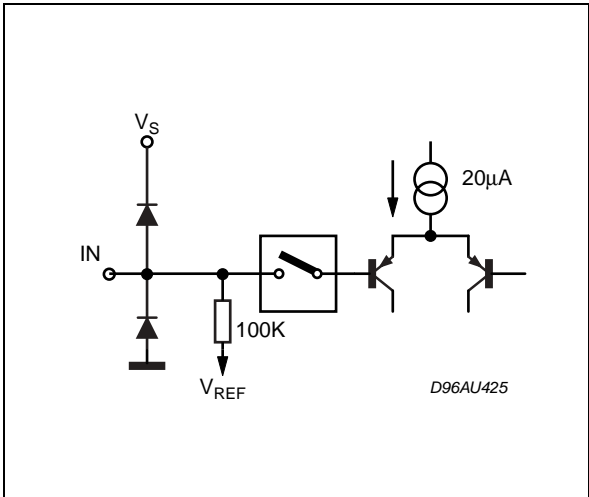


Figure 25. PINS 20, 25

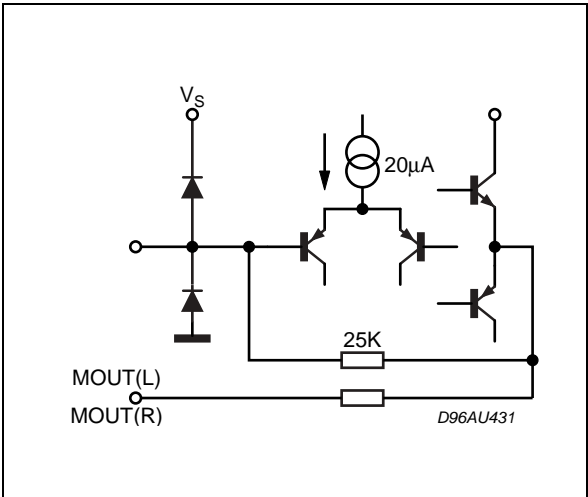


Figure 26. PINS 19,26

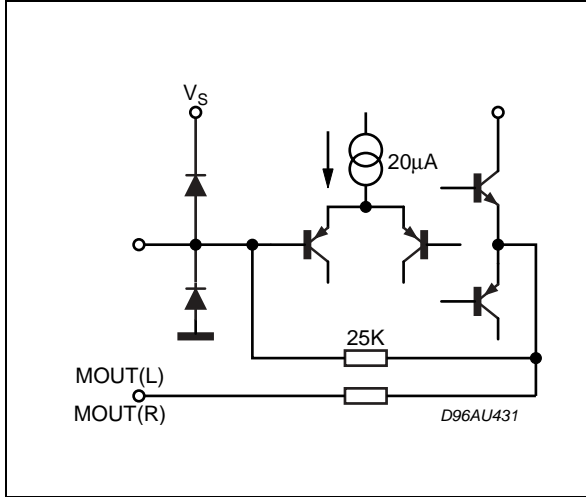


Figure 29. PINS 27, 28

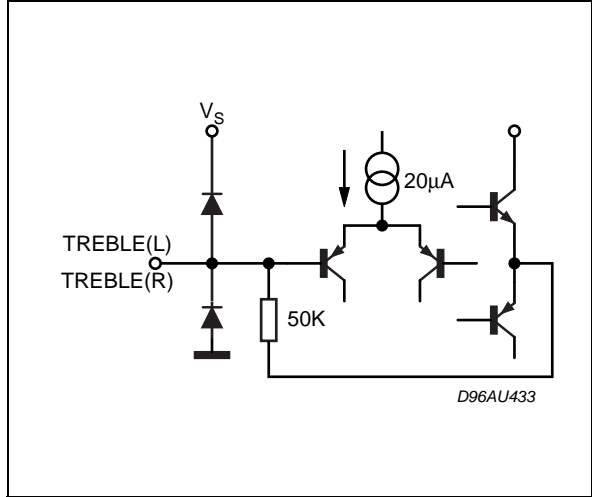


Figure 27. PINS 21, 23

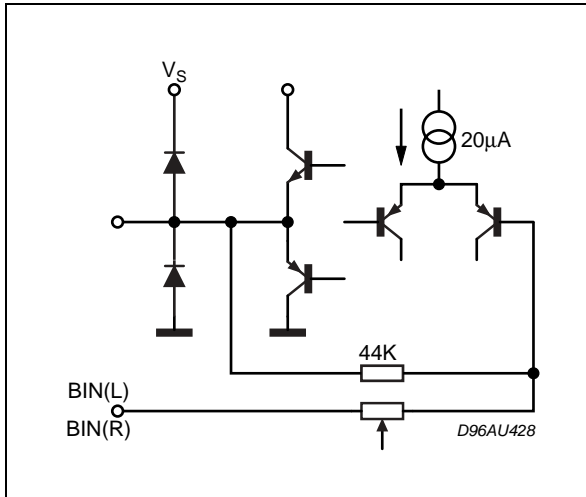


Figure 30. PIN 30

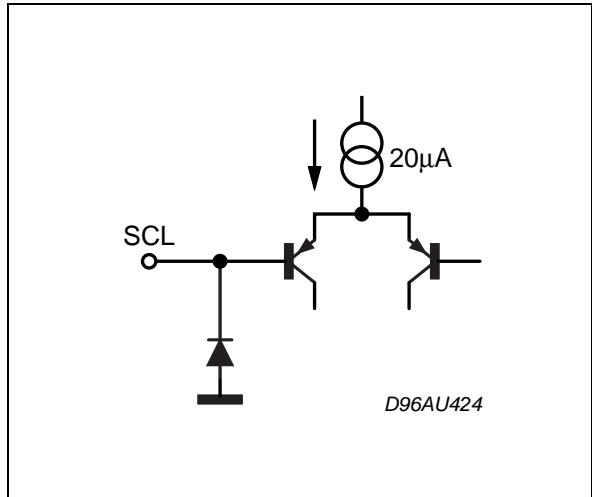


Figure 28. PINS 22, 24

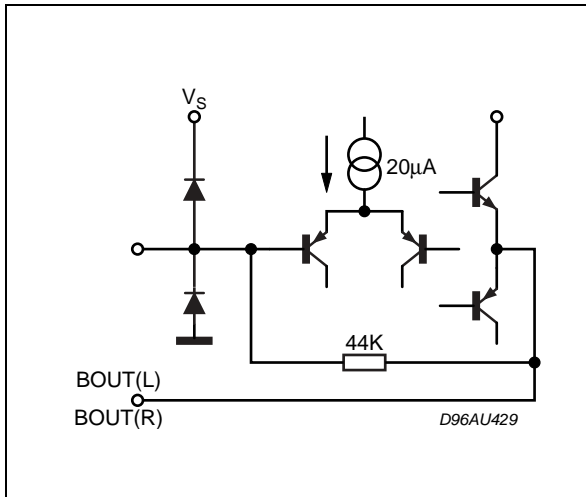


Figure 31. PIN 1

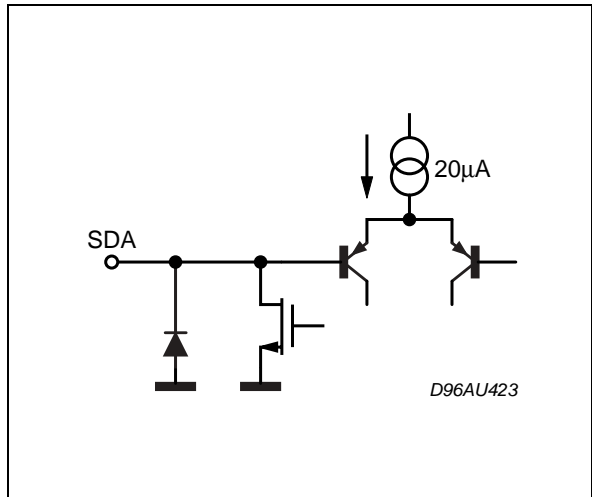
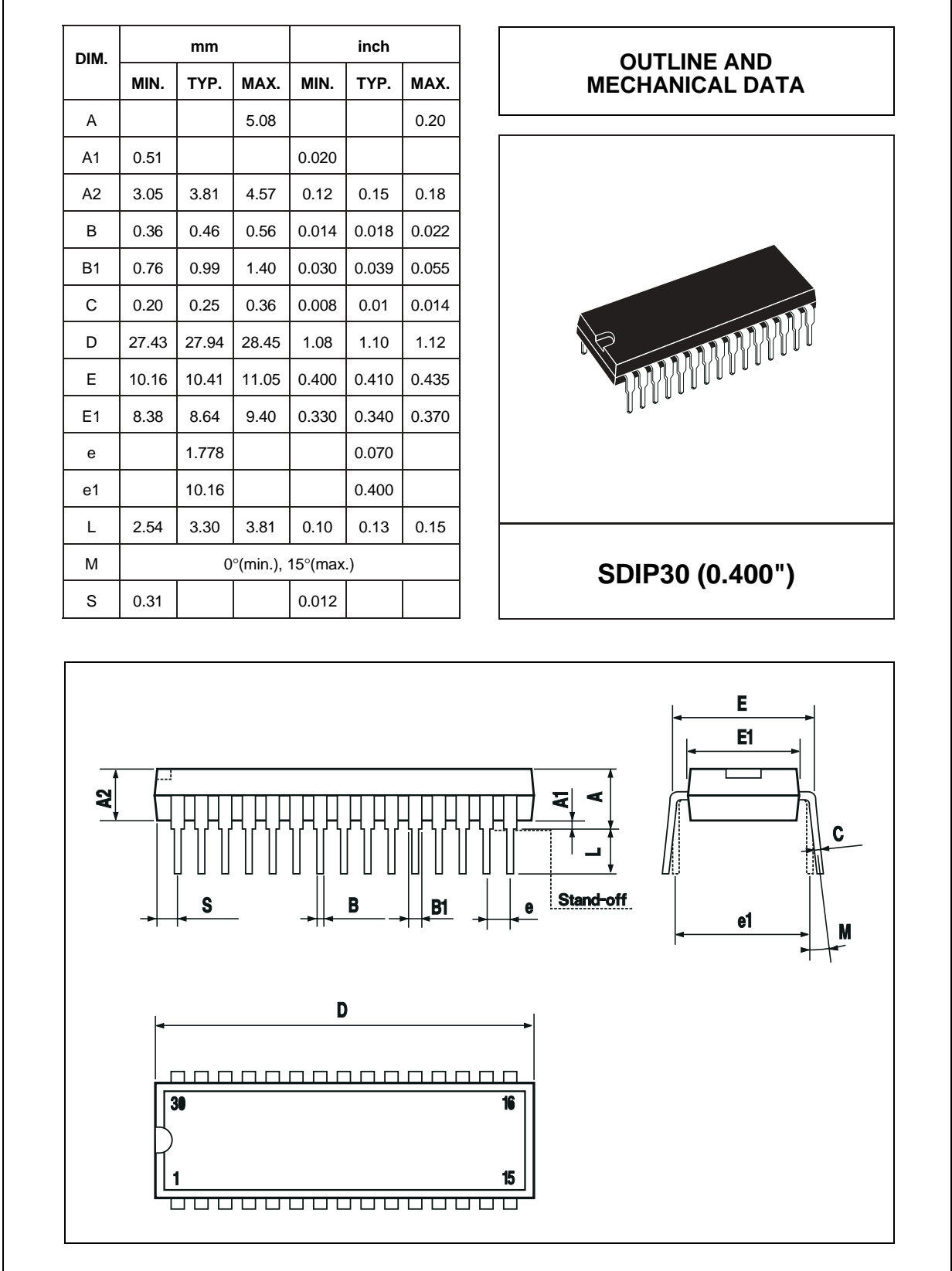




Figure 32. SDIP30 Mechanical Data & Package Dimensions



**Table 14. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
January 2004	9	First Issue in EDOCS DMS
June 2004	10	Changed the Style-sheet in compliance to the new "Corporate Technical Publications Design Guide"

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