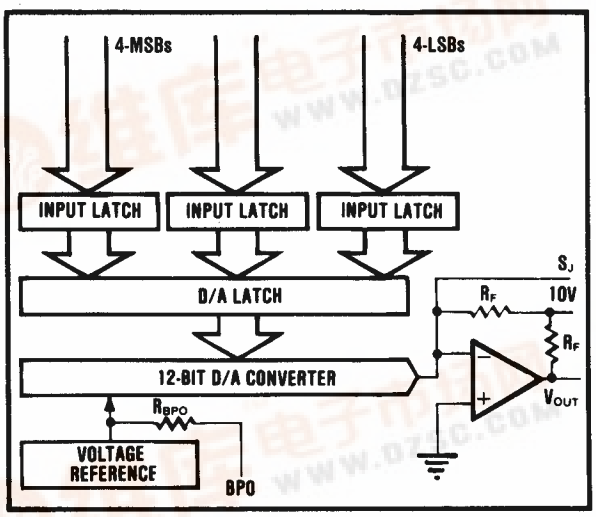
BURR-BROWN®

DAC1201KP-V

Monolithic Microprocessor-Compatible 12-Bit Resolution DIGITAL-TO-ANALOG CONVERTER

FEATURES

- COMPLETE D/A CONVERTER:
  INTERNAL REFERENCE
  ±10V OUTPUT OPERATIONAL AMPLIFIER
- MICROPROCESSOR INTERFACE LOGIC FOR A 4-, 8-, 12- OR 16-BIT BUS
- MONOTONICITY GUARANTEED 0°C to +70°C
- SETTLING TIME 7μs, MAX
- ±12V to ±15V POWER SUPPLY OPERATION
- 28-PIN MOLDED PLASTIC DIP
- LOWEST COST BUFFERED 12-BIT DAC



DESCRIPTION

The low price of DAC1201KP makes this 12-bit resolution D/A converter the best value available for commercial applications requiring a microprocessor interface.

The DAC1201 features microprocessor interface logic, TTL input compatibility, guaranteed monotonicity over 0°C to +70°C and settling time of 7μs maximum.

The interface logic is partitioned in 4-bit nibbles permitting 4-, 8-, 12- and 16-bit bus interface connections for right- or left-justified input words. Dual rank latches permit flexible timing operations for microprocessor control of the DAC1201.

This precision component is made possible using Burr-Brown's proprietary monolithic integrated circuit process which has been optimized for converter circuits. A stable subsurface reference zener, laser-trimmed thin-film ladder resistors, and high speed current switches combine to give superior performance over the rated temperature range.

DAC1201 is priced and specified for applications where high resolution and monotonocity are the key application parameters and where tightly specified performance over temperature is not required. Because of the low price, it is feasible to use this 12-bit D/A converter for new applications in communications systems, electronic controllers, medical instrumentation, electronic games and personal computer peripherals.

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SPECIFICATIONS

ELECTRICAL

Typical at +25°C and $\pm V_{CC}$ = 12V or 15V, V_{DD} = +5V unless otherwise noted.

MODEL	DAC1201KP-V	UNITS
INPUTS		
DIGITAL INPUTS		
Input Code[1]	USB, BOB	
Resolution	12	Bits
Digital Logic Inputs[2]:		
V_{IH}, min to max	+2.4 to $+V_{CC}$	V
V_{IL}, min to max	0 to +0.8	V
I_{IH}, V_I = +2.7V, max	+20	μA
I_{IL}, V_I = +0.4V, max	±30	μA
TRANSFER CHARACTERISTICS		
ACCURACY		
Linearity Error, max[3]	±0.018	% of FSR[4]
Differential Linearity Error, max	±0.024	% of FSR
Gain Error, max[5][6]	±0.3	%
Unipolar Offset Error[5][7]	±20	mV
Bipolar Offset Error, max[5][8]	±40	mV
Monotonicity Over 0°C to +70°C[9]	12	Bits
Sensitivity of Gain to Power Supply Variations:		
$+V_{CC}$ and $-V_{CC}$	±0.002	% of FSR/%V_{CC}
V_{DD}	±0.006	% of FSR/%V_{DD}
TEMPERATURE COEFFICIENTS		
Gain	±10	ppm/°C
Bipolar Zero[10]	±6	ppm of FSR/°C
SETTLING TIME (to ±0.012% of FSR)[11]		
20V step and 2kΩ load, max	7	μs
OUTPUT		
ANALOG OUTPUT		
Voltage Range, min[12]	±5, ±10, +10	V
Current, min[13]	±5	mA
Impedance	0.2	Ω
REFERENCE OUTPUT		
Voltage[14]	+6.3	V
Source Current Available for External Loads, max	+1.5	mA
Temperature Coefficient	±10	ppm/°C
POWER SUPPLY REQUIREMENTS		
RATED VOLTAGE		
$+V_{CC}/-V_{CC}$[15][16]	+15/−15	V
V_{DD}[17]	+5	V
CURRENT (no load), max[18]		
$+V_{CC}/-V_{CC}$	+25/−35	mA
V_{DD}	+15	mA
TEMPERATURE RANGE		
For parameters specified over temp, min to max	0 to +70	°C
Storage, min to max	−60 to +100	°C

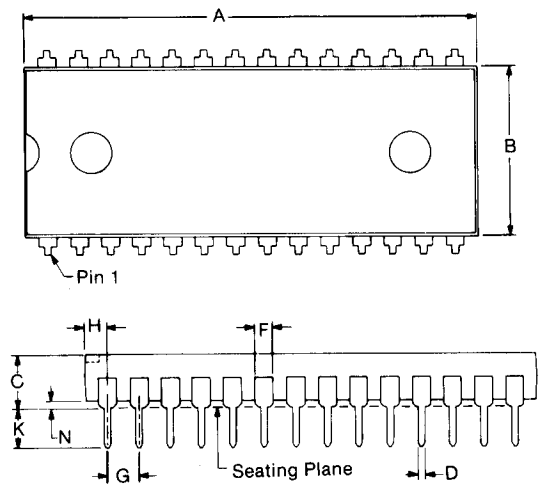
NOTES: (1) USB = Unipolar Straight Binary, BOB = Bipolar Offset Binary. (2) Digital inputs are TTL-compatible for V_{DD} over the range of +4.5V to 5.5V. Digital input specs are guaranteed over 0°C to +70°C. The specs are tested at 25°C only. (3) ±0.018% of FSR is 3/4LSB for 12 bits. (4) FSR means Full-Scale Range and is 20V for a ±10V range. (5) Adjustable to zero with external potentiometer. (6) Adjusting the Gain Adjust potentiometer rotates the transfer function about 0V for unipolar operation and about minus full scale (−FS) for bipolar operation. (7) Error at input code 000_H for unipolar operation (output at 0V). (8) Error at input code 000_H for bipolar operation (output at minus full scale, −FS). (9) Guaranteed. Tested at 25°C only. (10) Drift at 0V output for bipolar operation (input code 100_H). (11) Guaranteed. Not tested. (12) Minimum supply voltage required for ±10V output swing ±13.5V. Output swing for ±11.4V supplies is at least −8V to +8V. (13) Output may be indefinitely shorted to Common without damage. (14) Tolerance is ±5%. (15) The maximum voltage separation between $+V_{CC}$ and $-V_{CC}$ is 36V. (16) Range of operation is ±11.4V to ±16.5V. (17) Range of operation is +4.5V to +5.5V. (18) Typical power supply currents are approximately 70% of the maximum.

ABSOLUTE MAXIMUM RATINGS

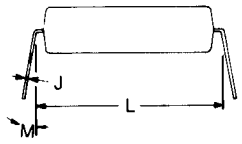
$+V_{CC}$ to ACOM	0 to +18V
$-V_{CC}$ to ACOM	0 to −18V
V_{DD} to DCOM	0 to +7V
V_{DD} to ACOM	±7V
ACOM to DCOM	±7V
Digital Inputs (pins 2-14, 16-19) to DCOM	−0.4V to +18V
External Voltage Applied to 10V Range Resistor	±12V
REF OUT	Indefinite short to ACOM
External Voltage Applied to Analog Output	−5V to +5V
Power Dissipation	1000mW
Operating Temperature	0°C to +70°C
Storage Temperature	−60°C to +100°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

MECHANICAL



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.400	1.460	35.56	37.08
B	.530	.575	13.46	13.67
C	.169	.224	4.29	5.70
D	.015	.023	0.38	0.58
F	.043	.065	1.09	1.65
G	.100 BASIC		2.54 BASIC	
H	.030	.090	0.76	2.29
J	.008	.015	0.20	0.38
K	.100	.136	2.54	3.46
L	.600 BASIC		15.24 BASIC	
M	0°	15°	0°	15°
N	.018	.022	0.46	0.56



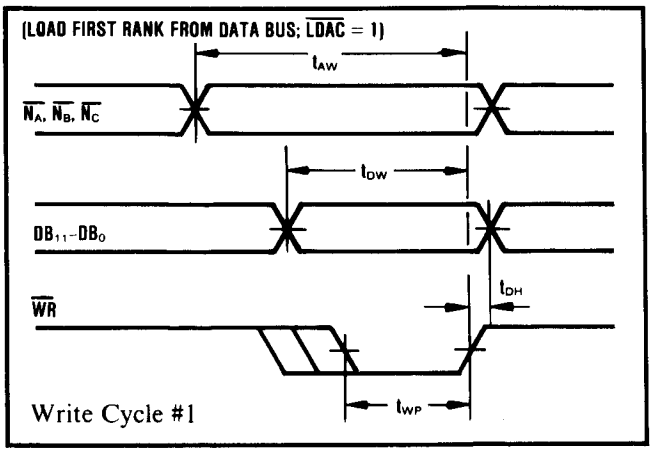
NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

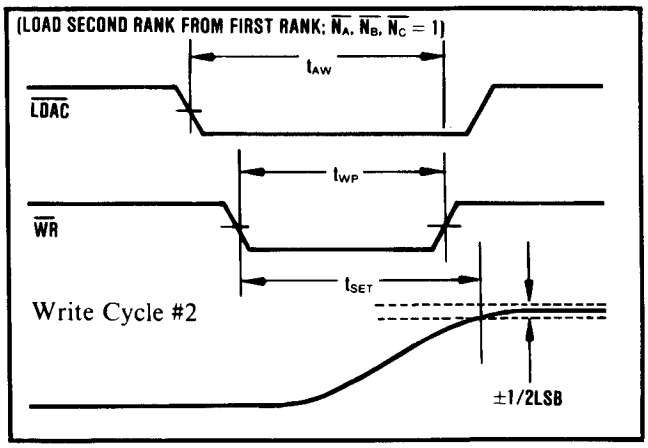
CASE: Plastic

MATING CONNECTOR: 2803MC

WEIGHT: 4.3gm (0.15oz)

TIMING DIAGRAMS





Digital Interface Timing Over Temperature Range:

t_{WP}, $\overline{WR}$ pulse width, min 50ns
$t_{AW}1$, $\overline{N_X}$ and $\overline{LDAC}$ valid to end of $\overline{WR}$, min 50ns
t_{DW}, data valid to end of $\overline{WR}$, min 80ns
t_{DH}, data valid hold time, min 0ns

PIN NOMENCLATURE

PIN	NAME	FUNCTION
1	V_{DD}	Logic Supply, +5V
2	$\overline{WR}$	WRITE, command signal to load latches. Logic low loads latches.
3	$\overline{LDAC}$	LOAD D/A CONVERTER, enables $\overline{WR}$ to load the D/A latch. Logic low enables.
4	$\overline{N_A}$	NYBBLE A, enables $\overline{WR}$ to load input latch A (the most significant nybble. Logic low enables.
5	$\overline{N_B}$	NYBBLE B, enables $\overline{WR}$ to load input latch B. Logic low enables.
6	$\overline{N_C}$	NYBBLE C, enables $\overline{WR}$ to load input latch C (the least significant nybble). Logic low enables.
7	D_{11}	DATA, Bit 12, MSB, positive true.
8	D_{10}	DATA, Bit 11
9	D_9	DATA, Bit 10
10	D_8	DATA, Bit 9
11	D_7	DATA, Bit 8
12	D_6	DATA, Bit 7
13	D_5	DATA, Bit 6
14	D_4	DATA, Bit 5
15	DCOM	DIGITAL COMMON, V_{DD} supply return
16	D_0	DATA, Bit 1, LSB
17	D_1	DATA, Bit 2
18	D_2	DATA, Bit 3
19	D_3	DATA, Bit 4
20	$+V_{CC}$	Analog Supply Input, +15V or +12V
21	$-V_{CC}$	Analog Supply Input, −15V or −12V
22	GAIN ADJ	To externally adjust gain
23	ACOM	ANALOG COMMON, $\pm V_{CC}$ supply return
24	V_{out}	D/A converter voltage output
25	10V RANGE	Connect to pin 24 for 10V Range
26	SJ	SUMMING JUNCTION of output amplifier
27	BPO	BIPOLAR OFFSET. Connect to pin 26 for Bipolar Operation
28	REF OUT	6.3V reference output

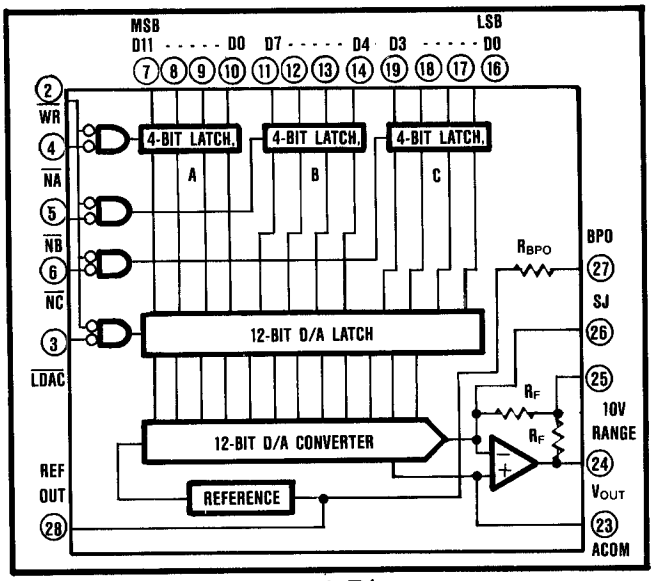


FIGURE 1. DAC1201 Block Diagram.

OPERATION

INTERFACE LOGIC

Input latches A, B, and C hold data temporarily while a complete 12-bit word is assembled before loading into the D/A register. This double-buffered organization prevents the generation of spurious analog output values. Each register is independently addressable.

These input latches are controlled by $\overline{N_A}$, $\overline{N_B}$, $\overline{N_C}$ and $\overline{WR}$. $\overline{N_A}$, $\overline{N_B}$, and $\overline{N_C}$ are internally NORed with $\overline{WR}$ so that the input latches transmit data when both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ are at logic "0". When either $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) or $\overline{WR}$ go to logic "1", the input data is latched into the input registers and held until both $\overline{N_A}$ (or $\overline{N_B}$, $\overline{N_C}$) and $\overline{WR}$ go to logic "0".

The D/A latch is controlled by $\overline{LDAC}$ and $\overline{WR}$. $\overline{LDAC}$ and $\overline{WR}$ are internally NORed so that the latches

transmit data to the D/A switches when both $\overline{LDAC}$ and $\overline{WR}$ are at logic "0". When either $\overline{LDAC}$ or $\overline{WR}$ are at logic "1", the data is latched in the D/A latch and held until $\overline{LDAC}$ and $\overline{WR}$ go to logic "0".

All latches are level-triggered. Data present when the control signals are logic "0" will enter the latch. When any one of the control signals returns to logic "1", the data is latched. A truth table for all latches is given in Table I.

TABLE I. DAC1201 Interface Logic Truth Table.

WR	N_A	N_B	N_C	LDAC	Operation
1	X	X	X	X	No Operation
0	0	1	1	1	Enables Input Latch 4MSBs
0	1	0	1	1	Enables Input Latch 4 Middle Bits
0	1	1	0	1	Enables Input Latch 4LSBs
0	1	1	1	0	Loads D/A Latch From Input Latches
0	0	0	0	0	All Latches Transparent

"X" = Don't Care.

GAIN AND OFFSET ADJUSTMENTS

Figures 2 and 3 illustrate the relationship of Offset and Gain adjustments to unipolar and bipolar D/A converter output.

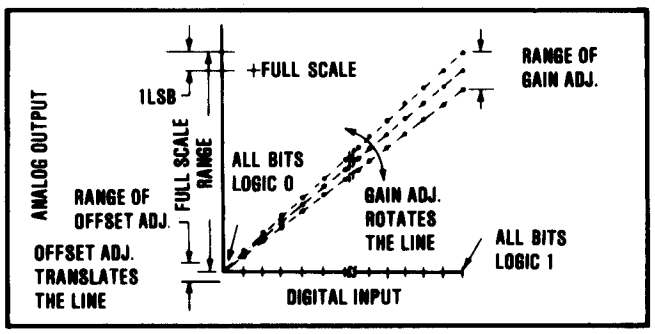


FIGURE 2. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

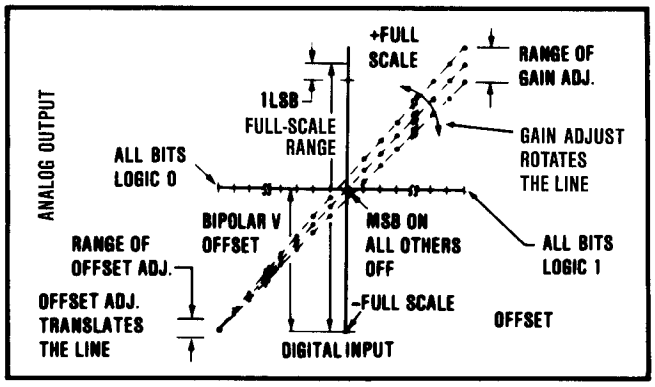


FIGURE 3. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

OFFSET ADJUSTMENT

For unipolar (USB) configurations, apply the digital input code that should produce zero voltage output and adjust the Offset potentiometer for zero output. For bipolar (BOB, BTC) configurations, apply the digital input code that should produce the maximum negative output voltage and adjust the Offset potentiometer for minus full-scale voltage. Example: If the full-scale range is connected for 20V, the maximum negative output voltage is −10V. See Table II for corresponding codes.

TABLE II. Digital Input/Analog Output, $\pm V_{CC} = \pm 15V$.

Digital Input	Analog Output		
12-Bit Resolution MSB ↓ LSB ↓	0 to +10V	±5V	±10V
111111111111	+9.9976V	+4.9976V	+9.9951V
100000000000	+5.0000V	0.0000V	0.0000V
011111111111	+4.9976V	−0.0024V	−0.0049V
000000000000	0.0000V	−5.0000V	−10.0000V
1LSB	2.44mV	2.44mV	4.88mV

GAIN ADJUSTMENT

For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full-scale voltage. See Table II for positive full-scale voltages.

±12V OPERATION

The DAC1201 is fully specified for operation on ±12V power supplies. However, in order for the output to swing to ±10V, the power supplies must be ±13.5V or greater. When operating with ±12V supplies, the output swing should be restricted to ±8V in order to meet specifications.

INSTALLATION

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram, Figure 4.

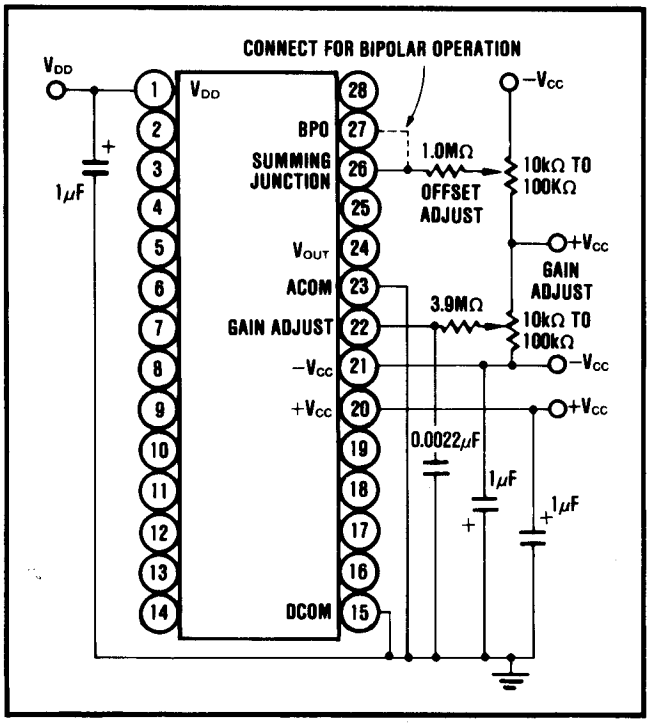


FIGURE 4. Power Supply, Gain, and Offset

These capacitors (1μF to 10μF tantalum recommended) should be located close to the DAC1201.

The DAC1201 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. The Analog Common (pin 23) and Digital Common (pin 15) should be connected together at one point. Separate returns minimize current flow in low-level signal paths if properly connected. Logic return currents are not added into the analog signal return path. A ±0.5V difference between ACOM and DCOM is permitted for specified operation. High frequency noise on DCOM with respect to ACOM may permit noise to be coupled through to the analog output; therefore, some caution is required in applying these common conections.

The Analog Common is the high quality return for the D/A converter and should be connected directly to the analog reference point of the system. The load driven by the output amplifier should be returned to the Analog Common.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and Gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in Figure 4. TCR of the potentiometers should be 100ppm/°C or less. The 1.0MΩ and 3.9MΩ resistors (20% carbon or better) should be located close to the DAC1201 to prevent noise pick-up. If it is not convenient to use these high value resistors, and equivalent "T" network, as shown in Figure 5, may be substituted in each case. The Gain Adjust (pin 22) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Analog Common to reduce noise pick-up in all applications, including those not employing external gain adjustment.

OUTPUT RANGE CONNECTIONS

Internal-scaling resistors provided in the DAC1201 may be connected to produce bipolar output voltage ranges of ±10V and ±5V or unipolar output voltage range of 0 to +10V. The 20V range (±10V bipolar range) is internally connected. Refer to Figure 6. Connections for the output ranges are listed in Table III.

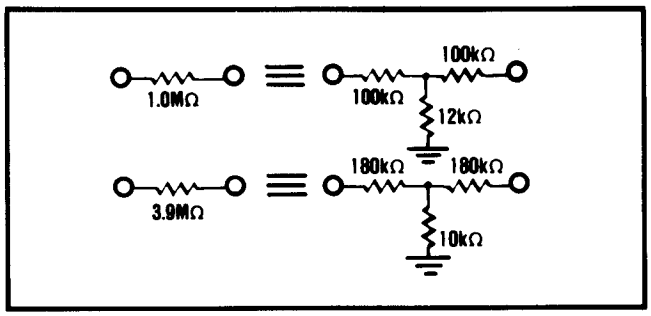


FIGURE 5. Equivalent Resistances.

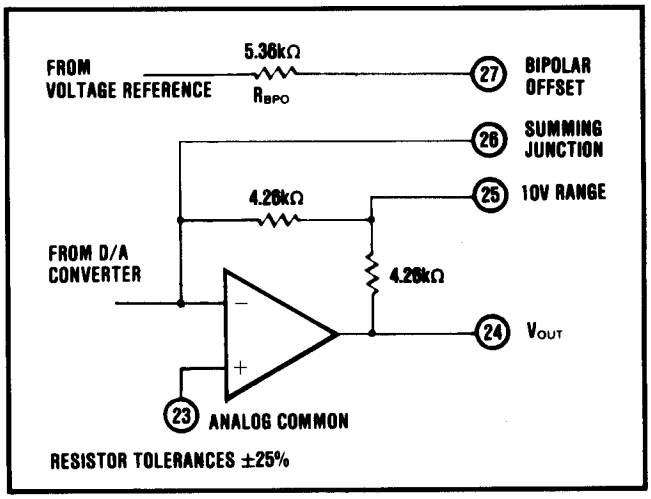


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

TABLE III. Output Range Connections.

Output Range	Digital Input Codes	Connect Pin 25 To	Connect Pin 27 To
0 to +10V	USB	24	23
±5V	BOB or BTC	24	26
±10V	BOB or BTC	NC	26

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
DAC1201KP-V	OBSOLETE	PDIP	NTD	28	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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