14-BIT, 400 MSPS, 2x/4x INTERPOLATING CommsDAC™ DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 200-MSPS Maximum Input Data Rate
- 400-MSPS Maximum Update Rate DAC
- 76-dBc SFDR Over Full First Nyquist Zone With Single Tone Input Signal (F_{out} = 21 MHz)
- 74-dBc ACPR W-CDMA at 15.36 MHz IF
- 69-dBc ACPR W-CDMA at 30.72 MHz IF
- Selectable 2x or 4x Interpolation Filter
  - Linear Phase
  - 0.05-dB Passband Ripple
  - 80-dB Stopband Attenuation
  - Stopband Transition 0.4−0.6 F_{data}
  - nterpolation Filters Configurable in Either Low-Pass or High-Pass Mode, Allows For Selection Higher Order Image
- On-chip 2x/4x PLL Clock Multiplier, PLL Bypass Mode
- Differential Scalable Current Outputs: 2 mA to 20 mA
- On-Chip 1.2-V Reference
- 1.8-V Digital and 3.3-V Analog Supply Operation
- 1.8/3.3-V CMOS Compatible Interface
- Power Dissipation: 435 mW at 400 MSPS
- Package: 48-Pin TQFP

APPLICATIONS

- Cellular Base Transceiver Station Transmit Channel
  - CDMA: W−CDMA, CDMA2000, IS−95
  - TDMA: GSM, IS−136, EDGE/UWC−136
- Test and Measurement: Arbitrary Waveform Generation
- Direct Digital Synthesis (DDS)
- Cable Modem Termination System

DESCRIPTION

The DAC5674 is a 14-bit resolution high-speed digital-to-analog converter (DAC) with integrated 4x-interpolation filter, on-board clock multiplier, and on-chip voltage reference. The device has been designed for high-speed digital data transmission in wired and wireless communication systems, high-frequency direct-digital synthesis (DDS) and waveform reconstruction in test and measurement applications.

The 4x-interpolation filter is implemented as a cascade of two 2x-interpolation filters, each of which can be configured for either low-pass or high-pass response. This enables the user to select one of the higher order images present at multiples of the input data rate clock while maintaining a low date input rate. The resulting high IF output frequency allows the user to omit the conventional first mixer in heterodyne transmitter architectures and directly up-convert to RF using only one mixer, thereby reducing system complexity and costs.

In 4x-interpolation low-pass response mode, the DACs excellent spurious free dynamic range (SFDR) at intermediate frequencies located in the first Nyquist zone (up to 40 MHz) allows for multicarrier transmission in cellular base transceiver stations (BTS). The low-pass interpolation mode thereby relaxes image filter requirements by filtering out the images in the adjacent Nyquist zones.

The DAC5674 PLL clock multiplier controls all internal clocks for the digital filters and DAC core. The differential clock input and internal clock circuitry provides for optimum jitter performance. Sine wave clock input signal is supported. The PLL can be bypassed by an external clock running at the DAC core update rate. The clock divider of the PLL ensures that the digital filters operate at the correct clock frequencies.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

The DAC5674 operates from an analog supply voltage of 3.3 V and a digital supply voltage of 1.8 V. The digital I/O's are 1.8-V and 3.3-V CMOS compatible. Power dissipation is 500 mW at maximum operating conditions. The DAC5674 provides a nominal full-scale differential current-output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The device has been specifically designed for a differential transformer coupled output with a 50-Ω doubly terminated load. For a 20-mA full-scale output current both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (−2-dBm output power) are supported. The latter configuration is preferred for optimum performance at high output frequencies and update rates.

An accurate on-chip 1.2-V temperature compensated bandgap reference and control amplifier allows the user to adjust the full-scale output current from 20 mA down to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage may be applied for maximum flexibility. The device features a SLEEP mode, which reduces the standby power to approximately 10 mW, thereby optimizing the power consumption for the system's need.

The DAC5674 is available in a 48-pin HTQFP Powerpad plastic quad flatpack package. The device is characterized for operation over the industrial temperature range of −40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
−40°C to 85°C	48-HTQFP PowerPAD™ Plastic Quad Flatpack
	DAC5674IPHP
	DAC5674IPHPR

NOTE: PowerPAD is a trademark of Texas Instruments.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Supply voltage range	AVDD(2), CLKVDD(2), IOVDD(2), PLLVDD(2)	−0.5 V to 4 V
	DVDD(3)	−0.5 V to 2.3 V
Voltage between AGND, DGND, CLKGND, PLLGND, and IOGND		−0.5 V to 0.5 V
Supply voltage range	D[13..0](3), HP1, HP2, DIV0(3), DIV1(3), PLLLOCK(3), RESET(3), X4(3)	−0.5 V to IOVDD + 0.5 V
	IOUT1, IOUT2(2)	−1 V to AVDD + 0.5 V
	EXTIO(2), EXTLO(2), BIASJ(2), SLEEP(2), CLK(2), CLKC(2), LPF(2)	−0.5 V to AVDD + 0.5 V
Peak input current (any input)		20 mA
Peak total input current (all inputs)		−30 mA
Operating free-air temperature range, T_A: DAC5674I		−40°C to 85°C
Storage temperature range		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND.
(3) Measured with respect to DGND.

DC ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, IOUTFS = 20 mA, R_{set} = 1.91 kΩ, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION			14			Bits
DC ACCURACY(1)						
INL	Integral nonlinearity	1 LSB = $IOUT_{FS}/2^{14}$, T_{MIN} to T_{MAX}	−3.5		3.5	LSB
			−2.14e−4		2.14e−4	$IOUT_{FS}$
DNL	Differential nonlinearity		−2		2	LSB
			−1.22e−4		1.22e−4	$IOUT_{FS}$
Monotonicity			Montonic to 12 bits			
ANALOG OUTPUT						
	Offset error			0.02		FSR
	Gain error	Without internal reference		2.3		%FSR
		With internal reference		1.3		
	Minimum full-scale output current(2)			2		mA
	Maximum full-scale output current(2)			20		mA
	Output compliance range(3)	$IOUT_{FS}$ = 20 mA	−1		1.25	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
REFERENCE OUTPUT						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(4)			100		nA
REFERENCE INPUT						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small signal bandwidth			1.4		MHz
	Input capacitance			100		pF
TEMPERATURE COEFFICIENTS						
	Offset drift			0		ppm of FSR/°C
	Gain drift	Without internal reference		±50		ppm of FSR/°C
		With internal reference		±100		ppm of FSR/°C
	Reference voltage drift			±50		ppm/°C
POWER SUPPLY						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		1.65	1.8	1.95	V
CLKVDD	Clock supply voltage		3	3.3	3.6	V
IOVDD	I/O supply voltage		1.65		3.6	V
PLLVDD	PLL supply voltage		3	3.3	3.6	V
I_{AVDD}	Analog supply current	Including output current through the load resistor, AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation,PLL on, 9-MHz IF, 400 MSPS		41	55	mA

Specifications subject to change without notice.

(1) Measured differentially across IOUT1 and IOUT2 into 50 Ω.

(2) Nominal full-scale current, IOUTFS, equals 32X the IBIAS current.

(3) The lower limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5674 device. The upper limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

(4) Use an external buffer amplifier with high impedance input to drive any external load.

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, IOUTFS = 20 mA, R_{set} = 1.91 kΩ, internal reference, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (CONTINUED)						
I_{DVDD}	Digital supply current	AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation,PLL on, 9-MHz IF, 400 MSPS		107	140	mA
$I_{SLEEP3.3}$	Sleep mode	Sleep mode, supply current 3.3 V		6	12	mA
$I_{SLEEP1.8}$	Sleep mode	Sleep mode, supply current 1.8 V		0.5	3	mA
I_{PLLVDD}	PLL supply current(1)	F_{data} = 100 MSPS, F_{update} = 400 MSPS, DIV[1:0] = '00', AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation,PLL on, 9-MHz IF, 400 MSPS		23	35	mA
I_{IOVDD}	Buffer supply current	AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation,PLL on, 9-MHz IF, 400 MSPS		4	10	mA
I_{CLKVDD}	Clock supply current(1)	AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation,PLL on, 9-MHz IF, 400 MSPS		6	10	mA
P_D	Power dissipation	AVDD = 3.3 V, DVDD = 1.8 V, 4x interpolation, PLL on, 9-MHz IF, 400 MSPS		435	550	mW
APSRR	Power supply rejection ratio		−0.2		0.2	%FSR/V
DPSRR			−0.2		0.2	
Operating range			−40		85	°C

Specifications subject to change without notice.
(1) PLL enabled

AC ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 1.8 V, DVDD = 1.8 V, IOUTFS = 20 mA, differential transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
f_{CLK}	Maximum output update rate		400			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Mid-scale transition		20		ns
$t_{r(IOUT)}$	Output rise time 10% to 90%(1)			1.4		ns
$t_{f(IOUT)}$	Output fall time 90% to 10%(1)			1.5		ns
	Output noise	$IOUT_{FS}$ = 20 mA		55		pA/√HZ
		$IOUT_{FS}$ = 2 mA		30		
AC LINEARITY 1:1 IMPEDANCE RATIO TRANSFORMER						
SFDR	Spurious free dynamic range (First Nyquist zone < f_{DATA}/2) X4 LL-mode	f_{DATA} = 52 MSPS, f_{OUT} = 14 MHz, T_A = 25°C		85		dBc
		f_{DATA} = 100 MSPS, f_{OUT} = 21 MHz, T_{MIN} to T_{MAX}		76		
		f_{DATA} = 100 MSPS, f_{OUT} = 41 MHz, T_{MIN} to T_{MAX}		71		
SNR	Signal-to-noise ratio (First Nyquist zone < f_{DATA}/2) X4 LL-mode	f_{DATA} = 78 MSPS, f_{OUT} = 20 MHz, T_{MIN} to T_{MAX}		71		dB
		f_{DATA} = 100 MSPS, f_{OUT} = 20 MHz, T_{MIN} to T_{MAX}		70		
ACPR	Adjacent channel power ratio W-CDMA signal with 3.84 MHz BW 5-MHz channel spacing	f_{DATA} = 61.44 MSPS, IF = 15.360 MHz, X4 LL-mode		74		dB
		f_{DATA} = 122.88 MSPS, IF = 30.72 MHz, X2 L-mode		69		
IMD3	Third-order two-tone intermodulation (each tone at −6 dBFS)	f_{DATA} = 61.44 MSPS, f_{OUT} = 45.4 and 46.4 MHz, X4 HL-mode		68		dBc
		f_{DATA} = 61.44 MSPS, f_{OUT} = 15.1 and 16.1 MHz, X4 LL-mode		82		
IMD	Four-tone Intermodulation to Nyquist (each tone at –12 dBFS)	f_{DATA} = 78 MSPS f_{OUT} = 15.6 MHz, 15.8 MHz, 16.2 MHz, 16.4 MHz, X4 LL-mode		76		dBc
		f_{DATA} = 52 MSPS f_{OUT} = 68.8 MHz, 69.6 MHz, 71.2 MHz, 72 MHz, X4 HH-mode		64		

(1) Measured single ended into 50-Ω load.

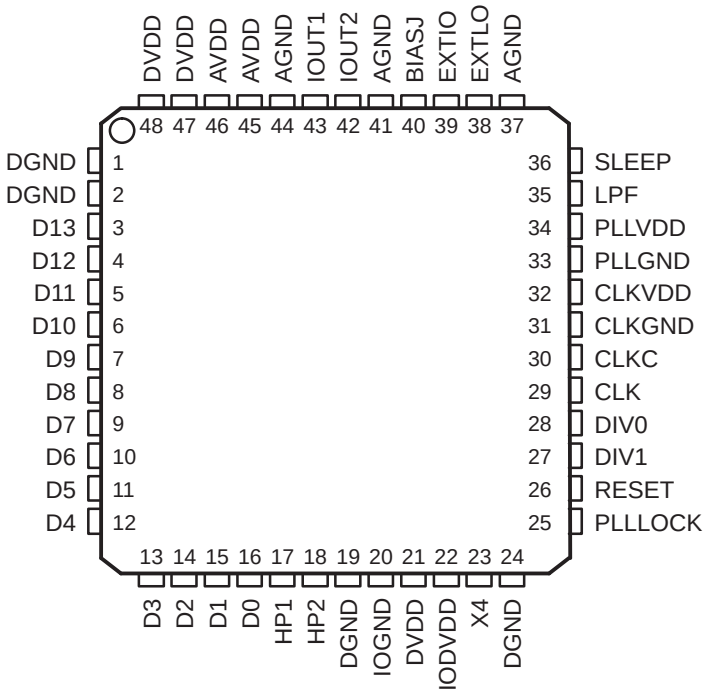
ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, IOUTFS = 20 mA, differential transformer coupled output, 50-Ω doubly terminated load (unless otherwise noted)

DIGITAL SPECIFICATIONS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS INTERFACE						
V_{IH}	High-level input voltage for SLEEP and EXTLO		$0.7xAV_{DD}$			V
V_{IL}	Low-level input voltage for SLEEP and EXTLO		0		$0.3xAV_{DD}$	V
V_{IH}	High-level input voltage other digital inputs		$0.7xIOV_{DD}$			V
V_{IL}	Low-level input voltage other digital inputs		0		$0.3xIOV_{DD}$	V
I_{IH}	High-level input current		10		30	µA
I_{IL}	Low-level input current		−1		10	µA
	Input capacitance		1		5	pF
TIMING INTERNAL CLOCK MODE						
t_{SU}	Input setup time		0.6			ns
t_H	Input hold time		0.6			ns
t_{LPH}	Input latch pulse high time			2		ns
t_{lat_2x}	Data in to DAC out latency − 2X interpolation			26		clk
t_{lat_4x}	Data in to DAC out latency − 4X interpolation			35		clk
TIMING − EXTERNAL CLOCK MODE						
t_{su}	Input setup time		5			ns
t_h	Input hold time		−1.75			ns
t_{lph}	Input latch pulse high time			2		ns
t_{d_clk}	Clock delay time			3.6		ns
t_{lat_2x}	Data in to DAC out latency − 2X interpolation			26		clk
t_{lat_4x}	Data in to DAC out latency − 4X interpolation			35		clk
PLL						
	Input data rate supported		5		200	MSPS
	Phase noise	At 600-kHz offset		−124		dBc/Hz
		At 6-MHz offset		−134		
DIGITAL FILTER SPECIFICATIONS						
f_{DATA}	Input data rate				200	MSPS
FIR1 and FIR2 DIGITAL FILTER CHARACTERISTICS						
	Passband width	0.005 db		0.407		f_{OUT}/f_{DATA}
		0.01 dB		0.41		
		0.1 dB		0.427		
		3 dB		0.481		

PIN OUT DIAGRAM

PHP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	37, 41, 44	I	Analog ground return
AVDD	45, 46	I	Analog supply voltage
BIASJ	40	O	Full-scale output current bias
CLK	29	I	External clock input
CLKC	30	I	Complementary external clock input
CLKGND	31	I	Ground return for internal clock buffer
CLKVDD	32	I	Internal clock buffer supply voltage
D[13..0]	3−16	I	Data bits 0 through 13 D13 is most significant data bit (MSB) D0 is least significant data bit (MSB)
DIV[1..0]	27,28	I	PLL prescaler divide ratio settings
DGND	1, 2, 19, 24	I	Digital ground return
DVDD	21, 47, 48	I	Digital supply voltage
EXTIO	39	I/O	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as internal reference output when EXTLO = AGND, requires a 0.1-µF decoupling capacitor to AGND when used as reference output
EXTLO	38	I	For internal reference connect to AGND. Connect to AVDD to disable the internal reference
HP1	17	I	Filter 1 high-pass setting. Active high
HP2	18	I	Filter 2 high-pass setting. Active high
IOGND	20	I	Input digital ground return
IOVDD	22	I	Input digital supply voltage
IOUT1	43	O	DAC current output. Full scale when all input bits are set 1
IOUT2	42	O	DAC complementary current output. Full scale when all input bits are 0
LPF	35	I	PLL loop filter connection
PLLGND	33	I	Ground return for internal PLL
PLLLOCK	25	O	PLL lock status bit. PLL is locked to input clock when high. Provides output clock equal to the data rate when the PLL is disabled.
PLLVDD	34	I	Internal PLL supply voltage. Connect to PLLGND to disable PLL clock multiplier.
RESET	26	I	Reset internal registers. Active high
SLEEP	36	I	Asynchronous hardware power down input. Active high. Internally pull down.
X4	23	I	4x interpolation mode. Active high. Filter 1 is bypassed when connected to DGND

FUNCTIONAL BLOCK DIAGRAM

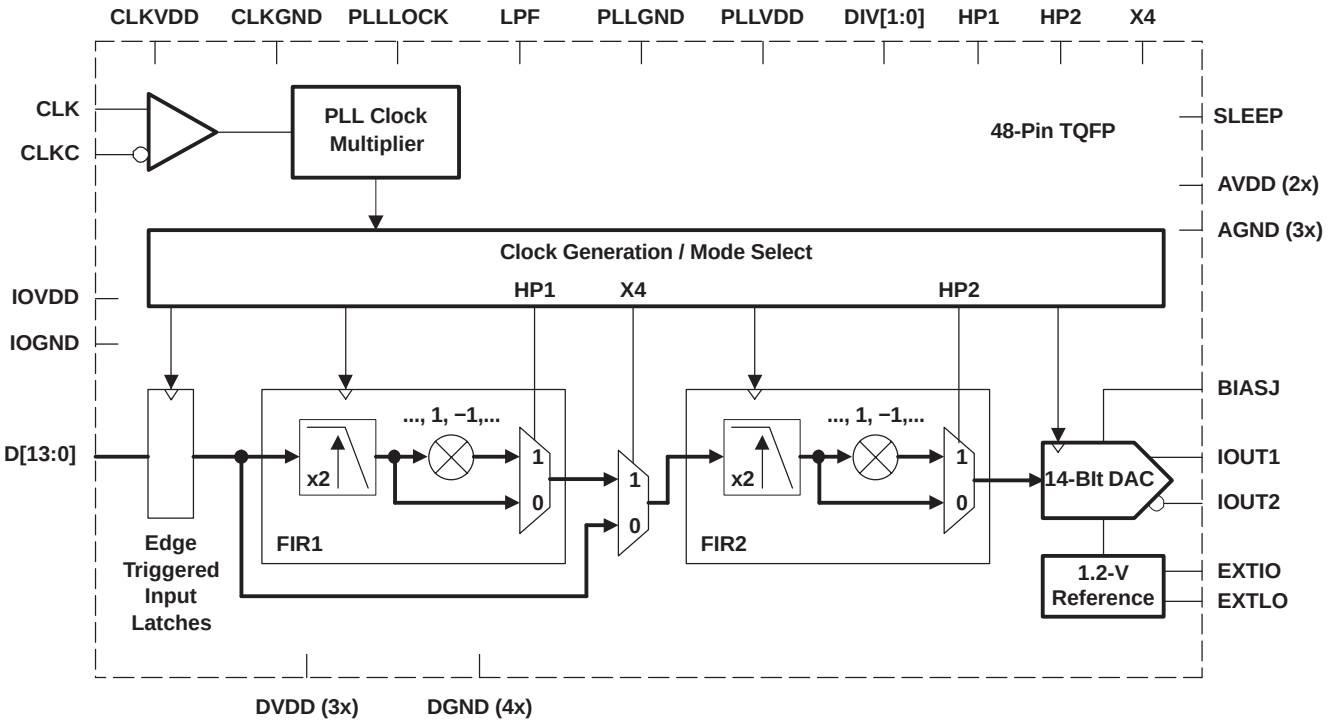


Figure 1. Block Diagram

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY
vs
INPUT CODE

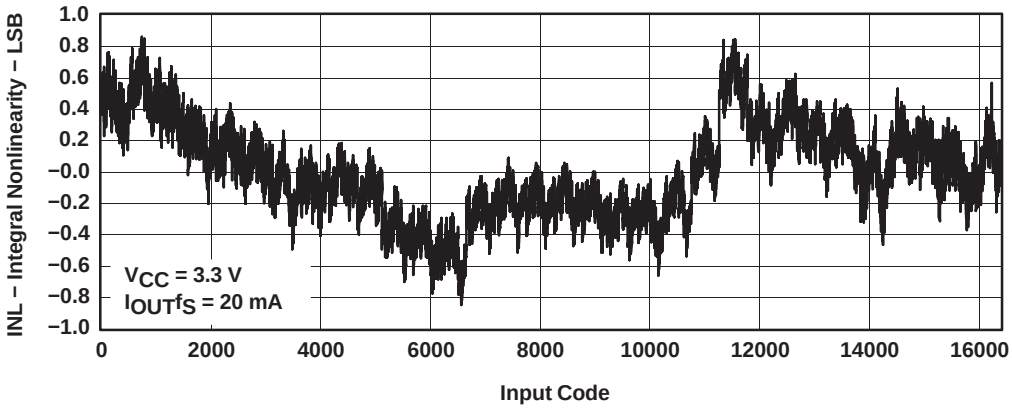


Figure 2

DIFFERENTIAL NONLINEARITY
vs
INPUT CODE

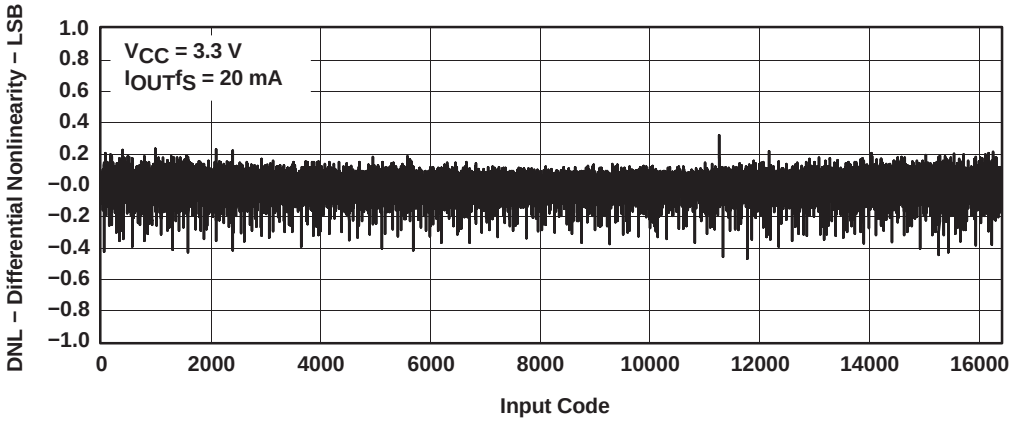


Figure 3

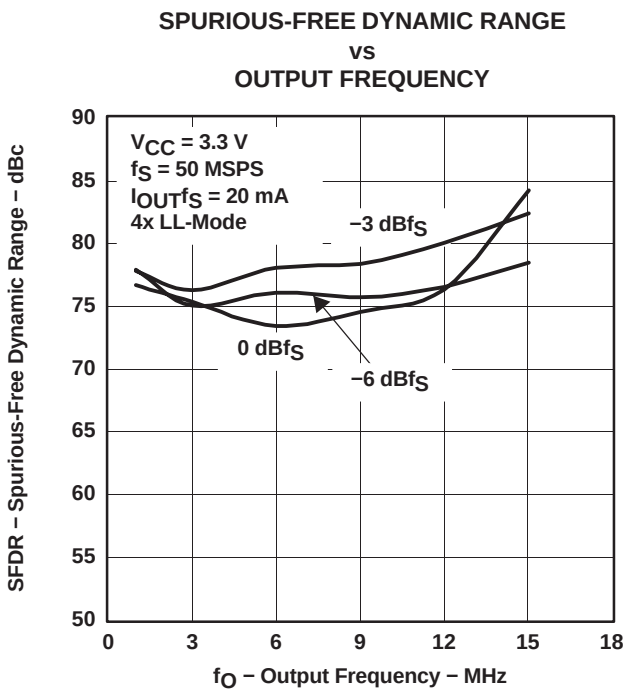


Figure 4

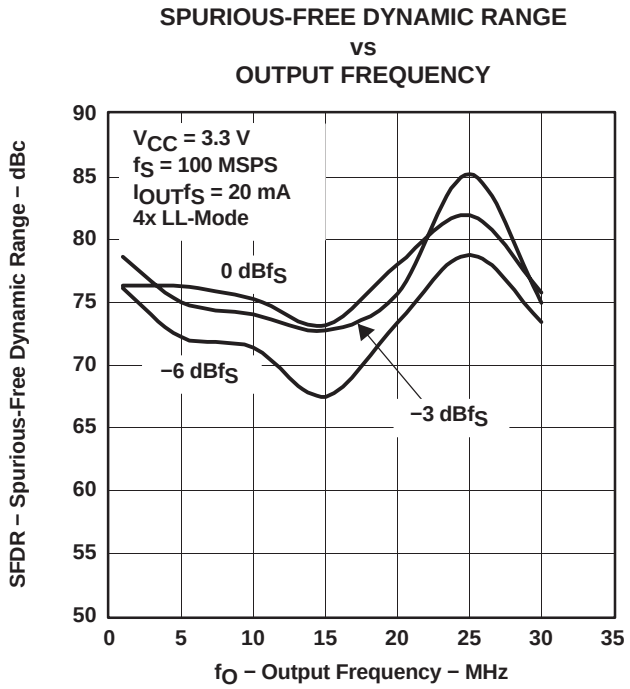


Figure 5

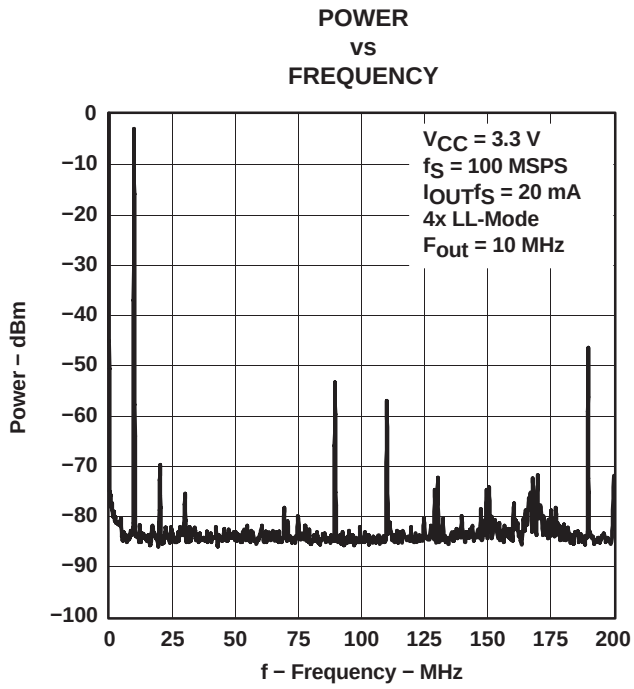


Figure 6

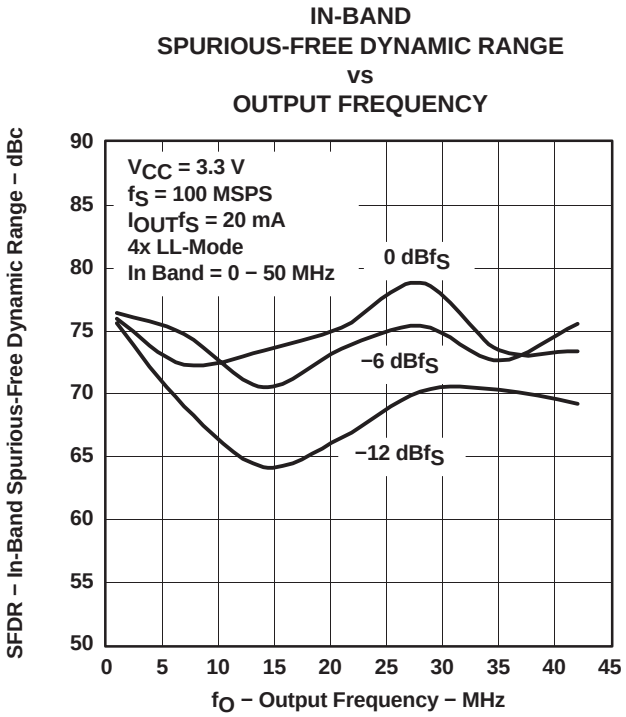


Figure 7

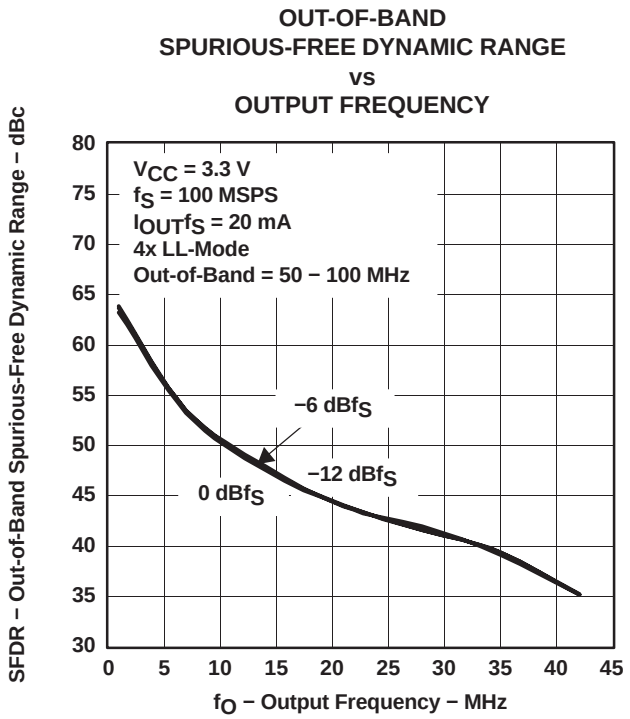


Figure 8

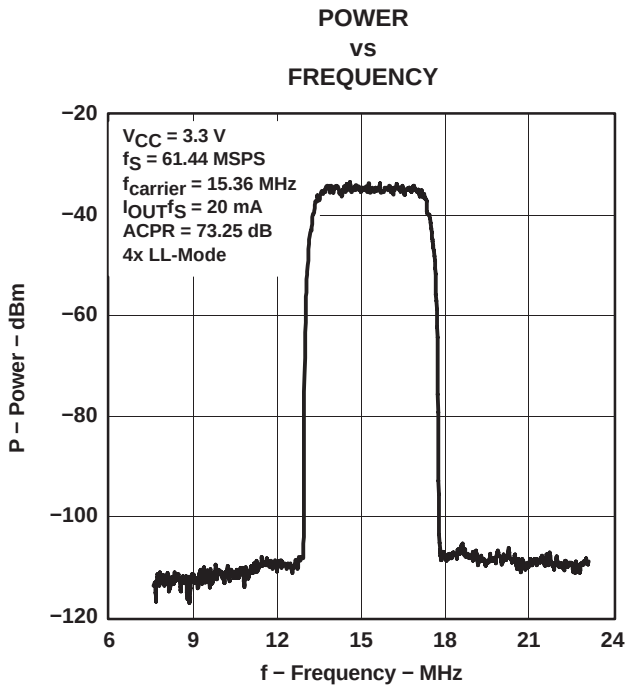


Figure 9

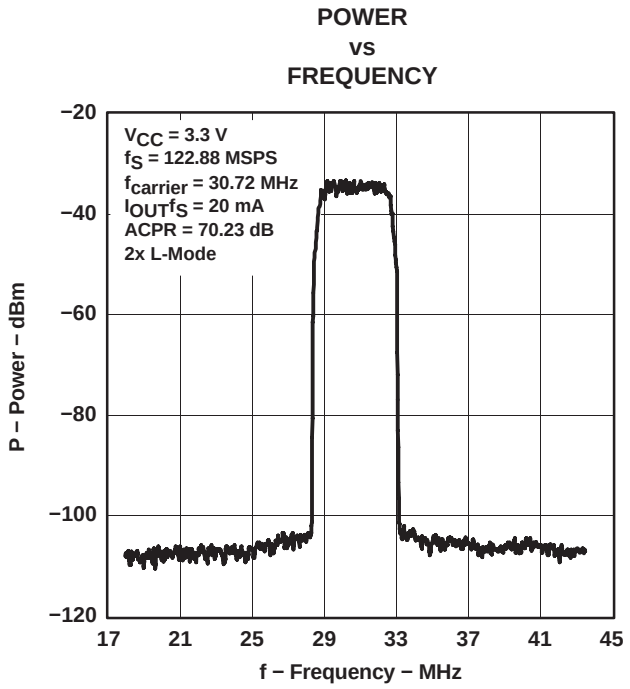


Figure 10

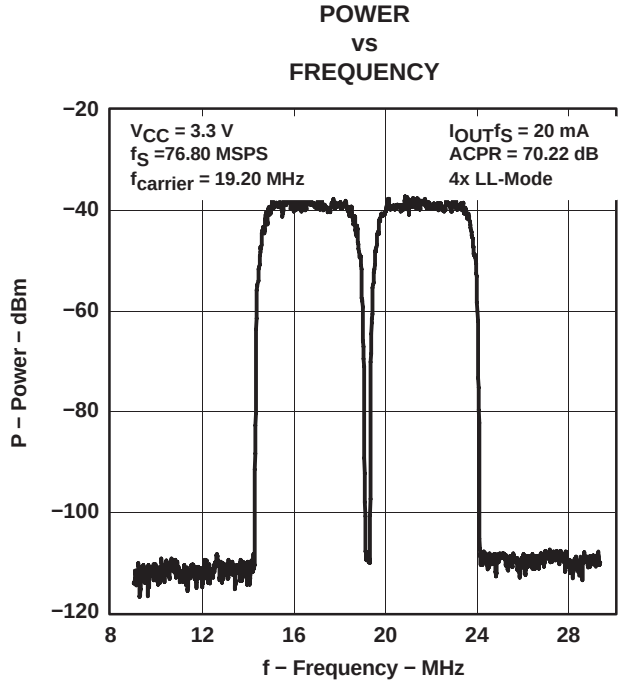


Figure 11

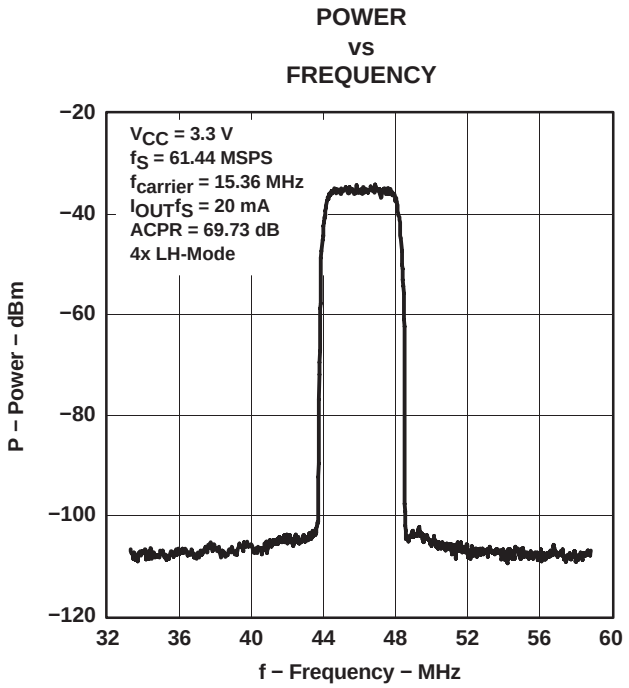


Figure 12

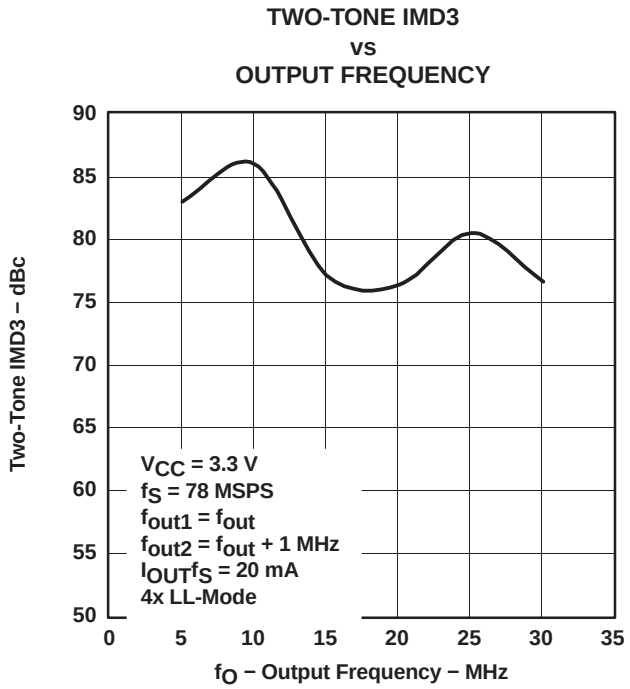


Figure 13

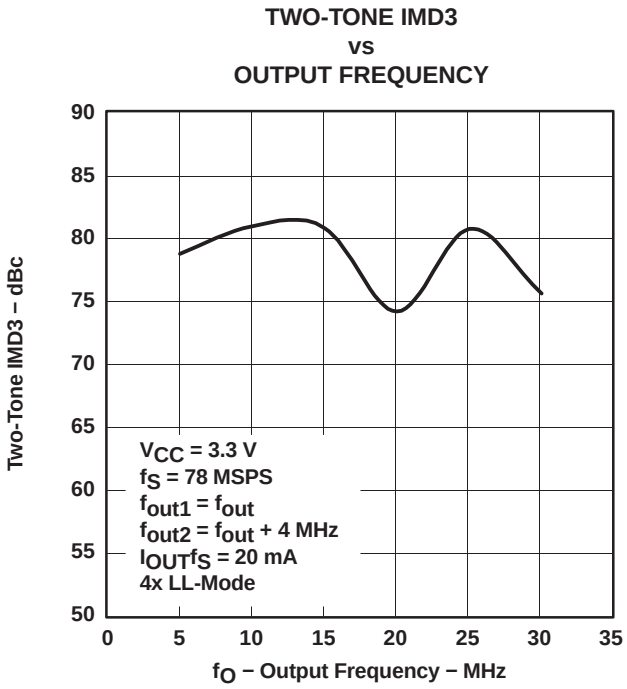


Figure 14

DETAILED DESCRIPTION

Figure 1 shows a simplified block diagram of the DAC5674. The CMOS device consists of a segmented array of PMOS current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. The complementary output currents thus enable differential operation, canceling out common mode noise sources (digital feed-through, on-chip, and PCB noise), dc offsets, even order distortion components, and increase signal output power by a factor of two.

The full-scale output current is set using an external resistor R_{BIAS} in combination with an on-chip bandgap voltage reference source (1.2 V) and control amplifier. The current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 32 times I_{BIAS}. The full-scale current can be adjusted from 20 mA down to 2 mA.

Interpolation Filter

The interpolation filters FIR1 and FIR2 can be configured for either low-pass or high-pass response. In this way, higher order images can be selected. This is shown in Table 1. Table 2 shows the DAC IF output range for the different filter response combinations, for both the first and second Nyquist zone (after interpolation). Table 3 lists the DAC IF output ranges for two popular GSM data rates. Table 3 shows the W-CDMA IF carrier center frequency for an input data rate of 61.44 MSPS and a fundamental input IF of 15.36 MHz. Figure 15 shows the spectral response; the corresponding nonzero tap weights are:

- [5, −20, 50, −108, 206, −361, 597, −947, 1467, −2267, 3633, −6617, 20746, 32768]

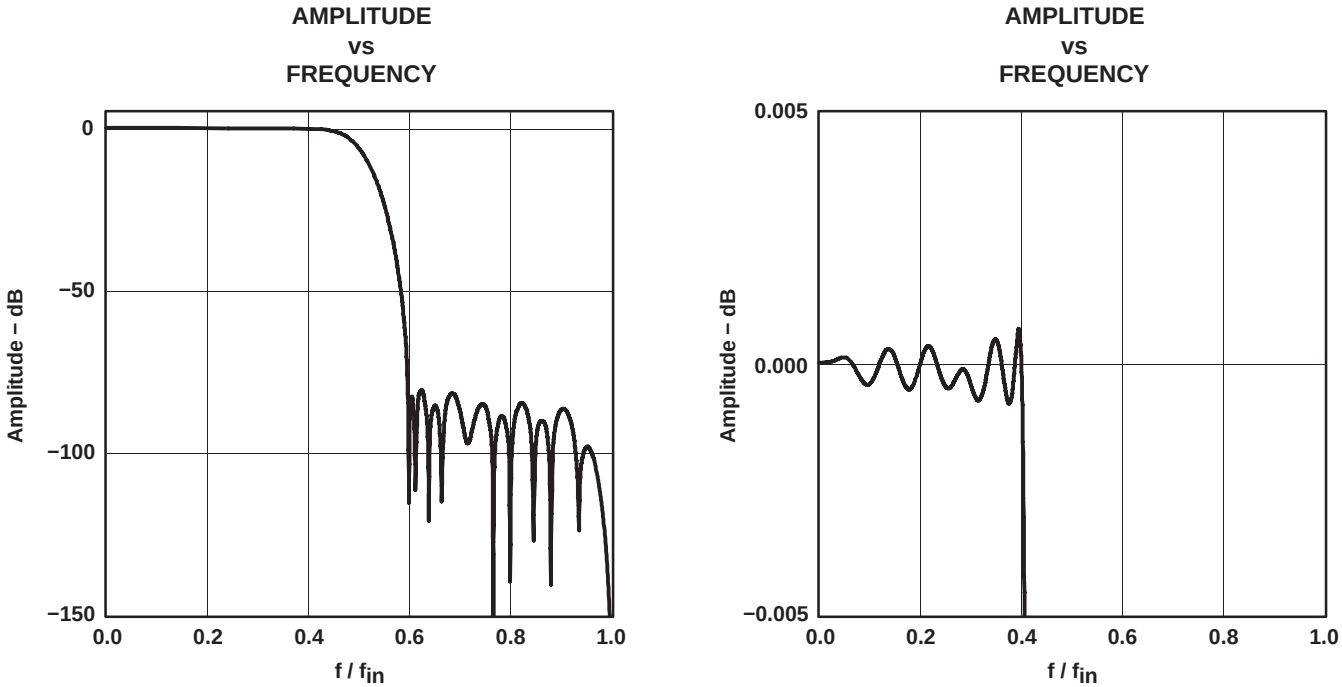


Figure 15. FIR1 and FIR2 Magnitude Spectrum

Table 1. Interpolation Filters Configuration

FILTER 1 CONFIGURATION	FILTER 2 CONFIGURATION	IF OUTPUT RANGE 1 (FIRST NYQUIST ZONE)		IF OUTPUT RANGE 2 (SECOND NYQUIST ZONE)	
		FREQUENCY	SINX/X ATT. [dB]	FREQUENCY	SINX/X ATT. [dB]
Low pass	Low pass	0…0.4F_{data}	0…0.14	3.6…4F_{data}	19.2…∞
Low pass	High pass	1.6…2F_{data}	2.42…3.92	2…2.4F_{data}	3.92…5.94
High pass	Low pass	0.6…0.8F_{data}	0.32…0.58	3.2…3.4F_{data}	12.6…15.4
High pass	High pass	1.2…1.4F_{data}	1.33…1.83	2.6…2.8F_{data}	7.20…8.69

Table 2. Interpolation Filters Configuration: Example Frequencies GSM

FILTER 1 CONFIGURATION	FILTER 2 CONFIGURATION	IF OUTPUT RANGE 1 (FIRST NYQUIST ZONE)		IF OUTPUT RANGE 2 (SECOND NYQUIST ZONE)	
		IF FREQUENCY [MHz]		IF FREQUENCY [MHz]	
		F_{data} = 52 MSPS	F_{data} = 78 MSPS	F_{data} = 52 MSPS	F_{data} = 78 MSPS
Low pass	Low pass	0…20.8	0…31.2	187.2…208	280.8…312
Low pass	High pass	83.2…108	124.8…156	104…124.8	156…187.2
High pass	Low pass	31.2…41.6	46.8…62.4	166.4…176.8	249.6…265.2
High pass	High pass	62.4…72.8	93.6…109.2	135.2…145.6	202.8…218.4

Table 3. Interpolation Filters Configuration: Example Frequencies W-CDMA, IF = F_{data}/4, F_{DATA} = 61.44 MSPS: F_{update} = 245.76 MSPS

FILTER 1 CONFIGURATION	FILTER 2 CONFIGURATION	IF FREQUENCY [MHZ] (FIRST NYQUIST ZONE)		IF FREQUENCY [MHZ] (SECOND NYQUIST ZONE)	
		IF CENTER [MHz]	SINX/X ATT. [dB]	IF CENTER [MHz]	SINX/X ATT. [dB]
Low pass	Low pass	15.36	0.05	230.4	23.6
Low pass	High pass	107.52	2.93	138.24	5.11
High pass	Low pass	46.08	0.51	199.68	13.2
High pass	High pass	76.8	1.44	168.96	8.29

Low-Pass/Low-Pass 4x Interpolation Filter Operation

Figure 16 shows the low-pass/low-pass interpolation operation where the 4x FIR filter is implemented as a cascade of two 2x interpolation filters. The user can place their IF signal at a maximum of 0.4 times the FIR filter input (i.e. DAC5674 input) data rate. For a 100-MSPS data rate, this would translate into a pass-band extending to 40 MHz.

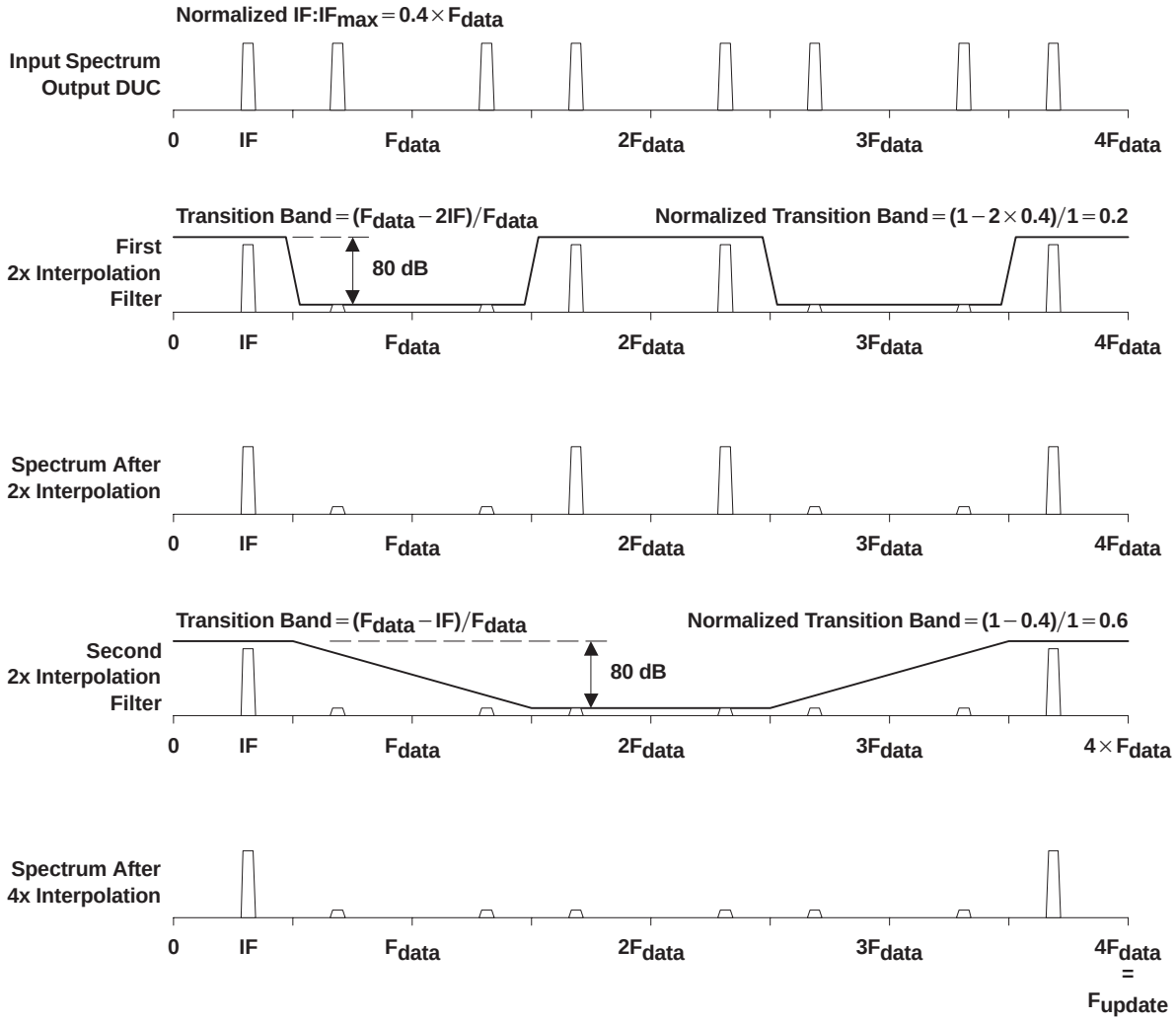


Figure 16. Low-Pass/Low-Pass 4x Interpolation Filter Operation

Low-Pass/High-Pass 4x Interpolation Filter Operation

By configuring the low-pass filters as high-pass filters the user can select one of the images present at multiples of the clock. Figure 17 shows the low-pass/high-pass filter response. After digital filtering, the DAC transmits at
$2F_{data}$ − IF and $2F_{data}$ + IF. This configuration is equivalent to sub-sampling receiver systems where a high-speed analog-to-digital converter samples high IF frequencies with relatively low sample rates, resulting in low (output) data rates.

The placement of the IF in the first Nyquist zone combined with the DAC5674 input data determines the final output signal frequency. For F_{data} = 100 MSPS and a fundamental IF of 0.4 x F_{data} = 40 MHz, this would translate into images located at 160 MHz and 240 MHz. Note that this is the equivalent of mixing a 40-MHz analog IF signal with a 200-MHz sine wave. By doing this, the first mixer in the total transmission chain is eliminated.

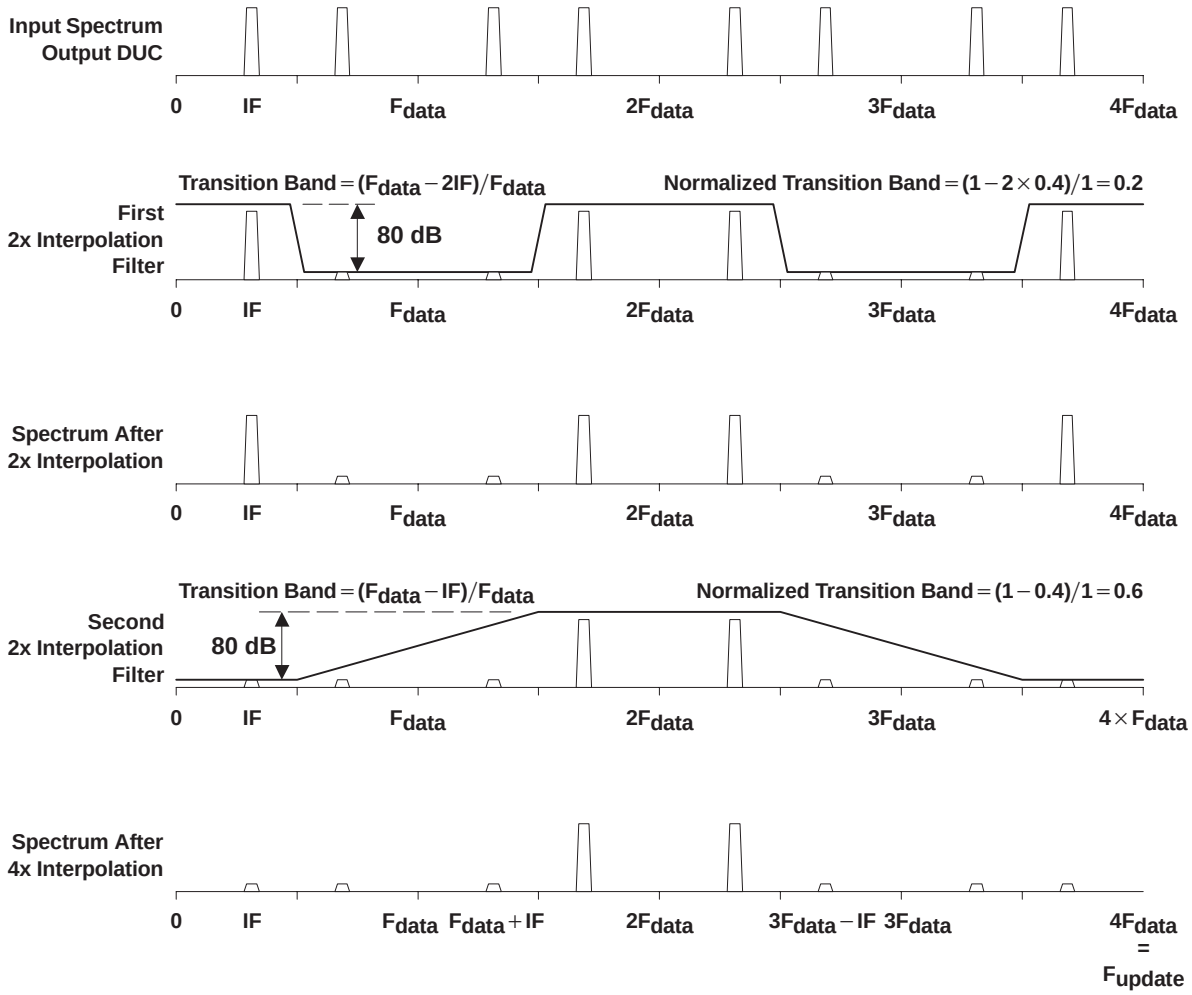


Figure 17. Low-Pass 2x, High-Pass 2x Interpolation Filter Operation

High-Pass/Low-Pass 4x Interpolation Filter Operation

Figure 18 shows the high-pass/low-pass filter configuration. Images at F_{data} − IF and $3F_{data}$ + IF can be selected. Note that the latter image severely attenuates by the sinx/x response. The transition bands of filter 1 and filter 2 of 0.2 allow for the placement of the fundamental IF between 0.2…0.4F_{data}. This results in an output IF of 0.6…0.8F_{data}.

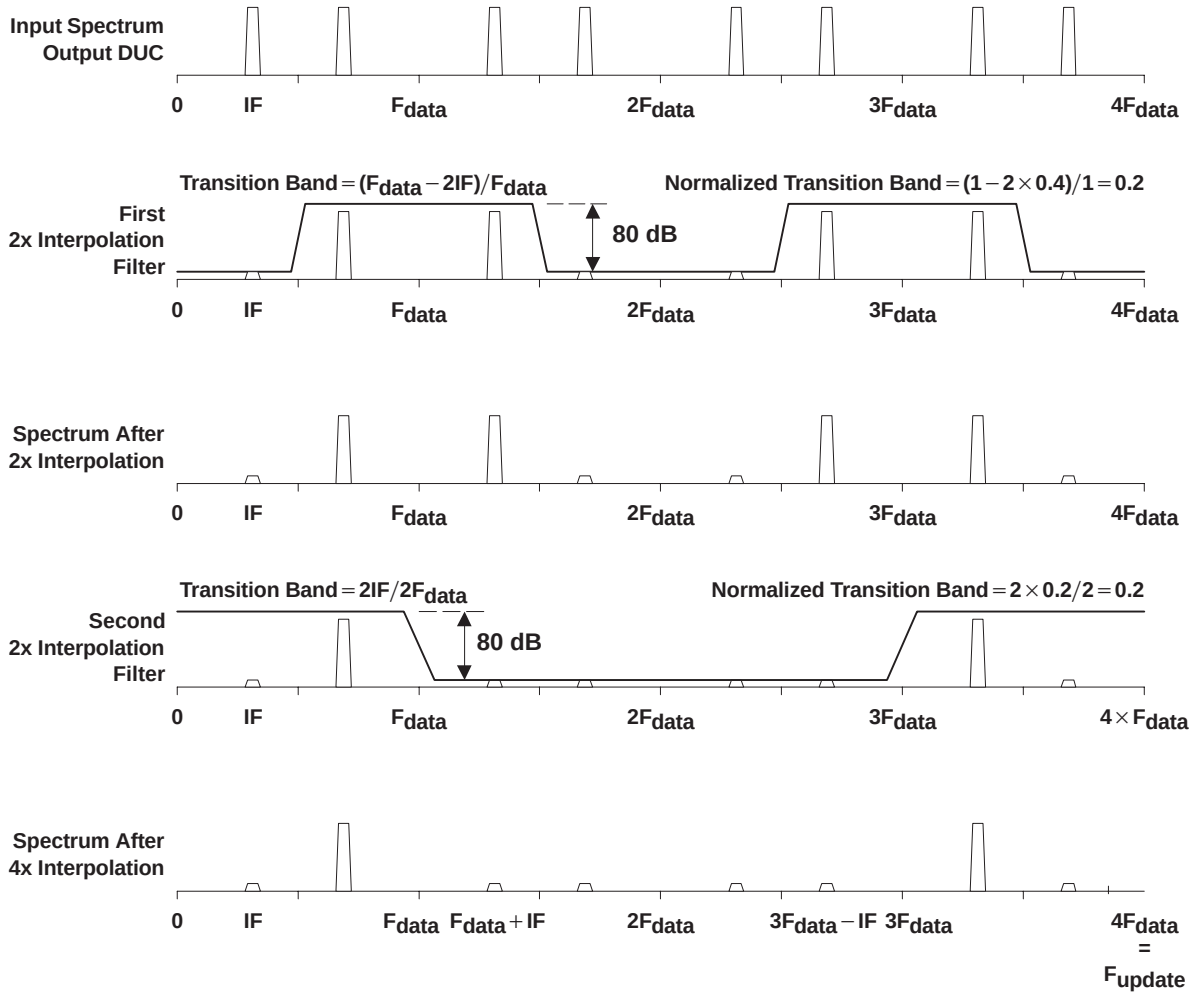


Figure 18. High-Pass 2x, Low-Pass 2x Interpolation Filter Operation

High-Pass/High-Pass 4x Interpolation Filter Operation

Figure 19 shows the high-pass/high-pass filter configuration. The transition bands of filter 1 and filter 2 allow for the placement of the fundamental IF between 0.2…0.4F_{data}. In this configuration the user can select the images at F_{data} + IF and 3F_{data} − IF. For F_{data} = 100 MSPS and a fundamental IF of 0.4 x F_{data} = 40 MHz, this would translate into images located at 140 MHz and 260 MHz. Note that this is the equivalent of mixing a 60-MHz analog IF signal with a 200-MHz sine wave.

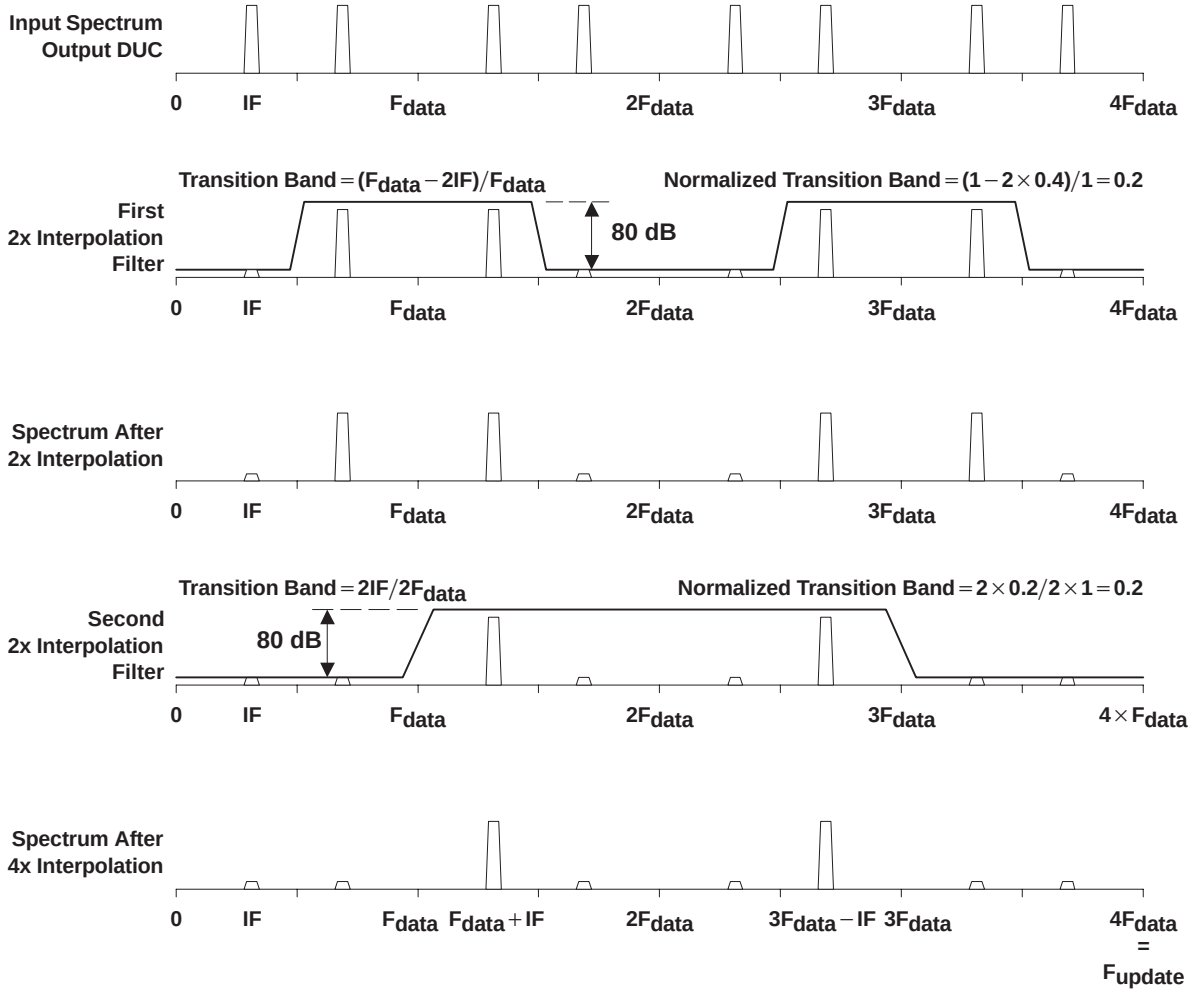


Figure 19. High-Pass/High-Pass 4x Interpolation Filter Operation

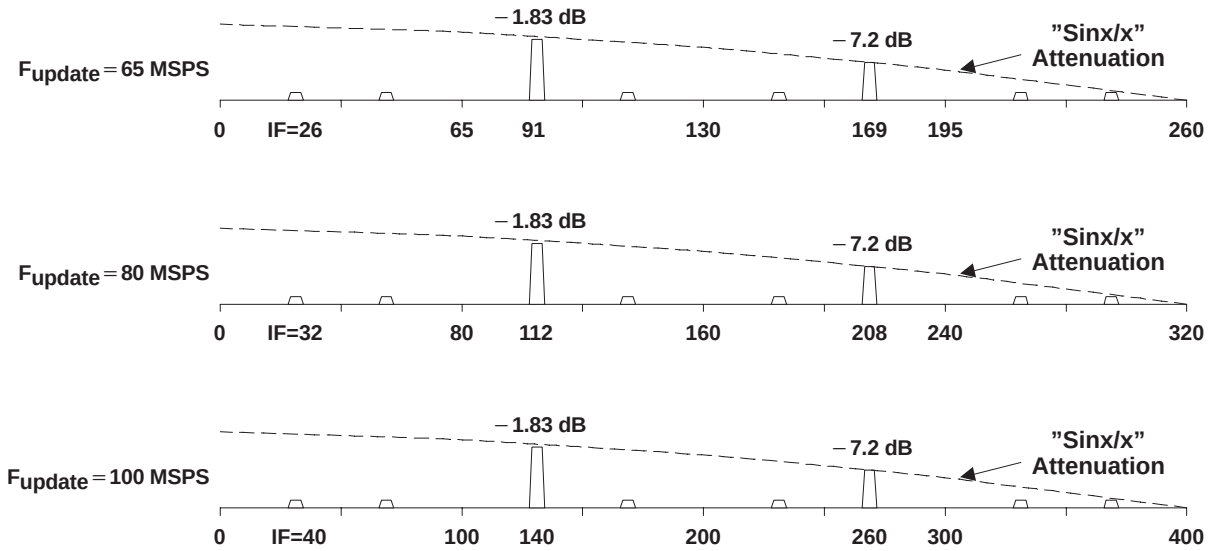


Figure 20. High-Pass 4x Interpolation Filter Operation: Example Frequencies

Clock Generation Function

An internal PLL or external clock can be used to derive the internal clocks (1x, 2x, and 4x) for the logic, FIR interpolation filters, and DAC. Basic functionality is depicted in Figure 21. Power for the internal PLL blocks (PLLVDD and PLLGND) is separate from the other clock generation blocks power (CLKVDD and CLKGND), thus minimizing phase noise within the PLL. The PLLVDD pin establishes internal/external clock mode: when PLLVDD is grounded, external clock mode is active and when PLLVDD is 3.3 V, internal clock mode is active.

In external clock mode, the user provides a differential external clock on pins CLK/CLKC. This clock becomes the 4x clock and is twice divided down to generate the 2x and 1x clocks. The 2x or 1x clock is multiplexed out on the PLLLOCK pin to allow for external clock synchronization.

In internal clock mode, the user provides a differential external reference clock on CLK/CLKC. A type four phase-frequency detector (PFD) in the internal PLL compares this reference clock to a feedback clock and drives the PLL to maintain synchronization between the two clocks. The feedback clock is generated by dividing the VCO output by 1x, 2x, 4x, or 8x, as selected by the prescaler (DIV[1:0]). The output of the prescaler is the 4x clock, and is divided down twice to generate the 2x and 1x clocks. Pin X4 selects the 1x or 2x clock to clock in the input data; the selected clock is also fed back to the PFD for synchronization. The PLLLOCK pin is an output indicating when the PLL has achieved lock. An external RC low-pass PLL filter is provided by the user at pin LPF. See the *Low-Pass Filter* section for filter setting calculations. Table 4 provides a summary of the clock configurations with corresponding data rate ranges.

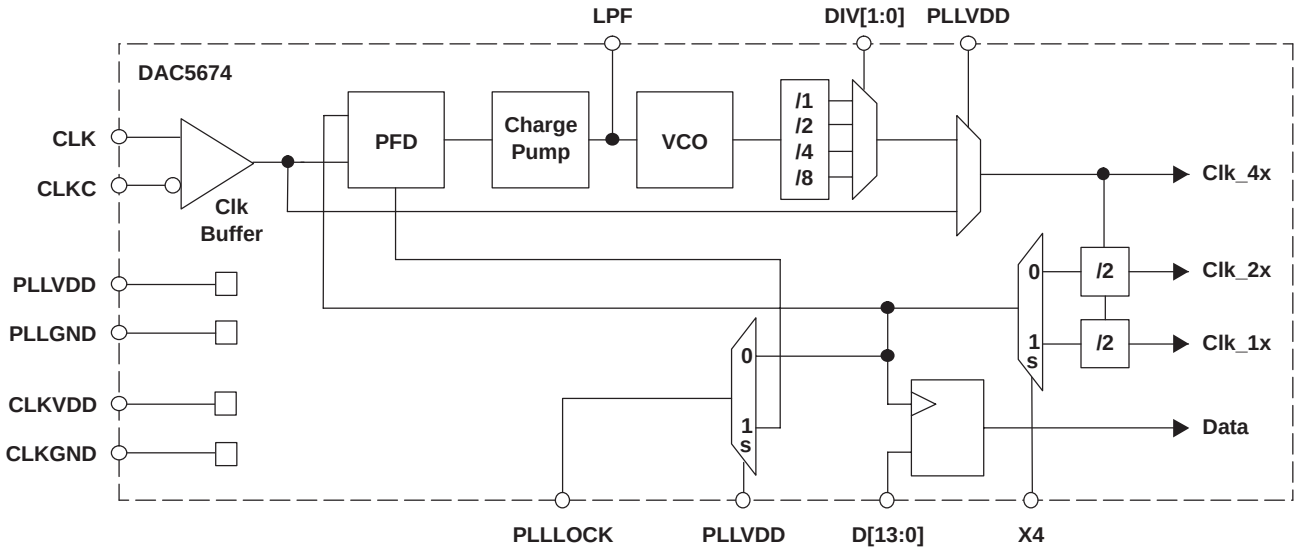


Figure 21. Clock Generation Functional Diagram

Table 4. Clock Mode Configuration

CLOCK MODE	PLLVDD	DIV[1:0]	X4	DATA RANGE (MHz)	PLLLOCK PIN FUNCTION
External 2X	0 V	XX	0	DC to 200	External clock/2
External 4X	0 V	XX	1	DC to 100	External clock/4
Internal 2X	3.3 V	00	0	100 to 200	Internal PLL lock indicator
Internal 2X	3.3 V	01	0	50 to 100	Internal PLL lock indicator
Internal 2X	3.3 V	10	0	25 to 50	Internal PLL lock indicator
Internal 2X	3.3 V	11	0	12 to 25	Internal PLL lock indicator
Internal 4X	3.3 V	00	1	50 to 100	Internal PLL lock indicator
Internal 4X	3.3 V	01	1	25 to 50	Internal PLL lock indicator
Internal 4X	3.3 V	10	1	12 to 25	Internal PLL lock indicator
Internal 4X	3.3 V	11	1	5 to 12	Internal PLL lock indicator

Low-Pass Filter

The PLL consists of a type four phase-frequency detector (PFD), charge pump, external low-pass loop filter, voltage to current converter, and current controlled oscillator (ICO) as shown in Figure 22. The DAC5674 evaluation board comes with component values R = 200, C1 = 0.01 µF, and C2 = 100 pF. These values have been designed to give the phase margins and loop bandwidths listed in Table 5 for the five divide down factors of prescaling and interpolation. Note that the values derived were based on a charge pump current output of 1 mA and a VCO gain of 300 MHz/V (nominal at Fvco = 400 MHz). With this filter, the settling time from a phase or frequency disturbance is about 2.5 µs. If different PLL dynamics are required, DAC5674 users can design a second order filter for their application using PLL Loop Filter Components section.

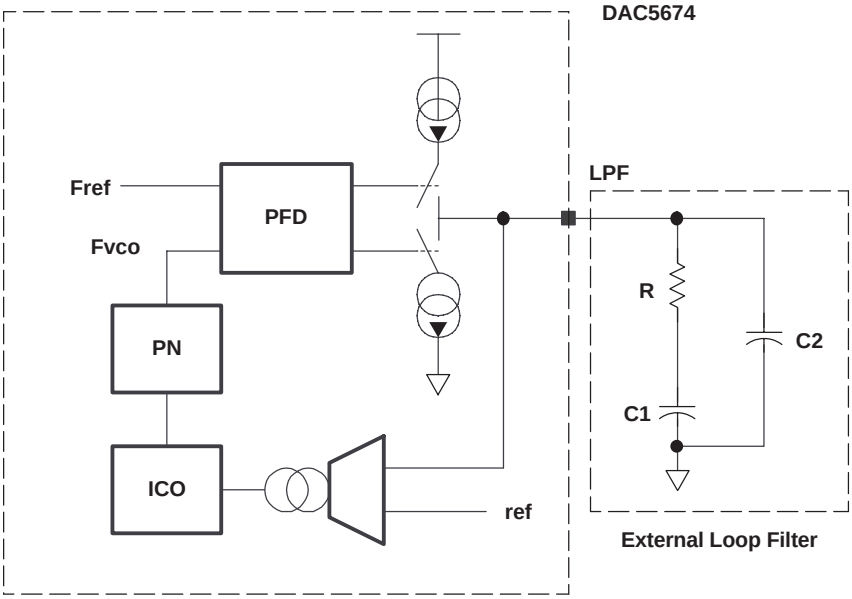


Figure 22. PLL Functional Block Diagram

Table 5. DAC5674 Evaluation Board PLL Loop Filter Parameters

N(1)	PHASE MARGIN (DEGREES)	BANDWIDTH (MHZ)
2	60	1.6
4	71	1.4
8	77	1
16	78	0.7
32	74	0.4

(1) N is the VCO divide-down factor from prescale and interpolation.

Digital Inputs

Figure 23 shows a schematic of the equivalent CMOS digital inputs of the DAC5674. The CMOS-compatible inputs have logic thresholds of IOVDD/2 ±20%. The 14-bit digital data input follows the offset positive binary coding scheme.

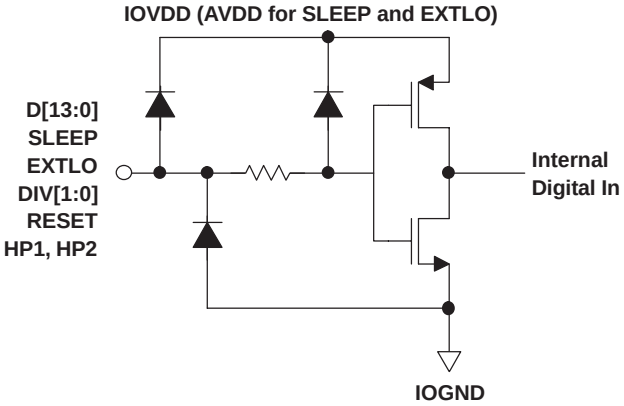


Figure 23. CMOS/TTL Digital Equivalent Input

Clock Input and Timing

Figure 24 shows the clock and data input timing diagram for internal and external clock modes, respectively. Note that a negative value indicates a reversal of the edge positions as shown in the timing diagram. Figure 24 also shows the delay (t_d) of the 1x/2x data clock (PLLLOCK) from CLK in external clock mode (typical t_d = 4.1

ns). The latency from data to DAC is defined by Figure 25. The DAC5674 features a differential clock input. In internal clock mode, the internal data clock is a divided down version of the PLL clock (/2 or /4), depending on the level of interpolation (2x or 4x). In external mode, the internal data clock is a divided down version of the input CLK (/2 or /4), depending on the level of interpolation (2x or 4x). Internal edge-triggered flip-flops latch the input word on the rising edge of the positive data clock.

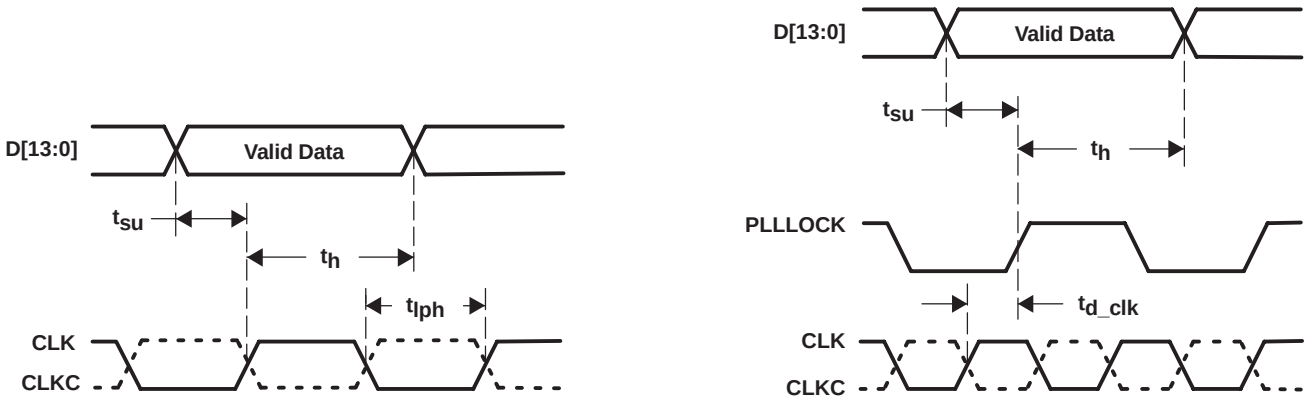


Figure 24. Internal (Left) and External (Right) Clock Mode Timing

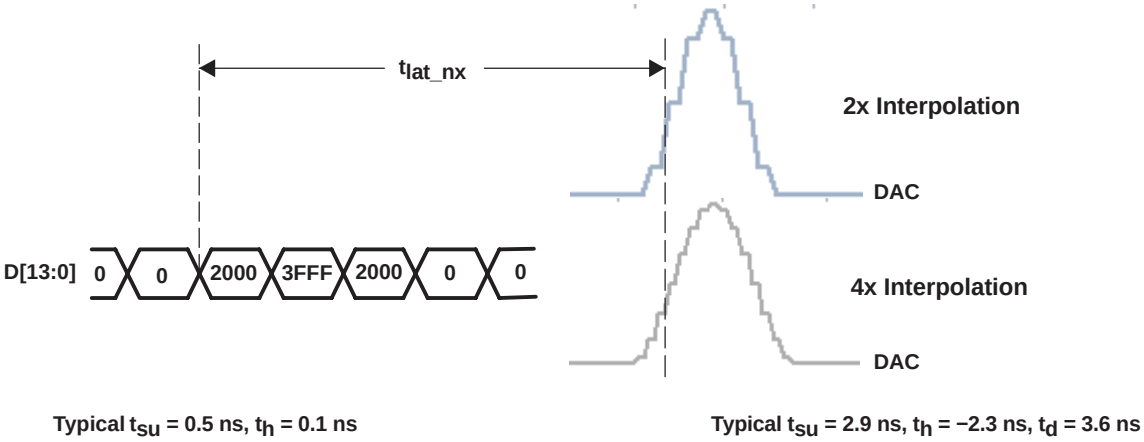


Figure 25. Data to DAC Latency

Figure 26 shows an equivalent circuit for the clock input.

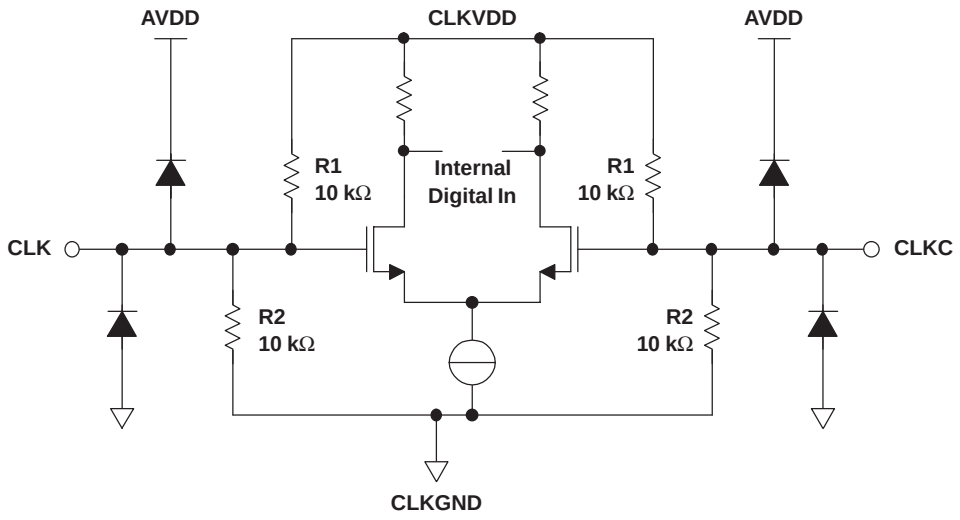


Figure 26. Clock Input Equivalent Circuit

Figure 27, Figure 28, Figure 29, and Figure 30 show various input configurations for driving the differential clock input (CLK/CLKC).

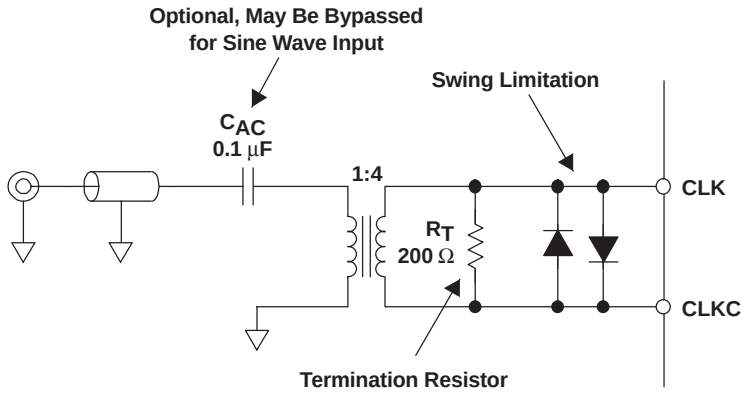


Figure 27. Preferred Clock Input Configuration

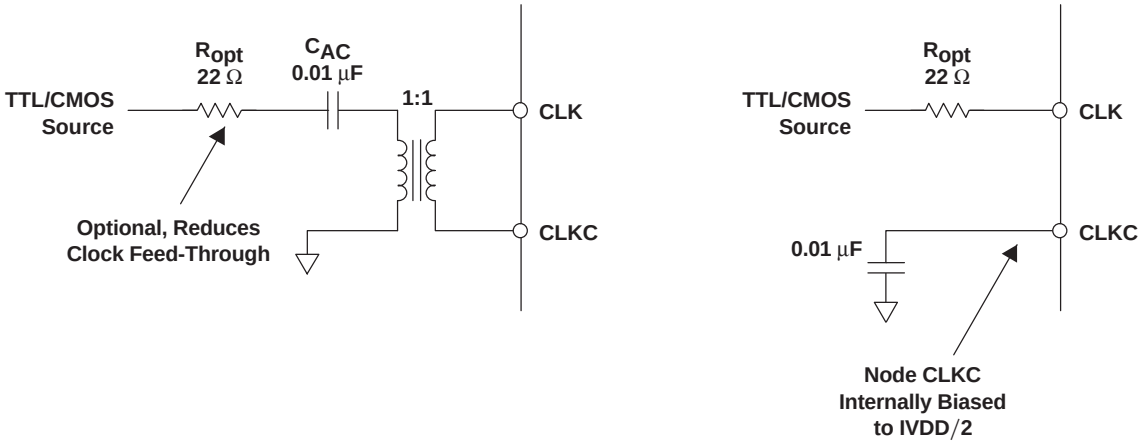


Figure 28. Driving the DAC5674 With a Single-Ended TTL/CMOS Clock Source

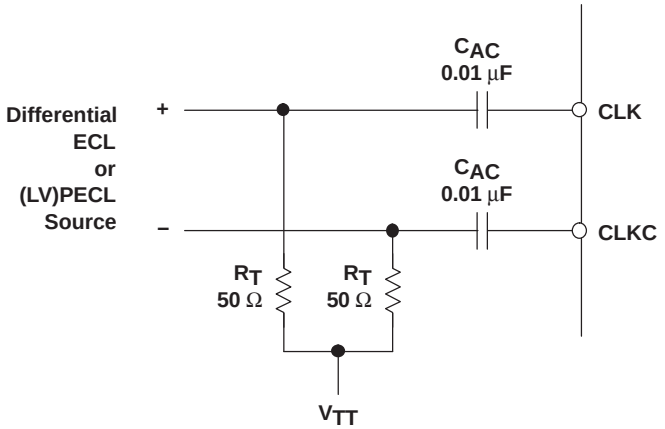


Figure 29. Driving the DAC5674 With Differential ECL/PECL Clock Source

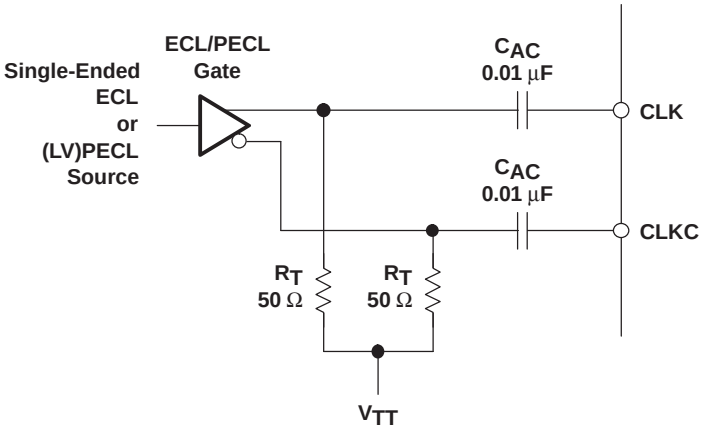


Figure 30. Driving the DAC5674 With a Single-Ended ECL/PECL Clock Source

Supply Inputs

The DAC5674 comprises separate analog and digital supplies at AVDD, DVDD, and IOVDD. These supplies can range from 3 V to 3.6 V for AVDD, 1.65 to 1.95 V for DVDD, and 1.65 to 3.6 for IOVDD.

DAC Transfer Function

The DAC5674 delivers complementary output currents IOUT1 and IOUT2. The DAC supports straight binary coding, with D13 being the MSB and D0 the LSB. Output current IOUT1 equals the approximate full-scale output current when all input bits are set high, i.e., the binary input word has the decimal representation 16383. Full-scale output current flows through terminal IOUT2 when all input bits are set low (mode 0, straight binary input). The relation between IOUT1 and IOUT2 can thus be expressed as:

$$IOUT1 = IOUT_{FS} - IOUT2$$

Where $IOUT_{FS}$ is the full-scale output current. The output currents can be expressed as:

$$IOUT1 = IOUT_{FS} \times \frac{CODE}{16384}$$

$$IOUT2 = IOUT_{FS} \times \frac{16383 - CODE}{16384}$$

Where CODE is the decimal representation of the DAC data input word. Output currents IOUT1 and IOUT2 drive resistor loads (R_L) or a transformer with equivalent input load resistance (R_L). This would translate into single-ended voltages VOUT1 and VOUT2 at terminal IOUT1 and IOUT2, respectively, of:

$$VOUT1 = IOUT1 \times R_L = \frac{CODE}{16384 \times IOUT_{FS} \times R_L}$$

$$VOUT2 = IOUT2 \times R_L = \frac{(16383–CODE)}{16384 \times IOUT_{FS} \times R_L}$$

The differential output voltage $VOUT_{DIFF}$ can thus be expressed as:

$$VOUT_{DIFF} = VOUT1–VOUT2 = \frac{(2CODE–1683)}{16384 \times IOUT_{FS} \times R_L}$$

The latter equation shows that applying the differential output results in doubling of the signal power delivered to the load. Since the output currents IOUT1 and IOUT2 are complementary, they become additive when processed differentially. Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

Reference Operation

The DAC5674 comprises a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 32 times this bias current. The full-scale output current $IOUT_{FS}$ can thus be expressed as:

$$IOUT_{FS} = 32 \times I_{BIAS} = \frac{32 \times V_{EXTIO}}{R_{BIAS}}$$

where V_{EXTIO} is the voltage at terminal EXTIO. The band-gap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor C_{EXT} of 0.1 µF should be connected externally to terminal EXTIO for compensation. The band-gap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the band-gap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 mA.

Analog Current Outputs

Figure 31 shows a simplified schematic of the current source array output with corresponding switches. Differential switches direct the current of each individual PMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to −1 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5674 device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals 1.25 V. Exceeding the maximum output compliance voltage adversely affects distortion performance and integral nonlinearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

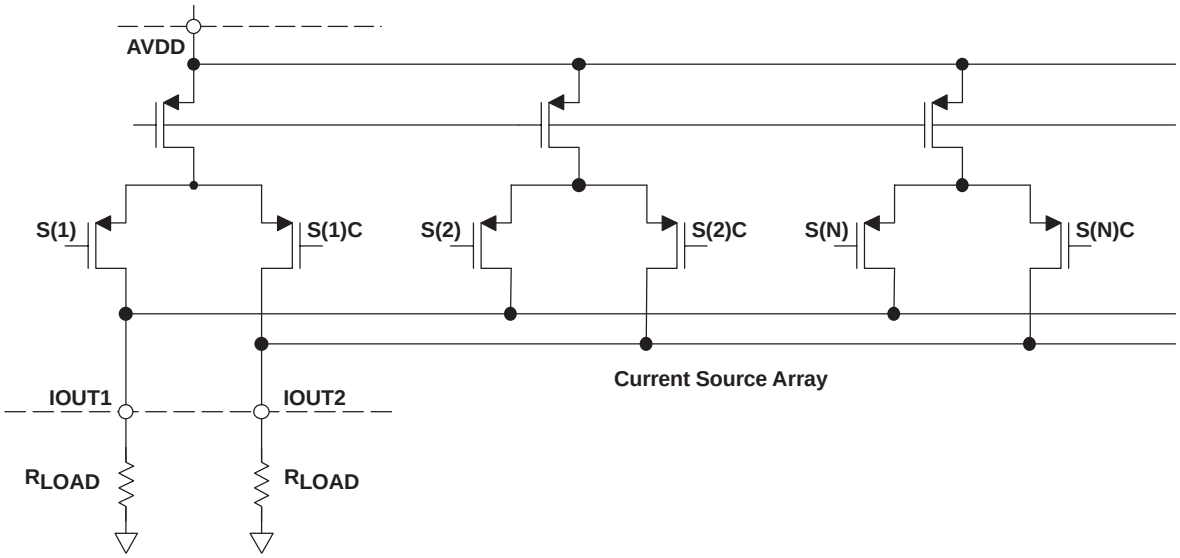


Figure 31. Equivalent Analog Current Output

The DAC5674 can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 19 and Figure 20 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be grounded to enable a DC current flow. Applying a 20-mA full-scale output current would lead to a 0.5 V_{PP} for a 1:1 transformer and a 1 V_{PP} output for a 4:1 transformer.

Figure 21 shows the single-ended output configuration, where the output current IOUT1 flows into an equivalent load resistance of 25 Ω. Node IOUT2 should be connected to AGND or terminated with a resistor of 25 Ω to AGND. The nominal resistor load of 25 Ω gives a differential output swing of 1 V_{PP} when applying a 20-mA full-scale output current.

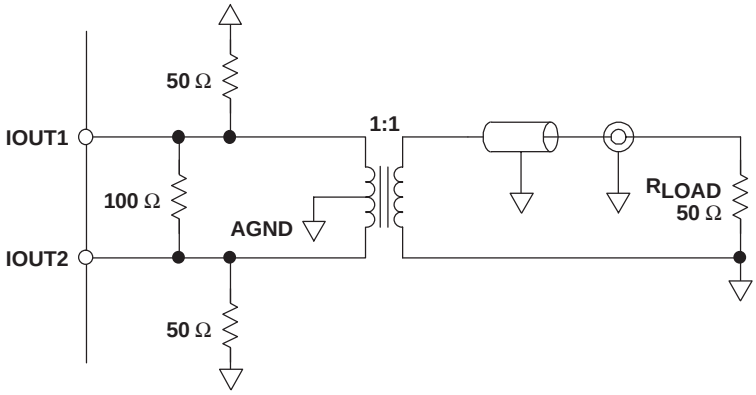


Figure 32. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance Ratio Transformer

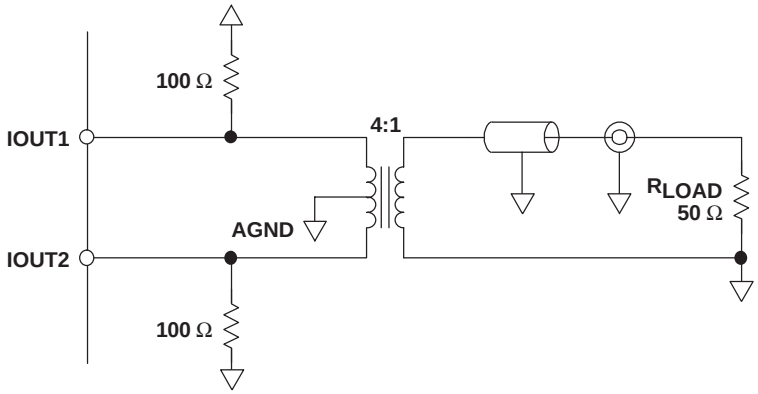


Figure 33. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance Ratio Transformer

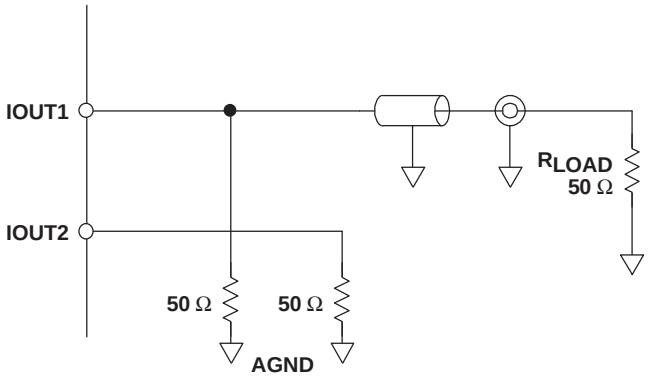


Figure 34. Driving a Doubly Terminated 50-Ω Cable Using Single-Ended Output

Sleep Mode

The DAC5674 features a power-down mode that turns off the output current and reduces the supply current to less than 5 mA over the supply range of 3 V to 3.6 V and temperature range. The power-down mode is activated by applying a logic level 1 to the SLEEP pin (e.g., by connecting pin SLEEP to AVDD). An internal pulldown circuit at node SLEEP ensures that the DAC5674 is enabled if the input is left disconnected. Power-up and power-down activation times depend on the value of external capacitor at node SLEEP. For a nominal capacitor value of 0.1-µF power-down takes less than 5 µs, and power-up takes approximately 3 ms.

DAC5674 Evaluation Board

There is a combo EVM board for the DAC5674 digital-to-analog converter for evaluation. This board allows the user the flexibility to operate the DAC5674 in various configurations. Possible output configurations include transformer coupled, resistor terminated, inverting/noninverting and differential amplifier outputs. The digital inputs are designed to interface with a TMS320 DSP SDK or to be driven directly from various pattern generators with the on-board option to add a resistor network for proper load termination.

PLL LOOP FILTER COMPONENTS

For the external second order filter shown in Figure 35, the components R, C1, and C2 are calculated for a desired phase margin and loop bandwidth. The resistance R3 = 200 Ω and the capacitance is C3 = 8 pF are internal to the DAC5674.

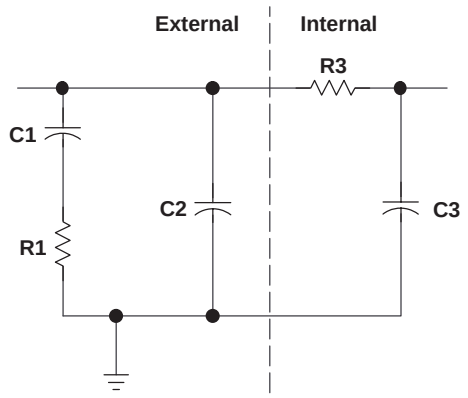


Figure 35. External Second Order Filter

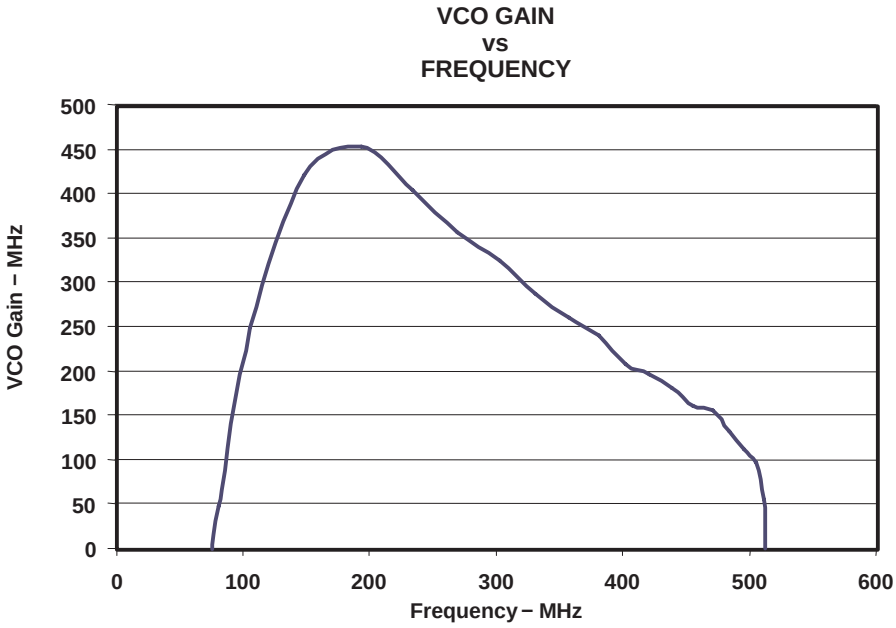


Figure 36. Typical DAC5674 G_{VCO} at 25°C

The VCO gain (G_{VCO}) as a function of VCO frequency for the DAC5674 is shown in Figure 36. For a desired VCO frequency, the loop filter values can be calculated using the equation below.

Nominal PLL design parameters include:

charge pump current: iqp = 1 mA

vco gain: Kvco = 2πxGvco rad/A

prescale/interpolation divide: N = {2,4,8,16,32}

phase detector gain: Kd = iqpx$(2\pi N)^{-1}$ A/rad

Let,

desired loop band width = ω_d

desired phase margin = ϕ_d

then,

$$C1 = \tau1\left(1-\frac{\tau2}{\tau3}\right) \qquad C2 = \frac{\tau1-\tau2}{\tau3} \qquad R = \frac{\tau3^2}{\tau1(\tau3-\tau2)}$$

where

$$\tau1 = \frac{K_d K_{vco}}{{}^{2}_{d}\ \grave{u}}\left(\tan\phi_d + \sec\phi_d\right) \qquad \tau2 = \frac{1}{\omega_d\left(\tan\phi_d + \sec\phi_d\right)} \qquad \tau3 = \frac{\tan\phi_d + \sec\phi_d}{\omega_d}$$

Example:

ϕ_d = 70 degrees, ω_d = 1 MHz

then,

N	R (Ω)	C1 (MF)	C2 (PF)
2	43	0.02	670
4	86	0.01	335
8	173	0.005	167
16	346	0.002	84
32	692	0.001	42

The calculated phase margin and loop band width can be verified by plotting the gain and phase of the open loop transfer function given by:

$$H(s) = \frac{K_{vco}K_d(+\ sRC1)}{s^3RC1C2 + s^2(C1 + C2)}$$

Figure 37 shows the open loop gain and phase for the DAC5674 evaluation board loop filter.

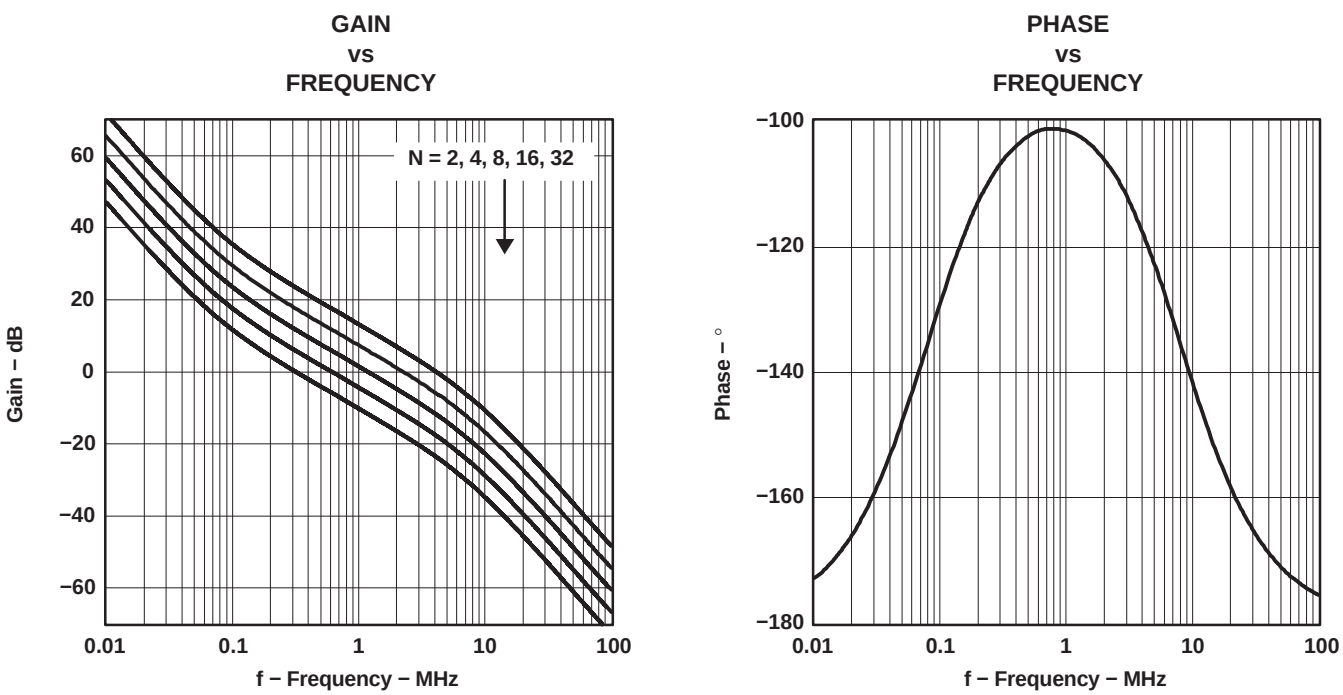


Figure 37. Open Loop Phase and Gain Plots for the DAC5674 Evaluation Board

The phase error (ϕ_{err}) phase and frequency step responses are given by the equations below and are plotted in Figure 24 for the DAC5674 evaluation board loop filter.

$$\phi_{err} = \Delta\phi \times \left[1 + \omega_n t - (\omega_n t)^2\right] \times e^{-\omega_n t}$$ Phase step response

$$\phi_{err} = \frac{\Delta\omega}{\omega_n} \times \left[\omega_n t - (\omega_n t)^2\right] \times e^{-\omega_n t}$$ Frequency step response

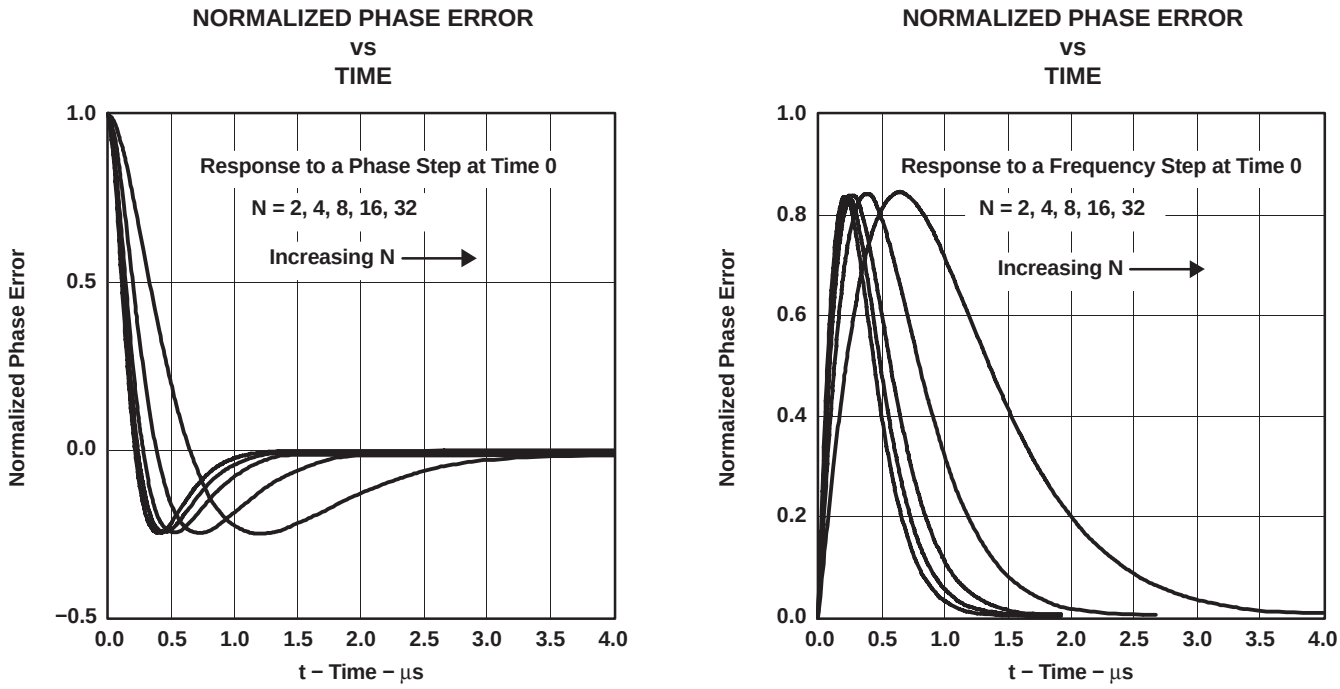
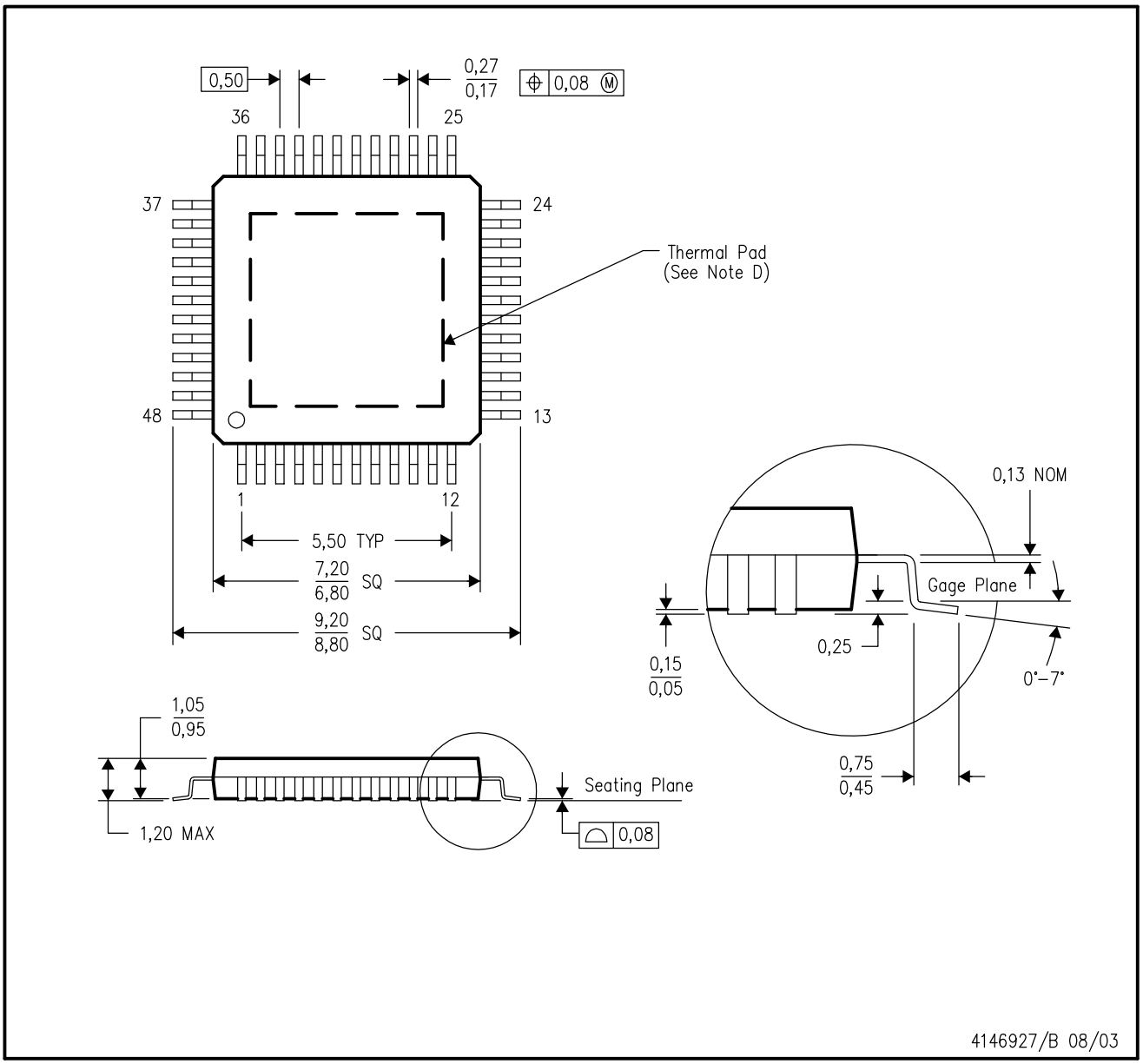


Figure 38. Phase and Frequency Step Responses for the DAC5674 Evaluation Board

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

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