Quad, Serial Input 16-Bit Multiplying Digital-to-Analog Converter

FEATURES

- **Relative Accuracy: 1 LSB Max**
- **Differential Nonlinearity: 1 LSB Max**
- **2-mA Full-Scale Current ±20%, with V_{REF} = ±10 V**
- **0.5 μs Settling Time**
- **Midscale or Zero-Scale Reset**
- **Four Separate 4Q Multiplying Reference Inputs**
- **Reference Bandwidth: 10 MHz**
- **Reference Dynamics: -105 dB THD**
- **SPI™-Compatible 3-Wire Interface: 50 MHz**
- **Double Buffered Registers Enable**
- **Simultaneous Multichannel Change**
- **Internal Power On Reset**
- **Industry-standard Pin Configuration**

APPLICATIONS

- **Automatic Test Equipment**
- **Instrumentation**
- **Digitally Controlled Calibration**

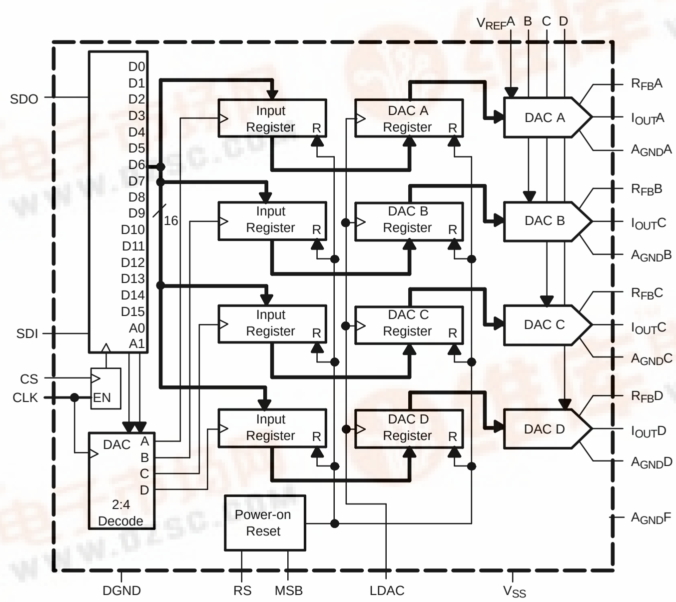
DESCRIPTION

The DAC8814 is a quad, 16-bit, current-output digital-to-analog converter (DAC) designed to operate from a single +2.7 V to 5.0 V supply.

The applied external reference input voltage V_{REF} determines the full-scale output current. An internal feedback resistor (R_{FB}) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier.

A doubled buffered serial data interface offers high-speed, 3-wire, SPI and microcontroller compatible inputs using serial data in (SDI), clock (CLK), and a chip-select ($\overline{CS}$). In addition, a serial data out pin (SDO) allows for daisy-chaining when multiple packages are used. A common level-sensitive load DAC strobe ($\overline{LDAC}$) input allows simultaneous update of all DAC outputs from previously loaded input registers. Additionally, an internal power on reset forces the output voltage to zero at system turn on. An MSB pin allows system reset assertion ($\overline{RS}$) to force all registers to zero code when MSB = 0, or to half-scale code when MSB = 1.

The DAC8814 is available in an SSOP package.



PRODUCT PREVIEW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola, Inc.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC8814C	±1	±1	-40°C to +85°C	SSOP-28	DB	DAC8814ICDBT	Tape and Reel, 250
						DAC8814ICDBR	Tape and Reel, 2500
DAC8814B	±4	±1.5	-40°C to +85°C	SSOP-28	DB	DAC8814IBDBT	Tape and Reel, 250
						DAC8814IBDBR	Tape and Reel, 2500

(1) For the most current specifications and package information, see the Package Option Addendum located at the end of this data sheet or refer to our web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS(1)

		DAC8814	UNIT
V_{DD} to GND		-0.3 to +8	V
V_{SS} to GND		-0.3 to -7	V
V_{REF} to GND		-18 to +18	V
Logic inputs and output to GND		-0.3 to + 8	V
$V(I_{OUT})$ to GND		-0.3 to V_{DD} + 0.3	V
$A_{GND}X$ to DGND		-0.3 to +0.3	V
Input current to any pin except supplies		±50	mA
Package power dissipation		$(T_J max - T_A)/\theta_{JA}$	
Thermal resistance, θ_{JA}	28-Lead shrink surface-mount (RS-28)	100	°C/W
Maximum junction temperature ($T_J$max)		150	°C
Operating temperature range, Model A		-40 to +85	°C
Storage temperature range		-65 to + 150	°C
Lead temperature	RS-28 (Vapor phase 60s)	215	°C
	RS-28 (Infrared 15s)	220	°C

(1) Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS(1)

V_{DD} = 2.7 V to 5.0 V ±10%; V_{SS} = 0 V, I_{OUT}X = Virtual GND, A_{GND}X = 0 V, V_{REF}A, B, C, D = 10 V, T_A = full operating temperature range, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC8814 MIN	DAC8814 TYP	DAC8814 MAX	UNIT
STATIC PERFORMANCE(2)						
Resolution					16	Bits
Relative accuracy	INL	DAC8814B			±4	LSB
	INL	DAC8814C			±1	LSB
Differential nonlinearity	DNL	DAC8814B			±1.5	LSB
	DNL	DAC8814C			±1	LSB
Output leakage current	I_{OUT}X	Data = 0000h, T_A = 25°C			10	nA
	I_{OUT}X	Data = 0000h, T_A = T_A max			20	nA
Full-scale gain error	G_{FSE}	Data = FFFFh		±0.75	±3	mV
Full-scale tempco(3)	TCV_{FS}			1		ppm/°C
Feedback resistor	R_{FB}X	V_{DD} = 5 V		5		kΩ
REFERENCE INPUT						
V_{REF}X Range	V_{REF}X		-15		15	V
Input resistance	R_{REF}X		4	6	8	kΩ
Input resistance match	R_{REF}X	Channel-to-channel		1		%
Input capacitance(3)	C_{REF}X			5		pF
ANALOG OUTPUT						
Output current	I_{OUT}X	Data = FFFFh	1.25		2.5	mA
Output capacitance(3)	C_{OUT}X	Code-dependent		80		pF
LOGIC INPUTS AND OUTPUT						
Input low voltage	V_{IL}	V_{DD} = +2.7 V			0.6	V
	V_{IL}	V_{DD} = +5 V			0.8	V
Input high voltage	V_{IH}	V_{DD} = +2.7 V	2.1			V
	V_{IH}	V_{DD} = +5 V	2.4			V
Input leakage current	I_{IL}				1	µA
Input capacitance(3)	C_{IL}				10	pF
Logic output low voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Logic output high voltage	V_{OH}	I_{OH} = 100 µA	4			V
INTERFACE TIMING(3), (4)						
Clock width high	t_{CH}		25			ns
Clock width low	t_{CL}		25			ns
$\overline{CS}$ to Clock setup	t_{CSS}		0			ns
Clock to $\overline{CS}$ hold	t_{CSH}		25			ns
Clock to SDO prop delay	t_{PD}		2		20	ns
Load DAC pulsewidth	t_{LDAC}		25			ns
Data setup	t_{DS}		20			ns
Data hold	t_{DH}		20			ns
Load setup	t_{LDS}		5			ns
Load hold	t_{LDH}		25			ns

PRODUCT PREVIEW

(1) Specifications subject to change without notice.
(2) All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision OPA277 I-to-V converter amplifier. The DAC8814 R_{FB} terminal is tied to the amplifier output. Typical values represent average readings measured at +25°C.
(3) These parameters are specified by design and not subject to production testing.
(4) All input control signals are specified with t_R = t_F = 2.5 ns (10% to 90% of 3 V) and timed from a voltage level of 1.5 V.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7 V to 5.0 V ±10%; V_{SS} = 0 V, $I_{OUT}X$ = Virtual GND, $A_{GND}X$ = 0 V, V_{REF}A, B, C, D = 10 V, T_A = full operating temperature range, unless otherwise noted.

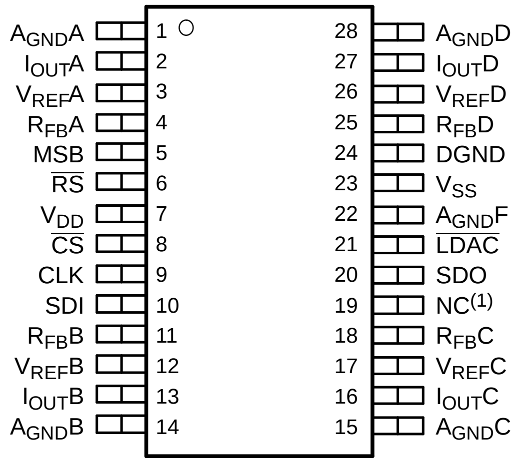
PARAMETER	SYMBOL	CONDITIONS	DAC8814 MIN	TYP	MAX	UNIT
SUPPLY CHARACTERISTICS						
Power supply range	$V_{DD\ RANGE}$		2.7		5.5	V
Positive supply current	I_{DD}	Logic inputs = 0 V		2	5	µA
	I_{DD}	V_{DD} = +4.5 V to +5.5 V		2	5	µA
	I_{DD}	V_{DD} = +2.7 V to +3.6 V		1	2.5	µA
Negative supply current	I_{SS}	Logic inputs = 0 V, V_{SS} = -5 V		0.001	1	µA
Power dissipation	P_{DISS}	Logic inputs = 0 V			0.0275	mW
Power supply sensitivity	P_{SS}	ΔV_{DD} = ±5%			0.006	%
AC CHARACTERISTICS[(5)]						
Output voltage settling time	t_s	To ±0.1% of full-scale, Data = 0000h to FFFFh to 0000h		0.5		µs
	t_s	To ±0.0051% of full-scale, Data = 0000h to FFFFh to 0000h		1		µs
Reference multiplying BW	BW -3 dB	$V_{REF}X$ = 100 mV_{RMS}, Data = $FFFF_H$, C_{FB} = 15 pF		10		MHz
DAC glitch impulse	Q	$V_{REF}X$ = 10 V, Data = 0000h to 8000h to 0000h		1		nV/s
Feedthrough error	$V_{OUT}X/V_{REF}X$	Data = 0000h, $V_{REF}X$ = 100 mV_{RMS}, f = 100 kHz		-70		dB
Crosstalk error	$V_{OUT}A/V_{REF}B$	Data = 0000h, $V_{REF}B$ = 100 mV_{RMS}, Adjacent channel, f = 100 kHz		-90		dB
Digital feedthrough	Q	$\overline{CS}$ = 1 and f_{CLK} = 1 MHz		2		nV/s
Total harmonic distortion	THD	V_{REF} = 5 V_{PP}, Data = FFFFh, f = 1 kHz		-105		dB
Output spot noise voltage	e_n	f = 1 kHz, BW = 1 Hz		12		$nV/\sqrt{Hz}$

(5) All ac characteristic tests are performed in a closed-loop system using an OPA627 I-to-V converter amplifier.

PRODUCT PREVIEW

PIN CONFIGURATIONS

DAC8814
(TOP VIEW)



NOTE (1): NC − No internal connection

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1, 14, 15, 28	A_{GND}A, A_{GND}B, A_{GND}C, A_{GND}D	DAC A, B, C, D Analog ground.
2, 13, 16, 27	I_{OUT}A, I_{OUT}B, I_{OUT}C, I_{OUT}D	DAC A, B, C, D Current output.
3, 12, 17, 26	V_{REF}A, V_{REF}B, V_{REF}C, V_{REF}D	DAC A, B, C, D Reference voltage input terminal. Establishes DAC A, B, C, D full-scale output voltage. Can be tied to V_{DD}.
4, 11, 18, 25	R_{FB}A, R_{FB}B, R_{FB}C, R_{FB}D	Establish voltage output for DAC A, B, C, D by connecting to external amplifier output.
5	MSB	MSB Bit set during a reset pulse (RS) or at system power on if tied to ground or V_{DD}.
6	$\overline{RS}$	Reset pin, active low. Input register and DAC registers are set to all zeros or half scale code (8000h) determined by the voltage on the MSB pin. Register data = 8000h when MSB = 1.
7	V_{DD}	Positive power supply input. Specified range of operation 5 V ±10%.
8	$\overline{CS}$	Chip-select; active low input. Disables shift register loading when high. Transfers shift register data to input register when CS/LDAC goes high. Does not affect LDAC operation.
9	CLK	Clock input; positive edge triggered clocks data into shift register
10	SDI	Serial data input; data loads directly into the shift register.
19	NC	Not connected; leave floating.
20	SDO	Serial data output; input data loads directly into shift register. Data appears at SDO, 19 clock pulses after input at the SDI pin.
21	$\overline{LDAC}$	Load DAC register strobe; level sensitive active low. Tranfers all input register data to the DAC registers. Asynchronous active low input. See Table 1 for operation.
22	A_{GND}F	High current analog force ground.
23	V_{SS}	Negative bias power-supply input. Specified range of operation -0.3 V to -5.5 V.
24	DGND	Digital ground.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 1.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 2.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 3.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 4.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 5.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 6.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 7.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 8.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 9.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 10.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 11.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 12.

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, +V_{DD} = +5 V, unless otherwise noted.

Channel C

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 13.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 14.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 15.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 16.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 17.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 18.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, $+V_{DD}$ = +5 V, unless otherwise noted.

Channel D

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 19.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 20.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 21.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 22.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, +V_{DD} = +5 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 23.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 24.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

At T_A = +25°C, +V_{DD} = +5 V, unless otherwise noted.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

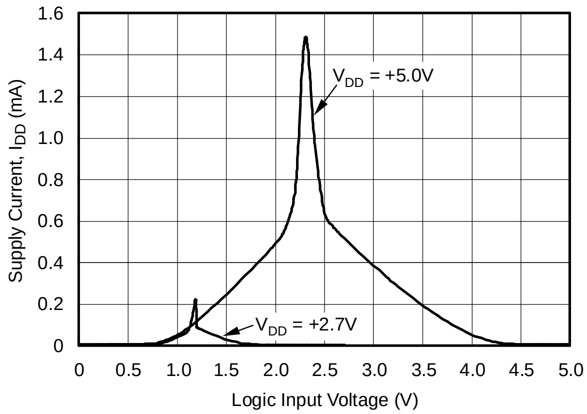


Figure 25.

REFERENCE MULTIPLYING BANDWIDTH

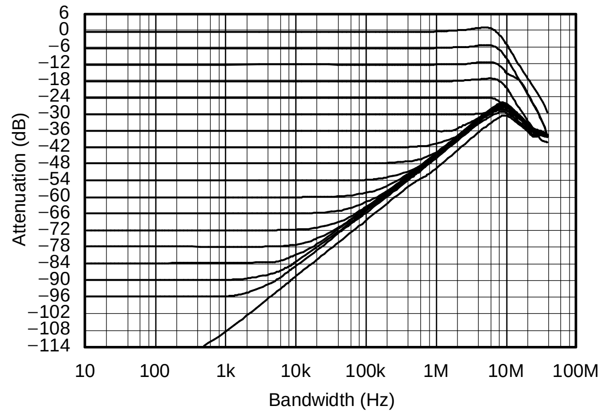


Figure 26.

DAC GLITCH

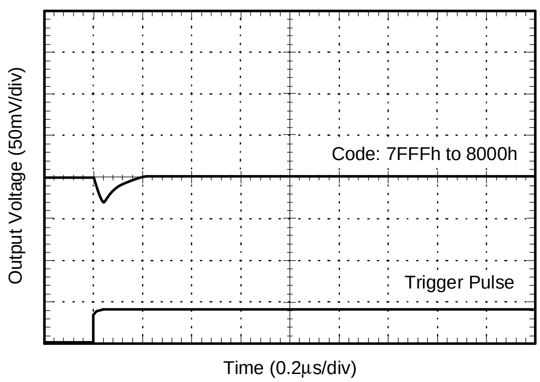


Figure 27.

DAC SETTLING TIME

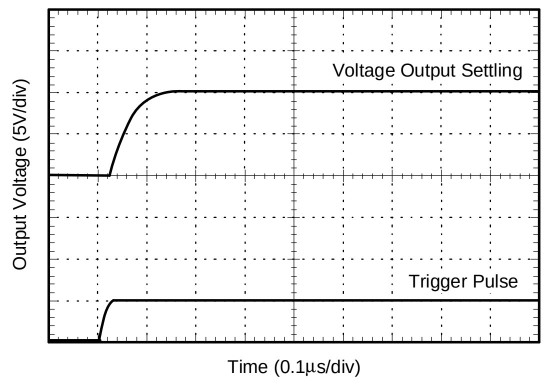


Figure 28.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V

At T_A = +25°C, $+V_{DD}$ = +2.7 V, unless otherwise noted.

Channel A

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 29.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 30.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 31.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 32.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7 V, unless otherwise noted.

LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 33.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 34.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, +V_{DD} = +2.7 V, unless otherwise noted.

Channel B

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 35.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 36.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 37.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 38.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, +V_{DD} = +2.7 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 39.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 40.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, +V_{DD} = +2.7 V, unless otherwise noted.

Channel C

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 41.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 42.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 43.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 44.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, +V_{DD} = +2.7 V, unless otherwise noted.

LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 45.

DIFFERENTIAL LINEARITY ERROR
vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 46.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, +V_{DD} = +2.7 V, unless otherwise noted.

Channel D

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 47.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 48.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 49.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 50.

TYPICAL CHARACTERISTICS: V_{DD} = +2.7 V (continued)

At T_A = +25°C, $+V_{DD}$ = +2.7 V, unless otherwise noted.

LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 51.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

Graphic Forthcoming

Figure 52.

PARAMETER MEASUREMENT INFORMATION

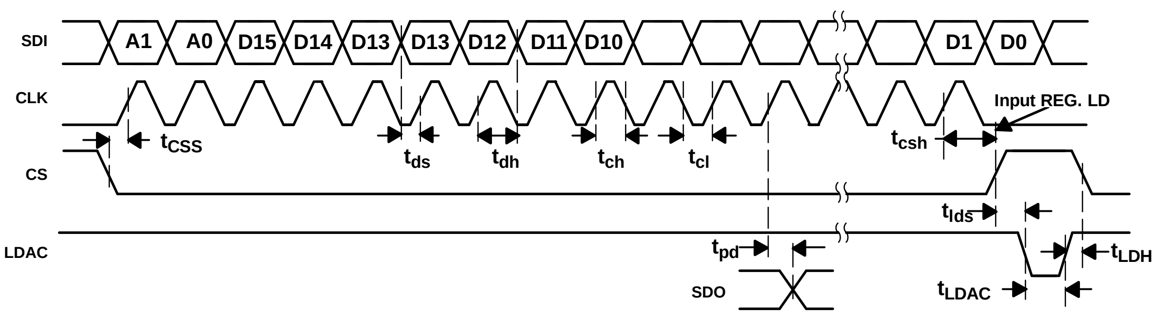


Figure 53. DAC8814 Timing Diagram

THEORY OF OPERATION

CIRCUIT OPERATION

The DAC8814 contains four, 16-bit, current-output, digital-to-analog converters (DACs) respectively. Each DAC has its own independent multiplying reference input. The DAC8814 uses a 3-wire SPI compatible serial data interface, with a configurable asynchronous $\overline{RS}$ pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an $\overline{LDAC}$ strobe enables four channel simultaneous updates for hardware synchronized output voltage changes.

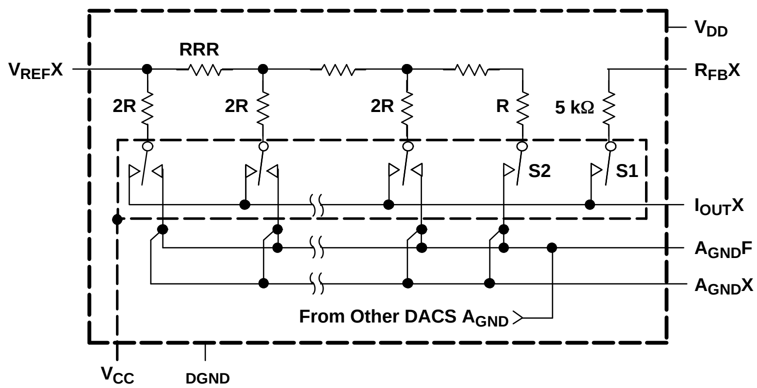
D/A Converter

The DAC8814 contains four current-steering R-2R ladder DACs. Figure 54 shows a typical equivalent DAC. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The R_{FB}X pin is connected to the output of the external amplifier. The I_{OUT}X terminal is connected to the inverting input of the external amplifier. The A_{GND}X pin should be Kelvin-connected to the load point in the circuit requiring the full 16-bit accuracy.

The DAC is designed to operate with both negative or positive reference voltages. The V_{DD} power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5 kΩ feedback resistor. If users are attempting to measure the value of R_{FB}, power must be applied to V_{DD} in order to achieve continuity. An additional V_{SS} bias pin is used to guard the substrate during high temperature applications to minimize zero-scale leakage currents that double every 10°C. The DAC output voltage is determined by V_{REF} and the digital data (D) according to Equation 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{65536} \qquad (1)$$

Note that the output polarity is opposite of the V_{REF} polarity for dc reference voltages.



Digital Interface Connections Omitted For Clarity.
Switches S1 and S2 are Closed, V_{DD} Most be Powered.

Figure 54. Typical Equivalent DAC Channel

The DAC is also designed to accommodate ac reference input signals. The DAC8814 accommodates input reference voltages in the range of -12 V to +12 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 kΩ, ± 30%. On the other hand, the DAC outputs I_{OUT}A, B, C, D are code-dependent and produce various output resistances and capacitances.

The choice of external amplifier should take into account the variation in impedance generated by the DAC8814 on the amplifiers' inverting input node. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor (C_{FB}) may be needed to provide a critically damped output response for step changes in reference input voltages.

Figure 26 shows the gain vs frequency performance at various attenuation settings using a 23 pF external feedback capacitor connected across the I_{OUT}X and R_{FB}X terminals. In order to maintain good analog performance, power supply bypassing of 0.01 µF, in parallel with 1 µF, is recommended. Under these conditions, clean power supply with low ripple voltage capability should be used. Switching power supplies is usually not suitable for this application due to the higher ripple voltage and P_{SS} frequency-dependent characteristics. It is best to derive the DAC8814 5-V supply from the system analog supply voltages. (Do not use the digital 5-V supply.) See Figure 55.

PRODUCT PREVIEW

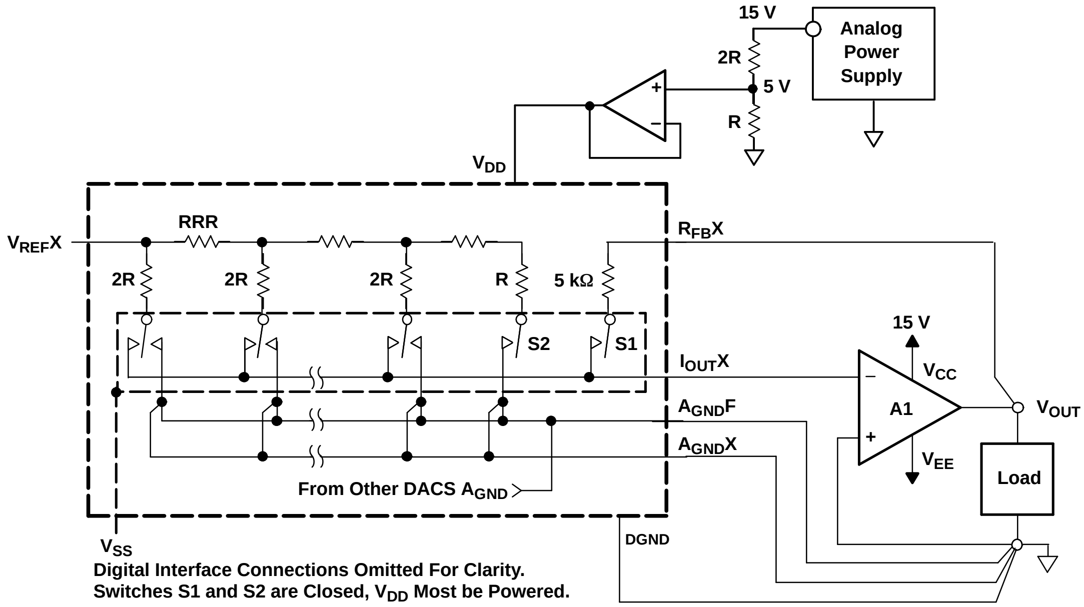


Figure 55. Recommended Kelvin-Sensed Hookup

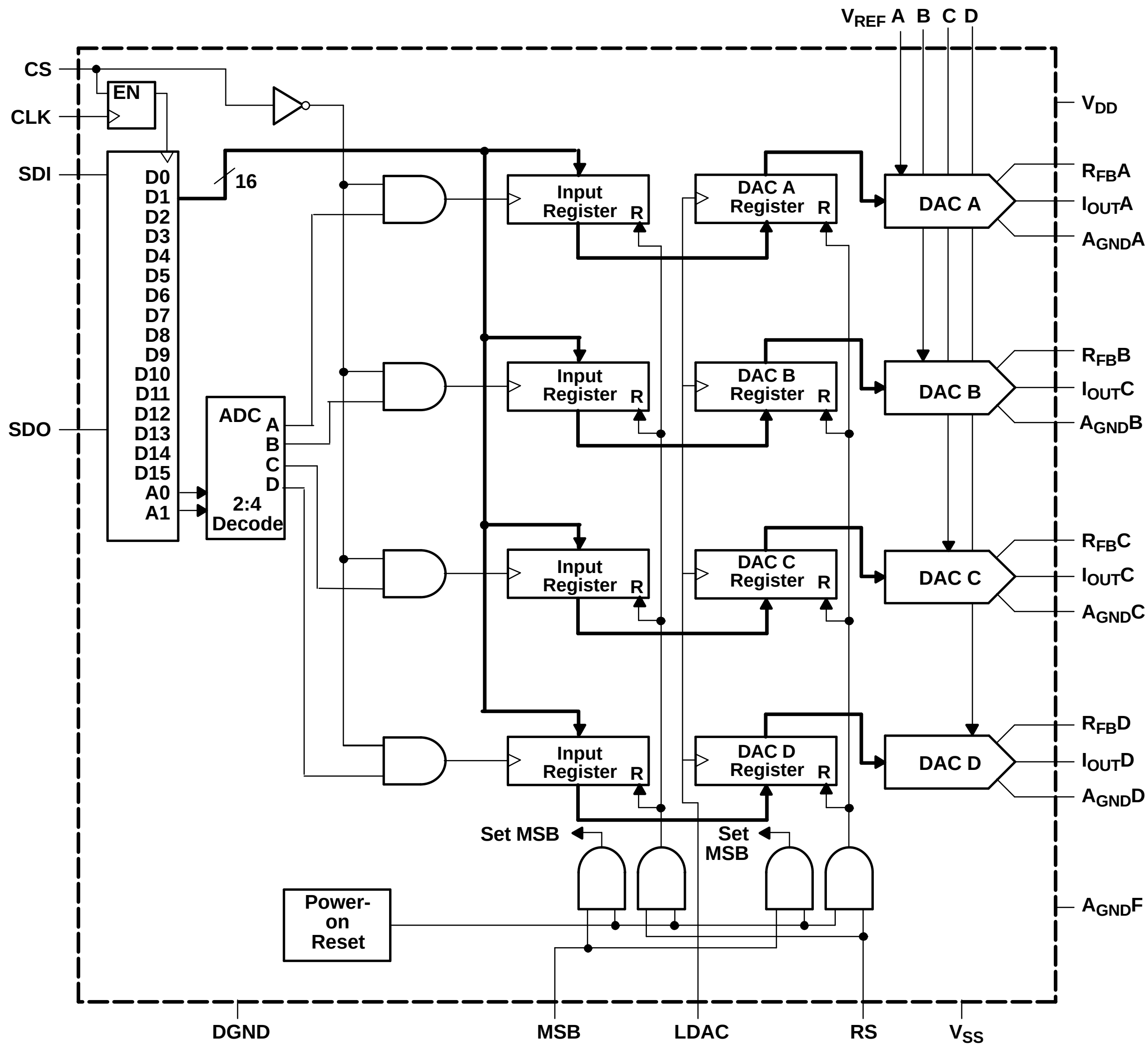


Figure 56. System Level Digital Interfacing

SERIAL DATA INTERFACE

The DAC8814 uses a 3-wire ($\overline{CS}$, SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8814 is clocked into the serial input register in an 16-bit data-word format. MSB bits are loaded first. Table 2 defines the 16 data-word bits for the DAC8814.

Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing Specifications. Data can only be clocked in while the $\overline{CS}$ chip select pin is active low. For the DAC8814, only the last 16 bits clocked into the serial register are interrogated when the $\overline{CS}$ pin returns to the logic high state.

Since most microcontrollers output serial data in 8-bit bytes, three right-justified data bytes can be written to the DAC8814. Keeping the $\overline{CS}$ line low between the first, second, and third byte transfers results in a successful serial register update. Similarly, two right-justified data bytes can be written to the DAC8814. Keeping the $\overline{CS}$ line low between the first and second byte transfer will result in a successful serial register update.

PRODUCT PREVIEW

Once the data is properly aligned in the shift register, the positive edge of the $\overline{CS}$ initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1and A0. For the DAC8814, Table 1, Table 2, Table 3 and Figure 53 define the characteristics of the software serial interface. Figure 57 shows the equivalent logic interface for the key digital control pins for the DAC8814.

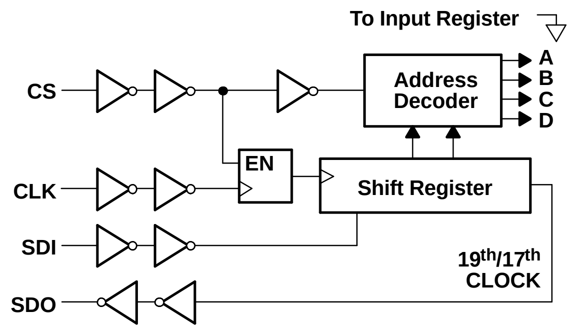


Figure 57. DAC8814 Equivalent Logic Interface

Two additional pins $\overline{RS}$ and MSB provide hardware control over the preset function and DAC register loading. If these functions are not needed, the $\overline{RS}$ pin can be tied to logic high. The asynchronous input $\overline{RS}$ pin forces all input and DAC registers to either the zero-code state (MSB = 0), or the half-scale state (MSB = 1).

POWER ON RESET

When the V_{DD} power supply is turned on, an internal reset strobe forces all the Input and DAC registers to the zero-code state or half-scale, depending on the MSB pin voltage. The V_{DD} power supply should have a smooth positive ramp without drooping in order to have consistent results, especially in the region of V_{DD} = 1.5 V to 2.3 V. The V_{SS} supply has no effect on the power-on reset performance. The DAC register data stays at zero or half-scale setting until a valid serial register data load takes place.

ESD Protection Circuits

All logic-input pins contain back-biased ESD protection zener diodes connected to ground (DGND) and V_{DD} as shown in Figure 58.

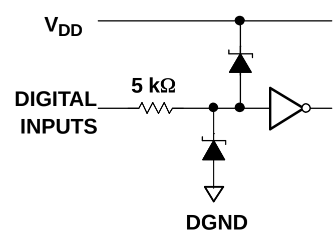


Figure 58. Equivalent ESD Protection Circuits

PRODUCT PREVIEW

PCB LAYOUT

In printed circuit board (PCB) layout, all analog ground $A_{GND}X$ should be tied together.

Table 1. Control Logic Truth Table(1)

$\overline{CS}$	CLK	$\overline{LDAC}$	$\overline{RS}$	MSB	SERIAL SHIFT REGISTER	INPUT REGISTER	DAC REGISTER
H	X	H	H	X	No effect	Latched	Latched
L	L	H	H	X	No effect	Latched	Latched
L	↑+	H	H	X	Shift register data advanced one bit	Latched	Latched
L	H	H	H	X	No effect	Latched	Latched
↑+	L	H	H	X	No effect	Selected DAC updated with current SR contents	Latched
H	X	L	H	X	No effect	Latched	Transparent
H	X	H	H	X	No effect	Latched	Latched
H	X	↑+	H	X	No effect	Latched	Latched
H	X	H	L	0	No effect	Latched data = 0000h	Latched data = 0000h
X	↑+	H	L	H	No effect	Latched data = 8000h	Latched data = 8000h

(1) **↑+** = Positive logic transition; **X** = Do not care

Table 2. Serial Input Register Data Format, Data Loaded MSB First(1)

Bit	B17 (MSB)	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0 (LSB)
Data	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

(1) Only the last 18 bits of data clocked into the serial register (address + data) are inspected when the $\overline{CS}$ line positive edge returns to logic high. At this point an internally-generated load strobe transfers the serial register data contents (bits D15-D0) to the decoded DAC-input-register address determined by bits A1 and A0. Any extra bits clocked into the DAC8814 shift register are ignored, only the last 18 bits clocked in are used. If double-buffered data is not needed, the $\overline{LDAC}$ pin can be tied logic low to disable the DAC registers.

Table 3. Address Decode

A1	A0	DAC DECODE
0	0	DAC A
0	1	DAC B
1	0	DAC C
1	1	DAC D

PRODUCT PREVIEW

APPLICATION INFORMATION

The DAC8814, a 2-quadrant multiplying DAC, can be used to generate a unipolar output. The polarity of the full-scale output I_{OUT} is the inverse of the input reference voltage at V_{REF}.

Some applications require full 4-quadrant multiplying capabilities or bipolar output swing, as shown in Figure 59. An additional external op amp A2 is added as a summing amp. In this circuit the first and second amps (A1 and A2) provide a gain of 2X that widens the output span to 20 V. A 4-quadrant multiplying circuit is implemented by using a 10-V offset of the reference voltage to bias A2. According to the following circuit transfer equation (Equation 2), input data (D) from code 0 to full scale produces output voltages of V_{OUT} = -10 V to V_{OUT} = 10 V.

$$V_{OUT} = \left(\frac{D}{32,768} - 1\right) \times V_{REF} \quad (2)$$

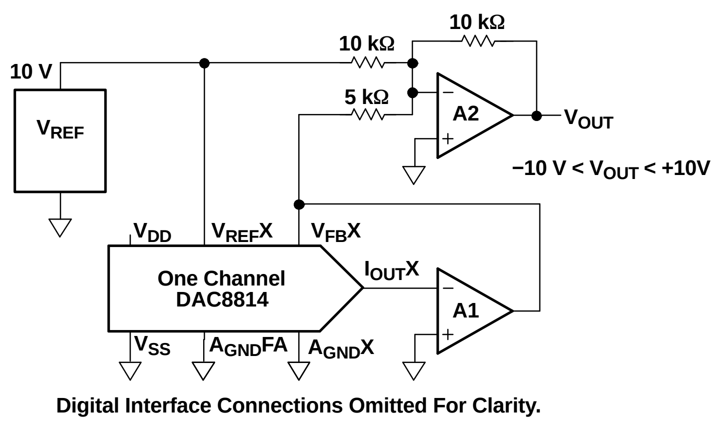


Figure 59. Four-Quadrant Multiplying Application Circuit

Cross-Reference

The DAC8814 has an industry-standard pinout. Table 4 provides the cross-reference information.

Table 4. Cross-Reference

PRODUCT	INL (LSB)	DNL (LSB)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESCRIPTION	PACKAGE OPTION	CROSS-REFERENCE PART
DAC8814ICDB	±1	±1	-40°C to +85°C	28-Lead MicroSOIC	SSOP-28	N/A
DAC8814IBDB	±4	±1.5	-40°C to +85°C	28-Lead MicroSOIC	SSOP-28	AD5544RS

PRODUCT PREVIEW

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC8814IBDBR	PREVIEW	SSOP	DB	28	2500	TBD	Call TI	Call TI
DAC8814IBDBT	PREVIEW	SSOP	DB	28	250	TBD	Call TI	Call TI
DAC8814ICDBR	PREVIEW	SSOP	DB	28	2500	TBD	Call TI	Call TI
DAC8814ICDBT	PREVIEW	SSOP	DB	28	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

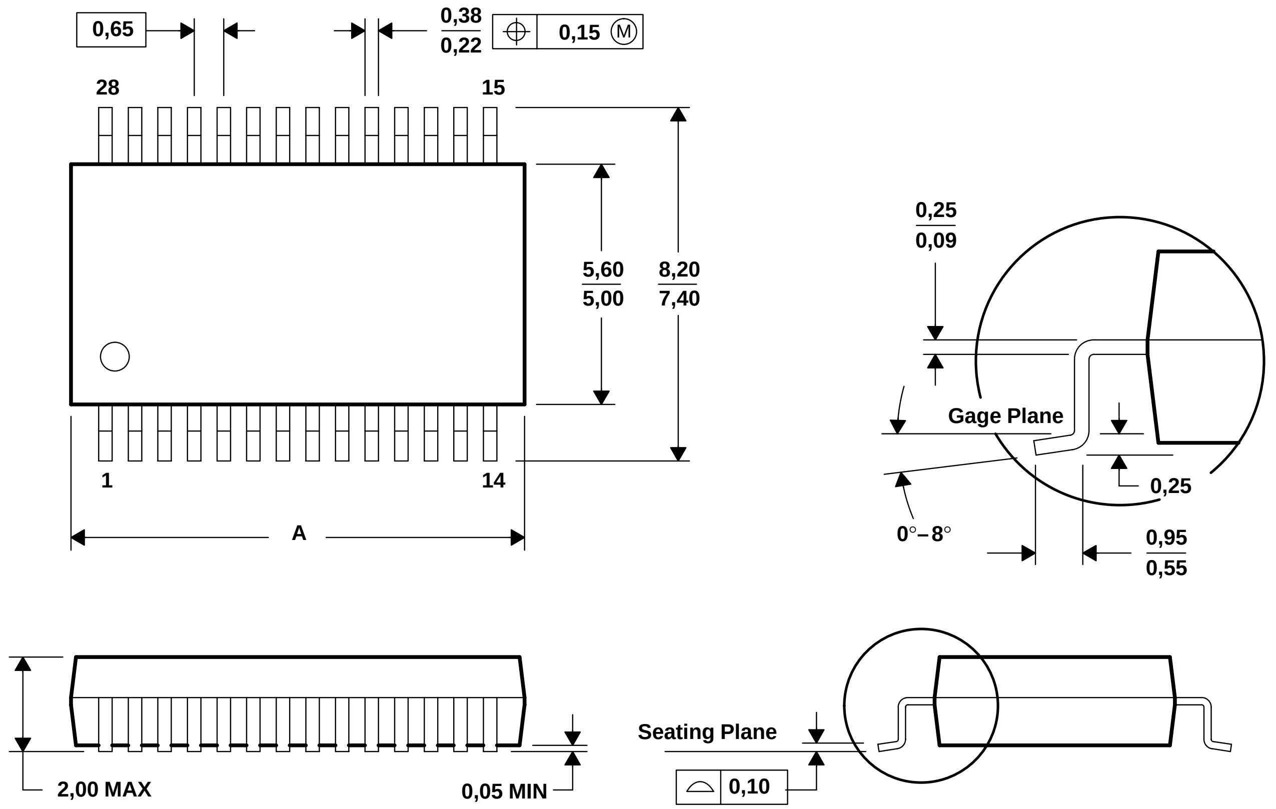
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150