ULTRALOW-NOISE, HIGH PSRR, FAST RF 250-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- 250-mA Low-Dropout Regulator With Enable
- Available in 1.8 V, 2.5 V, 2.8 V, 3 V, 3.3 V, and Adjustable (1.2 V to 5.5 V)
- High PSRR (60 dB at 10 kHz)
- Ultralow Noise (32 μVrms, TPS79428)
- Fast Start-Up Time (50 μs)
- Stable With a 2.2-μF Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (155 mV at Full Load)
- Available in MSOP-8 and SOT223-6 Packages

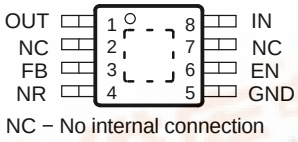
APPLICATIONS

- RF: VCOs, Receivers, ADCs
- Audio
- Bluetooth™, Wireless LAN
- Cellular and Cordless Telephones
- Handheld Organizers, PDAs

DESCRIPTION

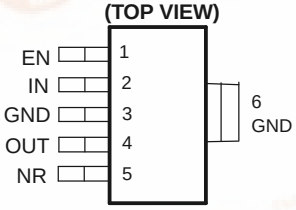
The TPS794xx family of low-dropout (LDO) linear voltage regulators features high power-supply rejection ratio (PSRR), ultralow-noise, fast start-up, and excellent line and load transient responses in small outline, MSOP-8 PowerPAD™ and SOT223-6 packages. Each device in the family is stable with a small 2.2-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 155 mV at 250 mA). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79428 exhibits approximately 32 μV_{RMS} of output voltage noise at 2.8 V output with a 0.1-μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

DGN PACKAGE
MSOP PowerPAD
(TOP VIEW)

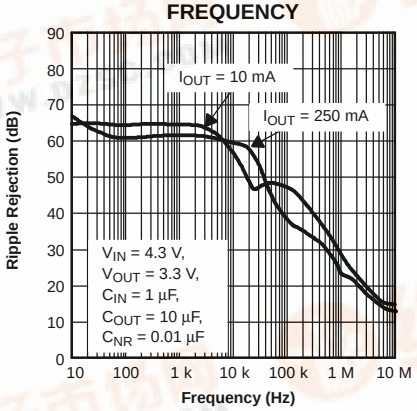


NC − No internal connection

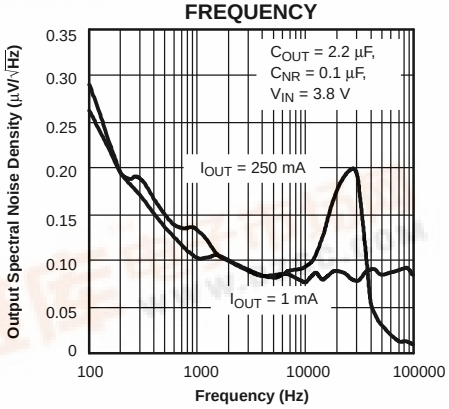
DCQ PACKAGE
SOT223-6
(TOP VIEW)



TPS79433
RIPPLE REJECTION
vs
FREQUENCY



TPS79428
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	VOLTAGE	PACKAGE	T_J	SYMBOL	PART NUMBER	TRANSPORT MEDIA, QUANTITY
TPS79401	Adjustable	MSOP-8	-40°C to 125°C	AXL	TPS79401DGNR	Tape and Reel, 2500
					TPS79401DGNT	Tape and Reel, 250
		SOT223-6		PS79401	TPS79401DCQR	Tape and Reel, 2500
					TPS79401DCQ	Tube, 78
TPS79418	1.8 V	MSOP-8		AXM	TPS79418DGNR	Tape and Reel, 2500
					TPS79418DGNT	Tape and Reel, 250
		SOT223-6		PS79418	TPS79418DCQR	Tape and Reel, 2500
					TPS79418DCQ	Tube, 78
TPS79423	2.5 V	MSOP-8		AYB	TPS79425DGNR	Tape and Reel, 2500
					TPS79425DGNT	Tape and Reel, 250
		SOT223-6		PS79425	TPS79425DCQR	Tape and Reel, 2500
					TPS79425DCQ	Tube, 78
TPS79428	2.8 V	MSOP-8		AYC	TPS79428DGNR	Tape and Reel, 2500
					TPS79428DGNT	Tape and Reel, 250
		SOT223-6		PS79428	TPS79428DCQR	Tape and Reel, 2500
					TPS79428DCQ	Tube, 78
TPS79430	3 V	MSOP-8		AYD	TPS79430DGNR	Tape and Reel, 2500
					TPS79430DGNT	Tape and Reel, 250
		SOT223-6		PS79430	TPS79430DCQR	Tape and Reel, 2500
					TPS79430DCQ	Tube, 78
TPS79433	3.3 V	MSOP-8		AYE	TPS79433DGNR	Tape and Reel, 2500
					TPS79433DGNT	Tape and Reel, 250
		SOT223-6		PS79433	TPS79433DCQR	Tape and Reel, 2500
					TPS79433DCQ	Tube, 78

ABSOLUTE MAXIMUM RATINGS

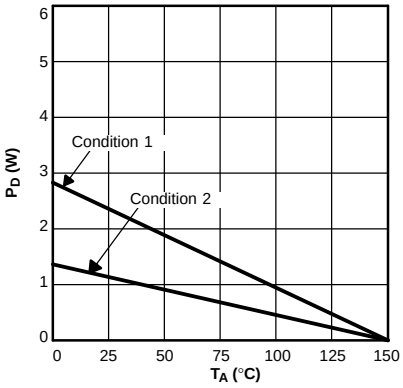
over operating temperature range unless otherwise noted(1)

	VALUE
V_{IN} range	-0.3 V to 6 V
V_{EN} range	-0.3 V to V_{IN} + 0.3 V
V_{OUT} range	-0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Ratings Table
Junction temperature range, T_J	-40°C to 150°C
Storage temperature range, T_{stg}	-65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	AIR FLOW (CFM)	$R_{\theta JC}$(°C/W)	$R_{\theta JA}$(°C/W)	$T_A \leq 25°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	0	8.47	55.09	2.27 W	1.45 W	1.18 W
	150	8.21	49.97	2.50 W	1.60 W	1.30 W
	250	8.20	48.10	2.60 W	1.66 W	1.35 W



CONDITIONS	PACKAGE	PCB AREA	θJA
1	SOT223	4in² Top Side Only	53°C/W
2	SOT223	0.5in² Top Side Only	110°C/W

Figure 1. SOT223 Power Dissipation

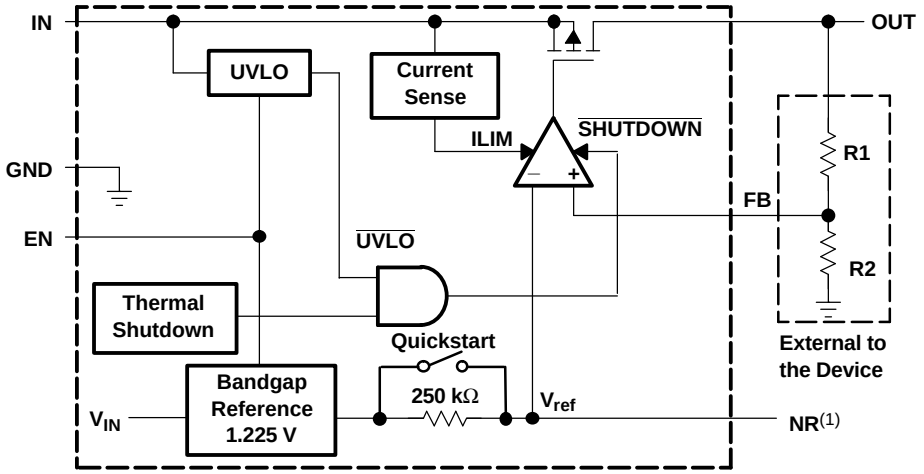
ELECTRICAL CHARACTERISTICS

Over recommended operating temperature range (T_J = -40°C to 125°C), $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)}$ + 1 V(1), I_{OUT} = 1mA, C_{OUT} = 10µF, C_{NR} = 0.01 µF, unless otherwise noted. Typical values are at 25°C.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)				2.7		5.5	V
I_{OUT}	Continuous output current				0		250	mA
V_{FB}	Internal reference	TPS79401	T_J = 25°C		1.220	1.225	1.230	V
V_{OUT}	Output voltage range	TPS79401			V_{FB}		5.5 - V_{DO}	V
	Accuracy(1)		V_{OUT} + 1 V ≤ V_{IN} ≤ 5.5 V	0 mA ≤ I_{OUT} ≤ 250 mA	-3.0		+3.0	%
	Output voltage line regulation ($\Delta V_{OUT}\%/\Delta V_{IN}$)(1)		V_{OUT} + 1 V < V_{IN} ≤ 5.5 V			0.05	0.12	%/V
	Load regulation ($\Delta V_{OUT}\%/\Delta I_{OUT}$)		0 µA < I_{OUT} < 250 mA			10		mV
	Dropout voltage(2) V_{IN} = $V_{OUT(nom)}$ - 0.1 V	TPS79428	I_{OUT} = 250 mA			155	210	mV
		TPS79430	I_{OUT} = 250 mA			155	210	
		TPS79433	I_{OUT} = 250 mA			145	200	
	Output current limit		V_{OUT} = 0 V			925		mA
	Ground pin current		0 µA < I_{OUT} < 250 mA			170	220	µA
	Shutdown current(3)		V_{EN} = 0 V	2.7 V < V_{IN} < 5.5 V		0.07	1	µA
	FB pin current		V_{FB} = 1.8 V				1	µA
	Power-supply ripple rejection	TPS79428	f = 100 Hz	I_{OUT} = 250 mA		65		dB
			f = 10 kHz	I_{OUT} = 250 mA		60		
			f = 100 kHz	I_{OUT} = 250 mA		40		
	Output noise voltage (TPS79428)		BW = 100 Hz to 100 kHz, I_{OUT} = 250 mA	C_{NR} = 0.001 µF		55		μV_{RMS}
				C_{NR} = 0.0047 µF		36		
				C_{NR} = 0.01 µF		33		
				C_{NR} = 0.1 µF		32		
	Time, start-up (TPS79428)		R_L - 14 Ω, C_{OUT} = 1 µF	C_{NR} = 0.001 µF		50		µs
				C_{NR} = 0.0047 µF		70		
				C_{NR} = 0.01 µF		100		
	High-level enable input voltage		2.7 V < V_{IN} < 5.5 V		1.7		V_{IN}	V
	Low-level enable input voltage		2.7 V < V_{IN} < 5.5 V		0		0.7	V
	EN pin current		V_{EN} = 0		1		1	µA
	UVLO threshold		V_{CC} rising		2.25		2.65	V
	UVLO hysteresis					100		mV

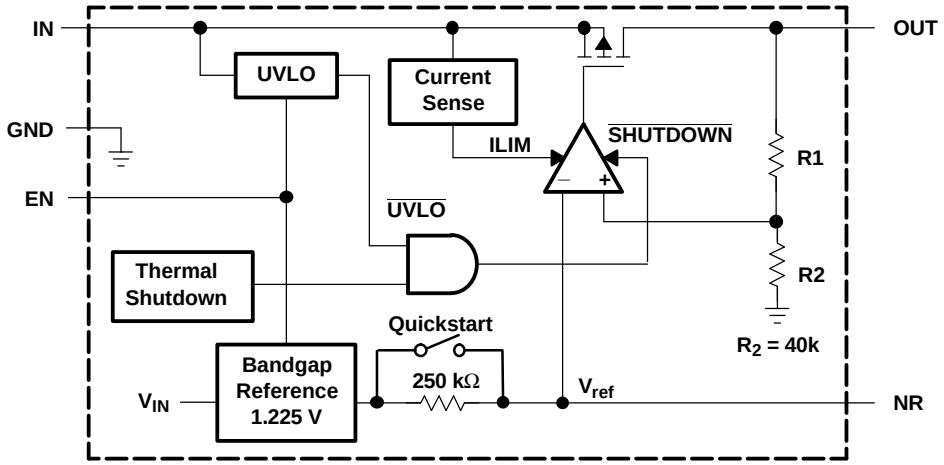
(1) Minimum V_{IN} is 2.7 V or V_{OUT} + V_{DO}, whichever is greater.
(2) Dropout is not measured for the TPS79418 and TPS79425 since minimum V_{IN} = 2.7 V.
(3) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



(1) Not Available on DCQ (SOT223) options.

FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			DESCRIPTION
NAME	DGN (MSOP)	DCQ (SOT223)	
NR	4	5	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This improves power-supply rejection and reduces output noise.
EN	6	1	The EN terminal is an input which enables or shuts down the device. When EN goes to a logic high, the device will be enabled. When the device goes to a logic low, the device is in shutdown mode.
FB	3	5	This terminal is the feedback input voltage for the adjustable device.
GND	5, PAD	3	Regulator ground.
IN	8	2	Unregulated input to the device.
NC	2, 7		No internal connection.
OUT	1	4	Output of the regulator.

TYPICAL CHARACTERISTICS

TPS79433 OUTPUT VOLTAGE vs OUTPUT CURRENT

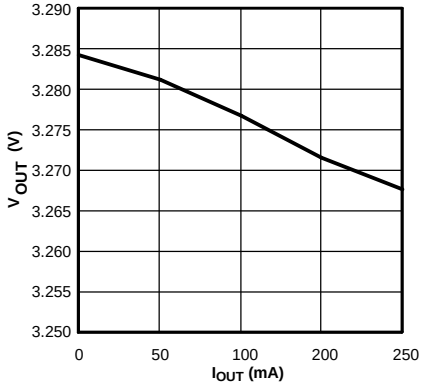


Figure 2.

TPS79428 OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

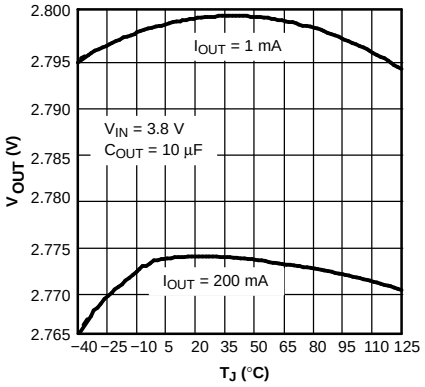


Figure 3.

TPS79428 GROUND CURRENT vs JUNCTION TEMPERATURE

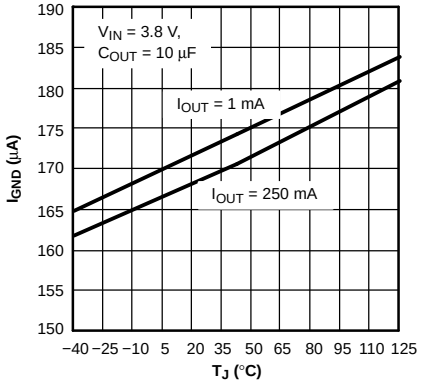


Figure 4.

TPS79428 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

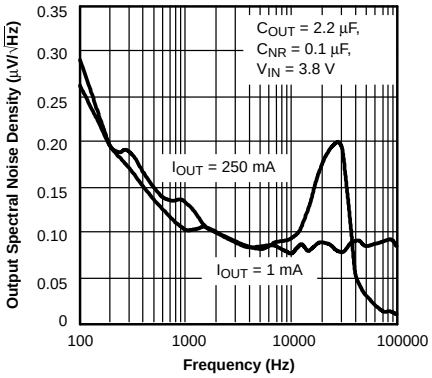


Figure 5.

TPS79428 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

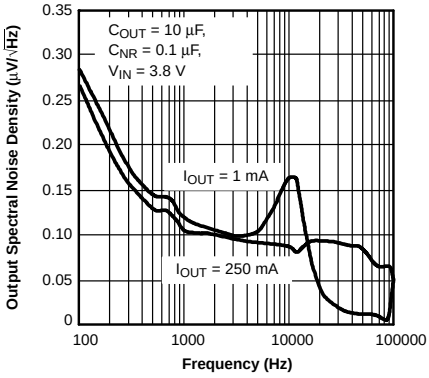


Figure 6.

TPS79428 OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

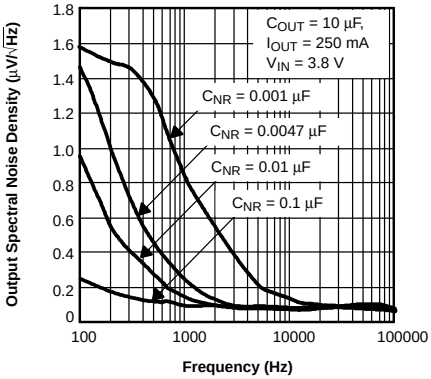


Figure 7.

TPS79428 ROOT MEAN SQUARED OUTPUT NOISE vs C_{NR}

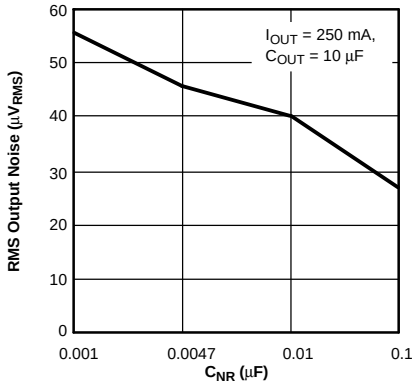


Figure 8.

TPS79433 OUTPUT IMPEDANCE vs FREQUENCY

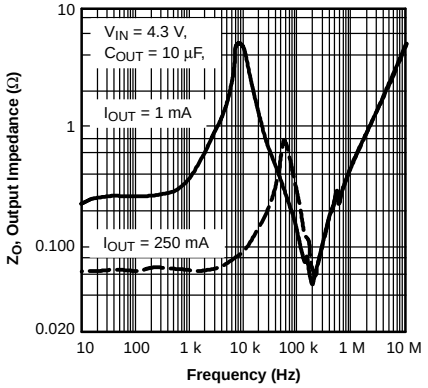


Figure 9.

TPS79428 DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

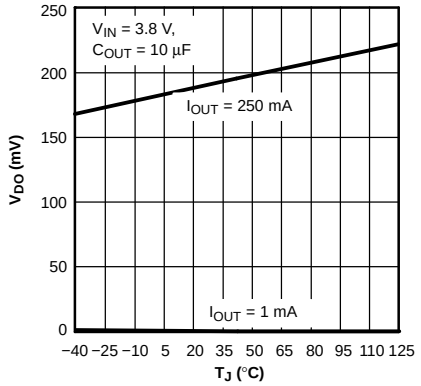


Figure 10.

TYPICAL CHARACTERISTICS (continued)

TPS79433 RIPPLE REJECTION vs FREQUENCY

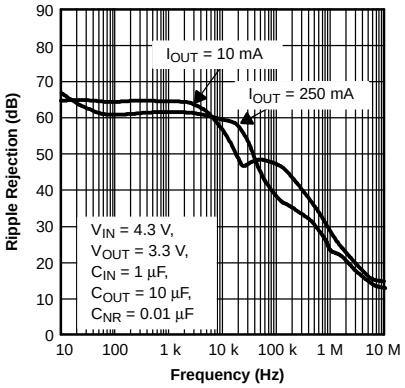


Figure 11.

TPS79433 RIPPLE REJECTION vs FREQUENCY

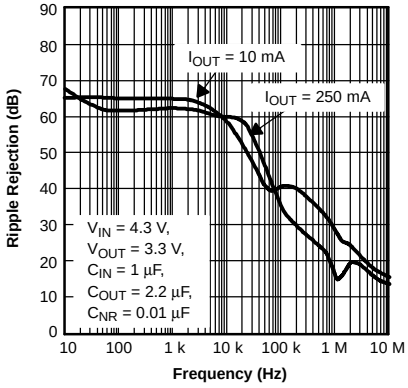


Figure 12.

TPS79433 RIPPLE REJECTION vs FREQUENCY

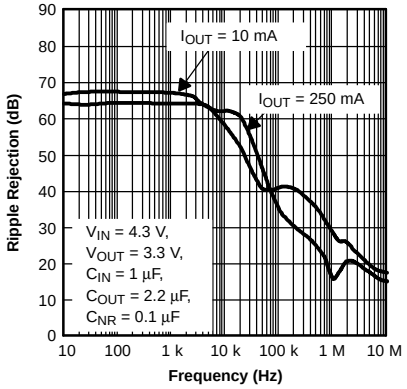


Figure 13.

TPS79433 OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)

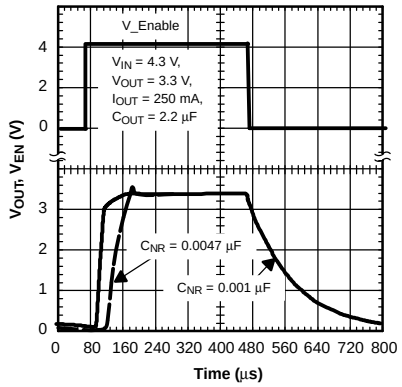


Figure 14.

TPS79433 LINE TRANSIENT RESPONSE

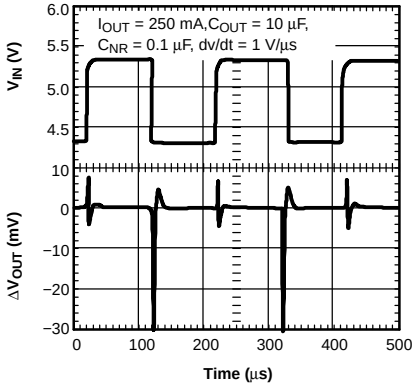


Figure 15.

TPS79433 LOAD TRANSIENT RESPONSE

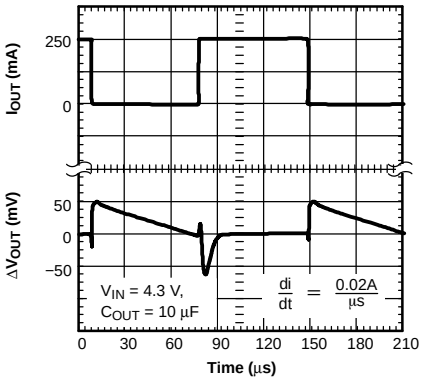


Figure 16.

TPS79425 POWER-UP/POWER-DOWN

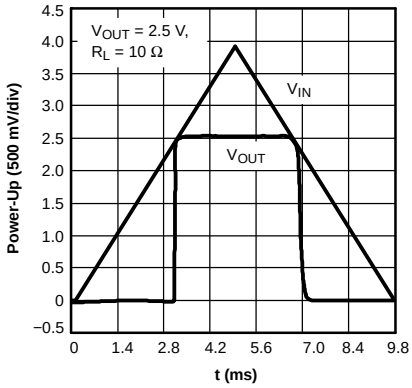


Figure 17.

TPS79433 DROPOUT VOLTAGE vs OUTPUT CURRENT

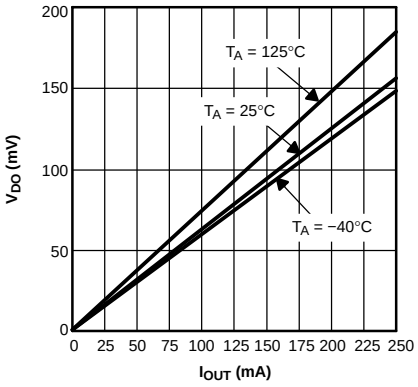


Figure 18.

TPS79401 DROPOUT VOLTAGE vs INPUT VOLTAGE

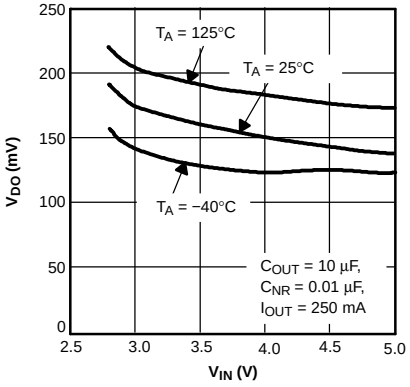


Figure 19.

TYPICAL CHARACTERISTICS (continued)

TPS79428 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

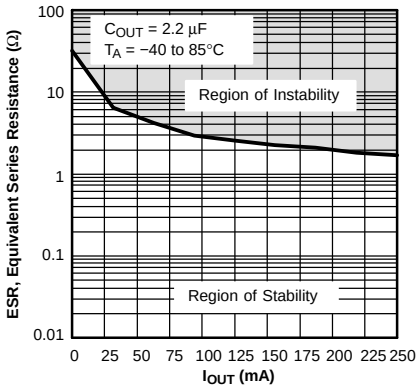


Figure 20.

TPS79428 TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT

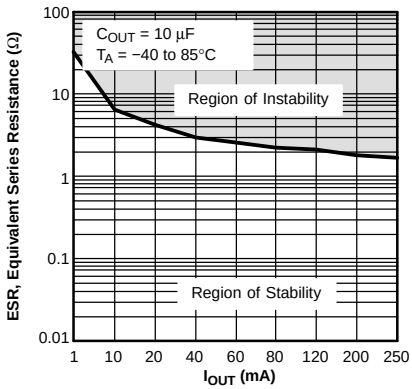


Figure 21.

APPLICATION INFORMATION

The TPS794xx family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current, and enable input to reduce supply currents to less than 1 µA when the regulator is turned off.

A typical application circuit is shown in Figure 22.

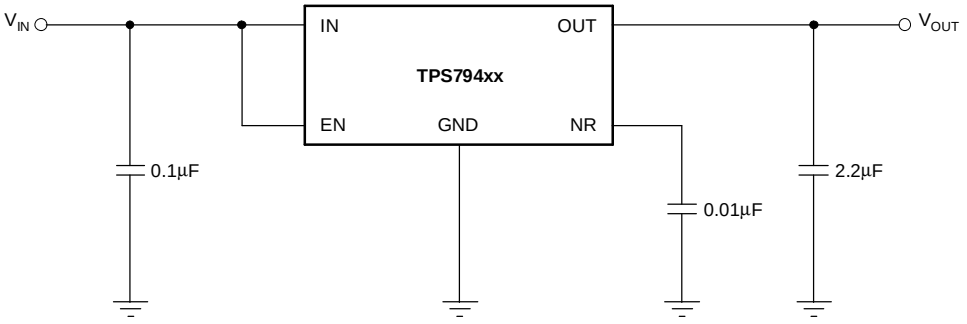


Figure 22. Typical Application Circuit

External Capacitor Requirements

A 0.1-µF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS794xx, is required for stability. It improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low dropout regulators, the TPS794xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 µF. Any 2.2 µF or larger ceramic capacitor is suitable.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS794xx has an NR pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the NR capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 µF to ensure that it is fully charged during the quickstart time provided by the internal switch shown in the functional block diagram.

For example, the TPS79428 exhibits only 32 μV_{RMS} of output voltage noise using a 0.1-µF ceramic NR capacitor and a 2.2-µF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250-kΩ resistor and external capacitor.

Board Layout Recommendation to Improve PSRR and Noise Performance

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

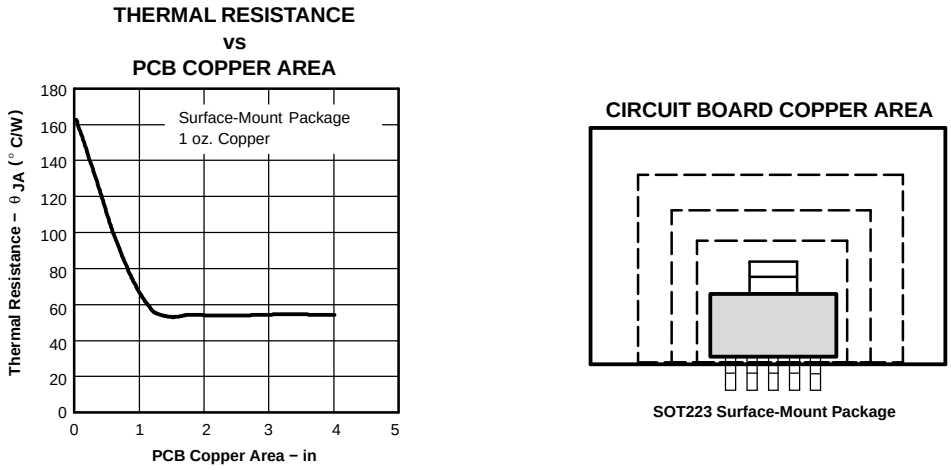


Figure 23. Thermal Resistance vs PCB Area for the SOT223-6.

Power and Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

where:

- $T_J$max is the maximum allowable junction temperature.
- $R\theta_{JA}$ is the thermal resistence juntion-to-ambient for the package. See the power dissipation table and Figure 1
- T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Regulator Mounting

The tab of the SOT223-6 package is electrically connected to ground. For best thermal performance, the tab of the surface-mount version should be soldered directly to a circuit-board copper area. Increasing the copper area improves heat dissipation. Solder pad footprint recommendations for the devices are presented in an application bulletin *Solder Pad Recommendations for Surface-Mount Devices*, literature number AB-132, available from the TI web site (www.ti.com).

Programming the TPS79401 Adjustable LDO Regulator

The output voltage of the TPS79401 adjustable regulator is programmed using an external resistor divider as shown in Figure 24. The output voltage is calculated using:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

where:

- V_{REF} = 1.2246 V typ (the internal reference voltage).

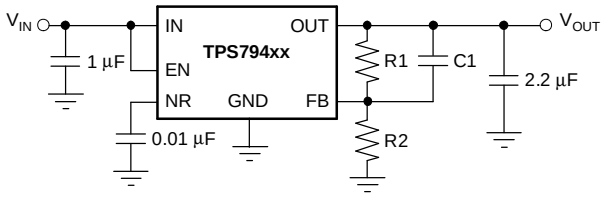
Resistors R1 and R2 should be chosen for approximately 40-µA divider current. Lower value resistors can be used for improved noise performance, but the device wastes more power. Higher values should be avoided as leakage current at FB increases the output voltage error. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 40 µA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages < 1.8 V, the value of this capacitor should be 100 pF. For voltages > 1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 µF instead of 2.2 µF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	49.9 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

† Not Available on the DCQ package.

Figure 24. TPS79401 Adjustable LDO Regulator Programming

Regulator Protection

The TPS794xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS794xx features internal current limiting and thermal protection. During normal operation, the TPS794xx limits output current to approximately 925 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage rating of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

TEXAS INSTRUMENTS

THERMAL PAD MECHANICAL DATA

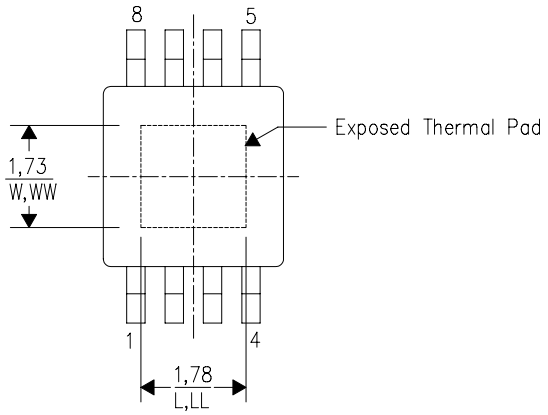
DGN (S–PDSO–G8)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. When the thermal pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

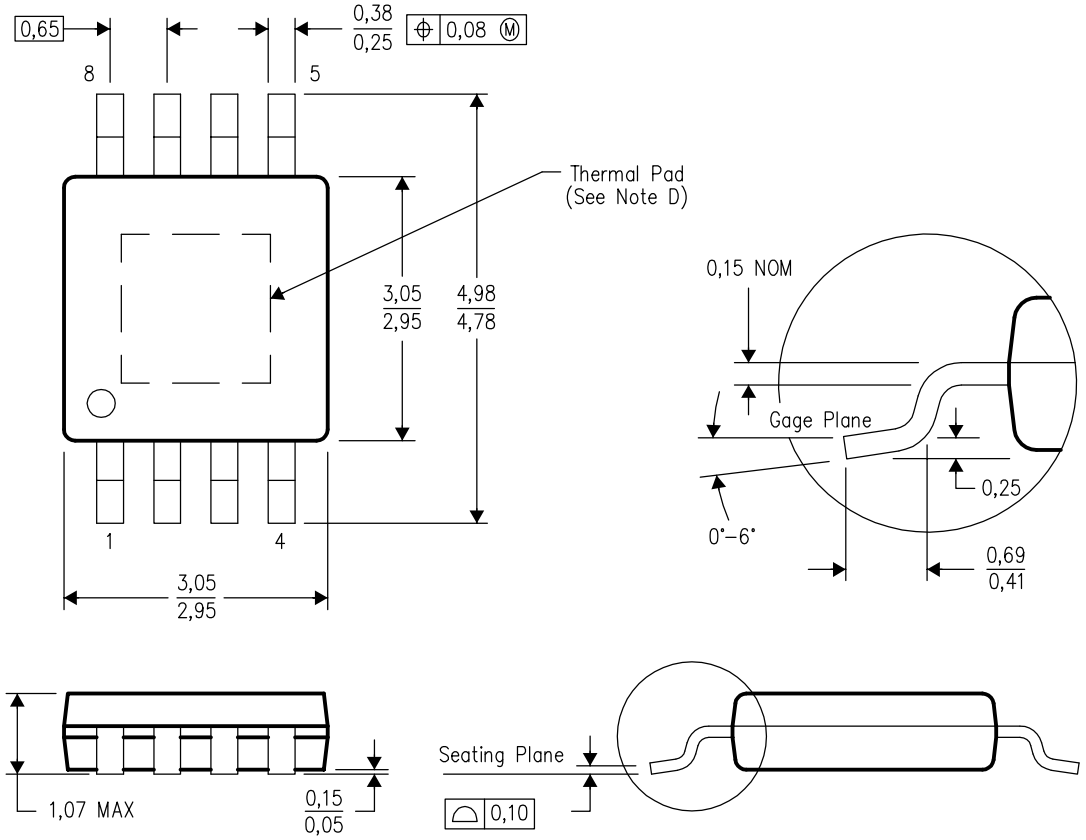
NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206323/– 12/04

SCALE		4206323		SHEET 2

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

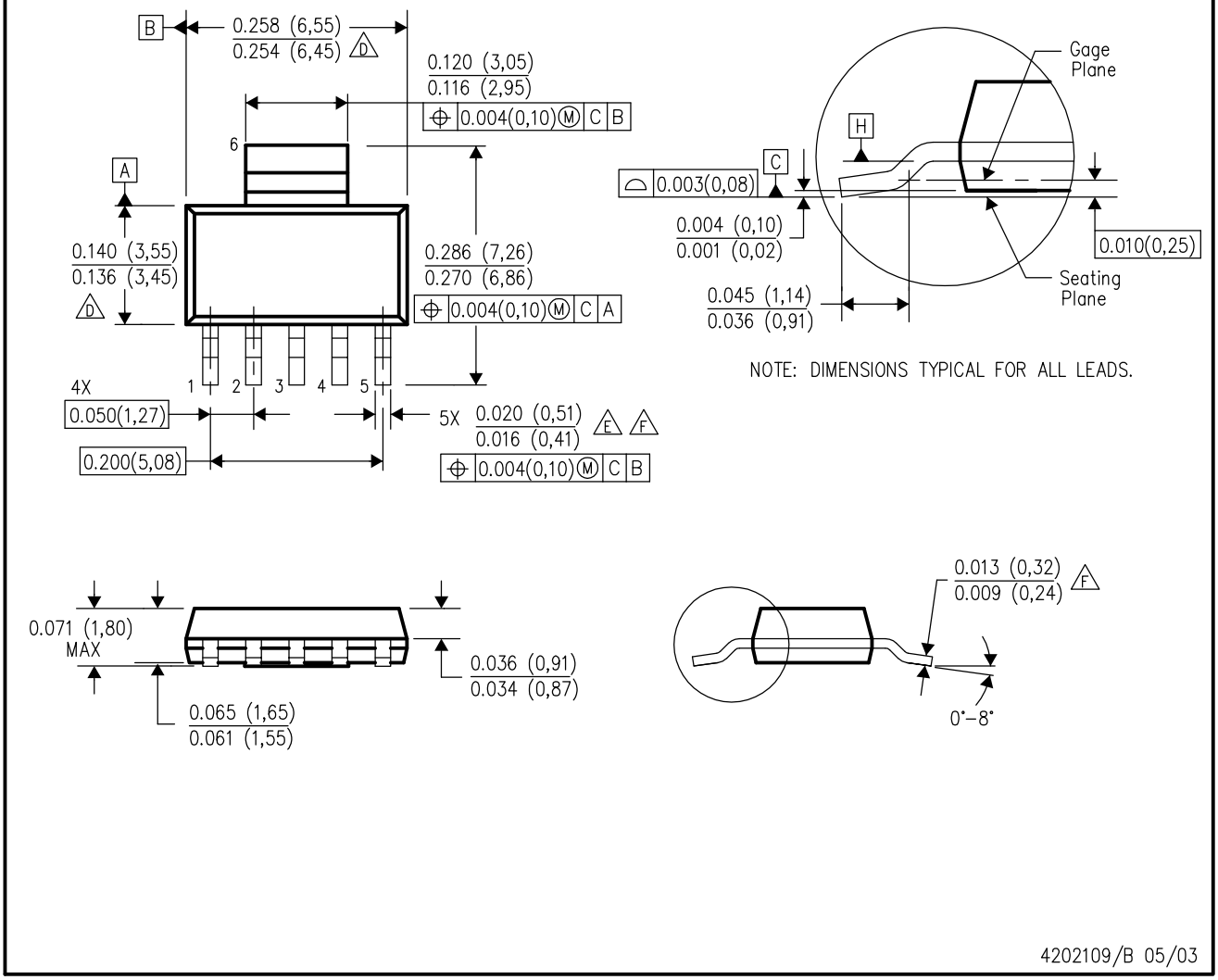


4073271/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

PowerPAD is a trademark of Texas Instruments.

DCQ (R–PDSO–G6) PLASTIC SMALL–OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Controlling dimension in inches.
- D. Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- E. Lead width dimension does not include dambar protrusion.
- F. Lead width and thickness dimensions apply to solder plated leads.
- G. Interlead flash allow 0.008 inch max.
- H. Gate burr/protrusion max. 0.006 inch.
- I. Datums A and B are to be determined at Datum H.
- J. Package dimensions per JEDEC outline drawing TO–261, issue B, dated Feb. 1999. This variation is not yet included.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265