FINAL

Am7996

IEEE 802.3/Ethernet/Cheapernet Transceiver

DISTINCTIVE CHARACTERISTICS

- **Compatible with Ethernet Version 2 and IEEE 802.3 10BASE-5 and 10BASE-2 specifications**
- **Pin-selectable SQE Test (heartbeat) option**
- **Internal jabber controller prevents excessive transmission time**
- **Noise rejection filter ensures that only valid data is transmitted onto the network**
- **Collision detection on both transmit and receive data**
- **Collision detect threshold levels adjustable for other networking applications**

GENERAL DESCRIPTION

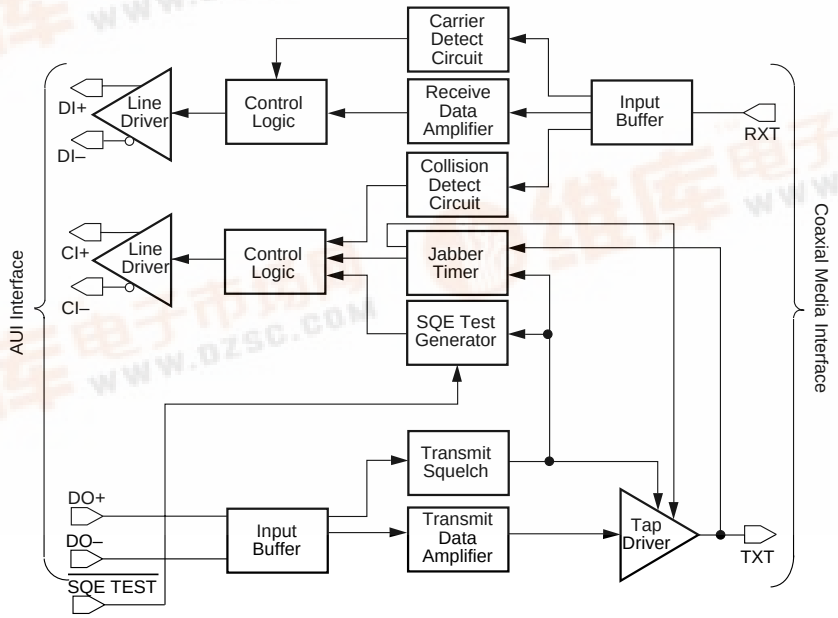
The Am7996 IEEE 802.3/Ethernet/Cheapernet Transceiver supports Ethernet Version 2, IEEE 802.3 10BASE-5 and IEEE 802.3 10BASE-2—Cheapernet) transceiver applications. Transmit, receive, and collision detect functions at the coaxial media interface to the data terminal equipment (DTE) are all performed by this single device.

In an IEEE 802.3 (10BASE-5)/Ethernet application, the Am7996 interfaces the coaxial (0.4″ diameter) media to the DTE through an isolating pulse transformer and the 78 Ω attachment unit interface (AUI) cable. In IEEE 802.3 10BASE-2—Cheapernet applications, the Am7996 typically resides inside the DTE with its signals to the DTE isolated and the coaxial (0.2″ diameter) media directly connected to the DTE. Transceiver power and ground in both applications are isolated from that of the DTE.

The Am7996's tap driver provides controlled skew and current drive for data signaling onto the media. The jabber controller prevents the node from transmitting excessively. While transmitting, collisions on the media are detected if one or more additional stations are transmitting.

The Am7996 features an optional SQE Test function that provides a signal on the CI pair at the end of every transmission. The SQE Test indicates the operational status of the CI pair to the DTE. It can also serve as an acknowledgment to the node that packet transmission onto the coax was completed.

BLOCK DIAGRAM



07506E-1

Publication# **07506** Rev: **E** Amendment/**0**
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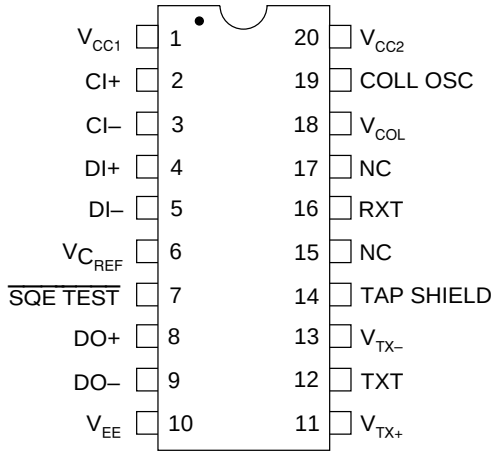
RELATED PRODUCTS

Part No.	Description
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am79C981	Integrated Multiport Repeater Plus™ (IMR+™)
Am79C987	Hardware Implemented Management Information Base™ (HIMIB™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C900	Integrated Local Area Communications Controller™ (ILACC™)
Am79C960	PCnet-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet-ISA+ Single-Chip Ethernet Controller (with Microsoft® Plug n' Play® Support)
Am79C965	PCnet-32 Single-Chip 32-Bit Ethernet Controller (for 386DX, 486 and VL buses)
Am79C970	PCnet-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C974	PCnet-SCSI Combination Ethernet and SCSI Controller for PCI Systems

CONNECTION DIAGRAMS

DIP



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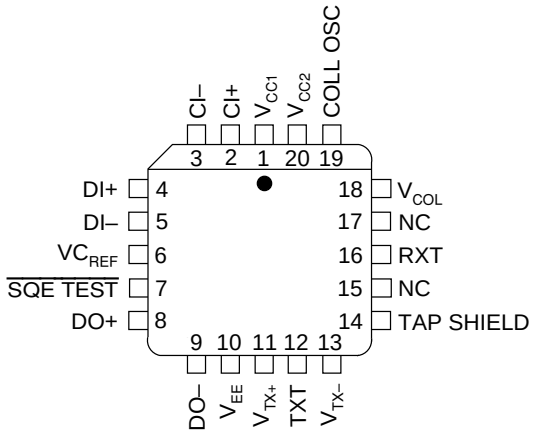
PLCC



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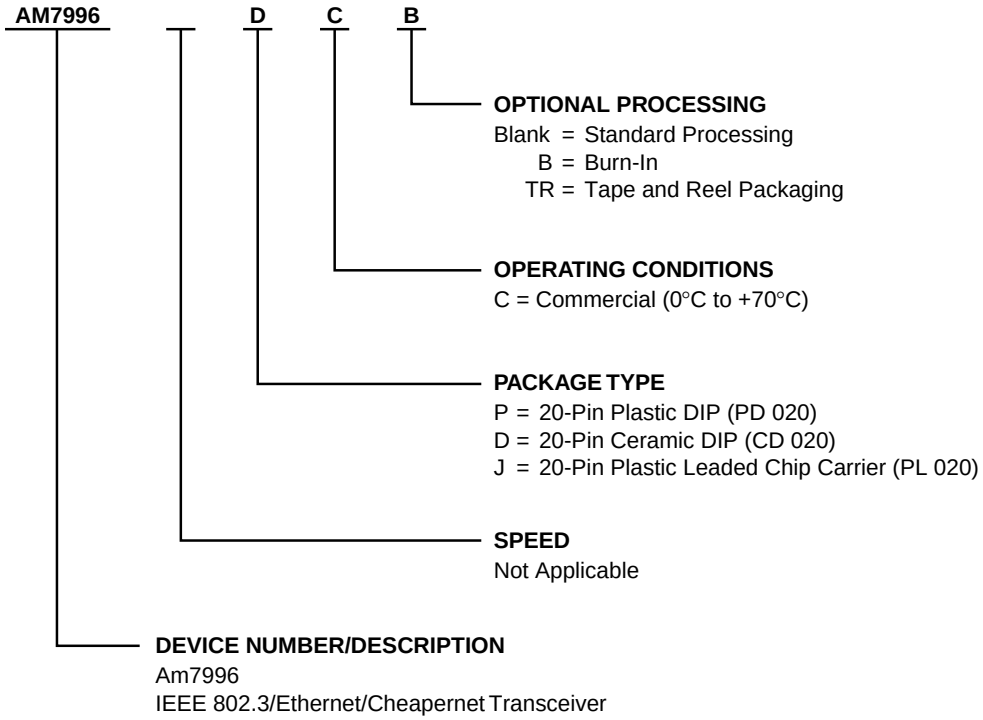
Notes:
Pin 1 is marked for orientation.
NC = No Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.



Valid Combinations	
AM7996	PC, PCB, DC, DCB, JC, JCTR

Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

Attachment Unit Interface (AUI)

DI+, DI–

Receive Line Output (Differential Outputs)

This pair is intended to operate into terminated 78 Ω transmission lines. Signals at RXT meeting bandwidth requirements and carrier sense levels are outputted at DI±. Signaling at DI± meets requirements of IEEE 802.3, Rev. D.

CI+, CI–

Collision Line Output (Differential Outputs)

This pair is intended to operate into terminated 78 Ω transmission lines. Signal Quality Error (SQE), detected at DO± inputs (excessive transmissions) or RXT input (during a collision), outputs the 10 MHz internal oscillator signal to the AUI interface. For proper component values at COLL OSC, signaling at CI± meets requirements of IEEE 802.3, Rev. D.

DO+, DO–

Transmit Input (Differential Inputs)

A pair of internally biased line receivers consisting of a squelch detect receiver with offset and noise filtering and a data receiver with zero offset for data signal processing. Signals meeting squelch requirements are waveshaped and output at TXT.

Coaxial Media Interface (TAP)

RXT

Media Signal Receiver Input (Input)

RXT connects to the media through a 4:1 attenuator of 100 kΩ total resistance (25 kΩ and 75 kΩ in series). Return for the attenuator is V_{COL}. RXT is an analog input with internal AC coupling for Manchester data signals and direct coupling for Carrier Detect and SQE average level detection. Signals at RXT meeting carrier squelch enable data to the DI± outputs. Data signals are AC coupled to DI± with a 150 ns time constant, high-pass filter. Signals meeting SQE levels enable COLL OSC frequency to CI± outputs.

TXT

Tap Node Driver (Input/Output)

A controlled bandwidth current source and sense amplifier. This I/O port is to be connected to the media through an isolation network and a low-pass filter. Signals meeting DO± squelch and jabber timing requirements are output at TXT as a controlled rise and fall time current pulse. When operated into a double terminated 50 Ω transmission line, signaling meets IEEE 802.3, Rev. D recommendations for amplitude, pulse-width distortion, rise and fall times, and harmonic content. The sense amplifier monitors TXT faults and inhibits transmission.

Global Signals

VC_{REF}

Timing Reference Set (Input)

VC_{REF} is a compensated voltage reference input with respect to V_{EE}. When a resistor is connected between VC_{REF} and V_{EE}, then internal transmit and receive squelch timing, SQE oscillator frequency, and receive and SQE output drive levels are set. SQE frequency set is also determined by components connected between V_{CC1} and COLL OSC.

$\overline{\text{SQE TEST}}$

Signal Quality Error Test Enable (Input)

The SQE Test function is enabled by connecting the $\overline{\text{SQE TEST}}$ pin to V_{EE} and disabled by connecting to V_{CC}.

V_{TX+}, V_{TX-}

Tap Node Driver Current Set (Inputs)

A reference input for transmission level and external redundant jabber. Transmit level is set by an external resistor between V_{TX+} and V_{TX-} (for an 80 mA peak level, R = 9.09 Ω). V_{TX-} may be operated between V_{EE} and V_{EE} + 1 V. When the voltage at V_{TX-} goes more positive than V_{EE} + 2 V, TXT is disabled and an SQE message is output at the CI pair.

TAP SHIELD

Low-Noise Media Cable Return (Input)

This input is the return for V_{COL} reference and the receive signal from the media. External connection is to a positive power supply.

V_{COL}

SQE Reference Voltage (Bias Supply)

SQE sense voltage and RXT input amplifier reference. An internally set analog reference for SQE level and data signal set at –1.600 V nominal with a source resistance of 150 Ω nominal. This reference should be filtered with respect to TAP SHIELD (see Applications section for adjusting threshold levels for other applications).

COLL OSC

SQE Timing Set (Input)

Timing input for SQE oscillator. For a properly set input at VC_{REF}, SQE oscillator period is set at 2.1RC. For a 10 MHz SQE oscillator frequency, R should be 1 kΩ and C 47 pF, including interconnect and device capacitance.

V_{CC1}

Positive Logic Supply

V_{CC2}

SQE Timing Reference (Positive Supply Voltage)

Timing reference return for SQE oscillator and analog signal ground.

V_{EE}

Negative Logic Supply and IC Substrate

FUNCTIONAL DESCRIPTION

The Am7996 IEEE 802.3/Ethernet/Cheapernet Transceiver consists of four sections: 1) Transmit—receives signals from DTE and sends it to the coaxial medium; 2) Receive—obtains data from media and sends it to DTE; 3) Collision Detect—indicates to DTE any collision on the media; and 4) Jabber—guards medium from node transmissions that are excessive in length.

Transmit

The Am7996 receives differential signals from the DTE (in the case of Am7990 family applications, from the Am7992—serial interface adapter—SIA). For IEEE (10BASE-5)/Ethernet applications, this signal is received through the AUI cable and isolation transformer. In IEEE 802.3 10BASE-2—Cheapernet applications, the AUI cable is optional.

Data is received through a noise rejection filter that rejects signals with pulse widths less than 7 ns (negative going), or with levels less than 175 mV peak. Only signals greater than –275 mV peak from the DTE are enabled. This minimizes false starts due to noise and ensures that no valid packets are missed.

The Am7996's tap driver provides the driving capability to ensure adequate signal level at the end of the maximum length network segment (500 meters) under the worst-case number of connections (100 nodes). Required rise and fall times of data transmitted on the network are maintained by the Am7996 Tap Driver. The tap driver's output is connected to the media through external isolating diodes. To safeguard network integrity, the driver is disabled whenever power falls below the minimum operation voltage.

During transmission, the Am7996 Jabber Controller monitors the duration that the transmit tap driver is active and disables the driver if the jabber time is exceeded. This prevents network tie-up due to a "babbling" transceiver. Once disabled, the driver is not reset until 400 ms after the DO pair is idle and there is no fault on TXT. During the disable time, an SQE signal is sent on the Cl pair to the DTE.

When $\overline{\text{SQE TEST}}$ is tied to V_{EE}, the Am7996 generates an SQE message at the end of every transmission. This signal is a self-test indication to the DTE that the media attachment unit (MAU) collision pair is operational.

Receive and Carrier Detect

Signal is acquired from the tap through a high-impedance (100 kΩ) resistive divider. A high input-impedance (low capacitance, high bandwidth, low noise) DC-coupled input amplifier in the Am7996 receives the signal. The received signal passes through a high-pass filter to minimize inter-symbol distortion, and then through a data slicer. The Am7996 Carrier Detect compares received signals to a reference. Signals meeting carrier squelch requirements enable data to the differential line driver within five bit times from the start of the packet.

Received data is transmitted from the Dl pair through an isolation transformer to the AUI cable (Ethernet/ IEEE 802.3—10BASE-5). In IEEE 802.3 10BASE-2—Cheapernet, the AUI cable is optional. Following the last transition of the packet, the Dl pair is held HIGH for two bit times and then decreases to idle level within twenty bit times.

Collision Detect

The Am7996 detects collisions on transmit if one or more additional stations are transmitting on the network.

Received signals are compared against the collision threshold reference. If the level is more negative than the reference, an enable signal is generated to the Cl pair. The collision threshold can be modified by external components.

The collision oscillator is a 10 MHz oscillator that drives the differential Cl pair to the DTE through an isolation transformer.

This signal is gated to the Cl pair whenever there is a collision, the SQE Test is in progress, or the jabber controller is activated. The oscillator is also utilized in counting time for the jabber timer and SQE Test.

The Cl± output meets the drive requirements for the AUI interface. The output stays HIGH for two bit times at the end of the packet, decreasing to the idle level within twenty bit times.

Jabber Function

The Am7996 Jabber Timer monitors the activity on the DO pair and senses TXT faults. It inhibits transmission if the tap driver is active for longer than the jabber time (26 ms). An SQE message (10 MHz collision signal), is enabled on the Cl pair for the fault duration.

After the fault is removed, the jabber timer counts the unjab time of 400 ms before it enables the driver.

If desired, a redundant jabber function can be implemented externally, and the output driver disabled by removing the driver supply at V_{TX-}.The Am7996 senses this condition and forces an SQE message on the Cl pair during the disable time.

SQE Test

An SQE Test will occur at the end of every transmission if the $\overline{\text{SQE TEST}}$ pin is tied to V_{EE}. The SQE Test signal is a gated 10 MHz signal to the Cl pair. The SQE Test ensures that the twisted-pair assigned for collision notification to the DTE is intact and operational. The SQE Test starts eight bit times after the last transition of the transmitted signal and lasts for a duration of eight bit times.

The SQE Test can be disabled by connecting the $\overline{\text{SQE TEST}}$ pin to V_{CC}.

APPLICATIONS

The Am7996 is compatible with Ethernet Version 2 and IEEE 802.3 10BASE5 and 10BASE2 applications. (See Figure 1).

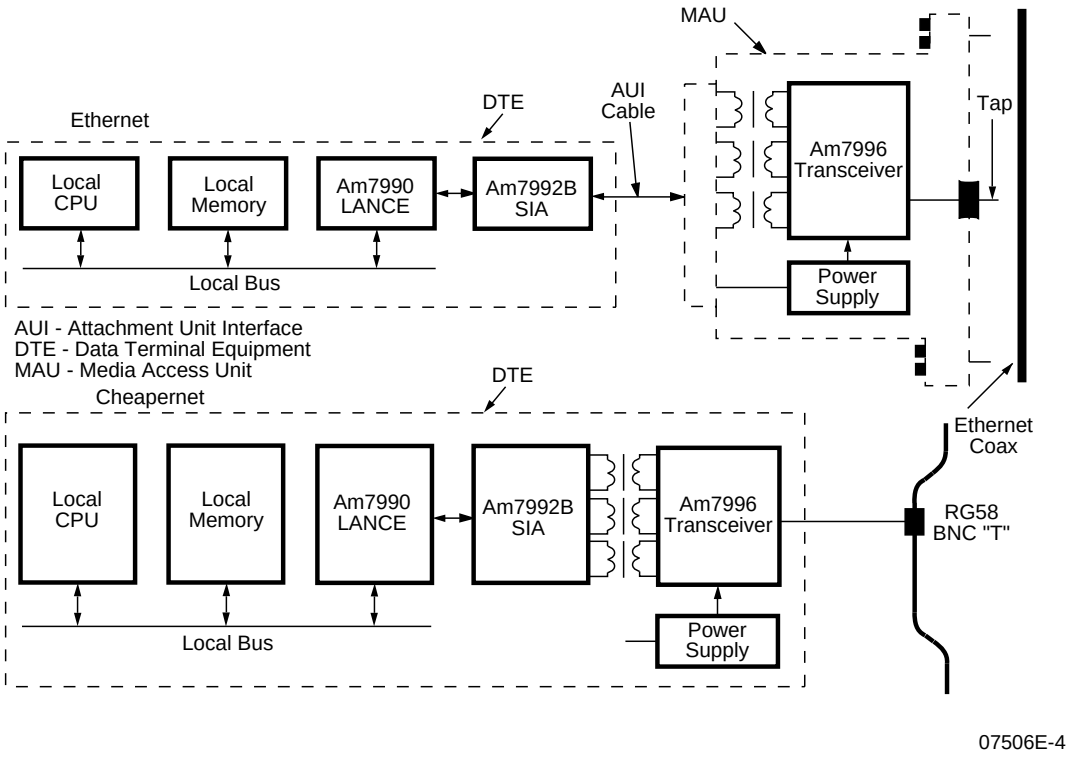


Figure 1. Typical Ethernet Node

Table 1. Transmit Mode Collision Detect Function Table

MAU Mode of Operation	Number of Transmitters		
	< 2	= 2	> 2
Transmitting	No	Yes	Yes
Not Transmitting	No	May	Yes

Table 2. IEEE 802.3 Recommended Transmit Mode Collision Detect Thresholds

IEEE 802.3	Threshold Voltage Level	
	No Detect	Must Detect
10BASE5, Ethernet	–1.492 V	–
10BASE2, Cheapernet	–1.404 V	–1.782 V

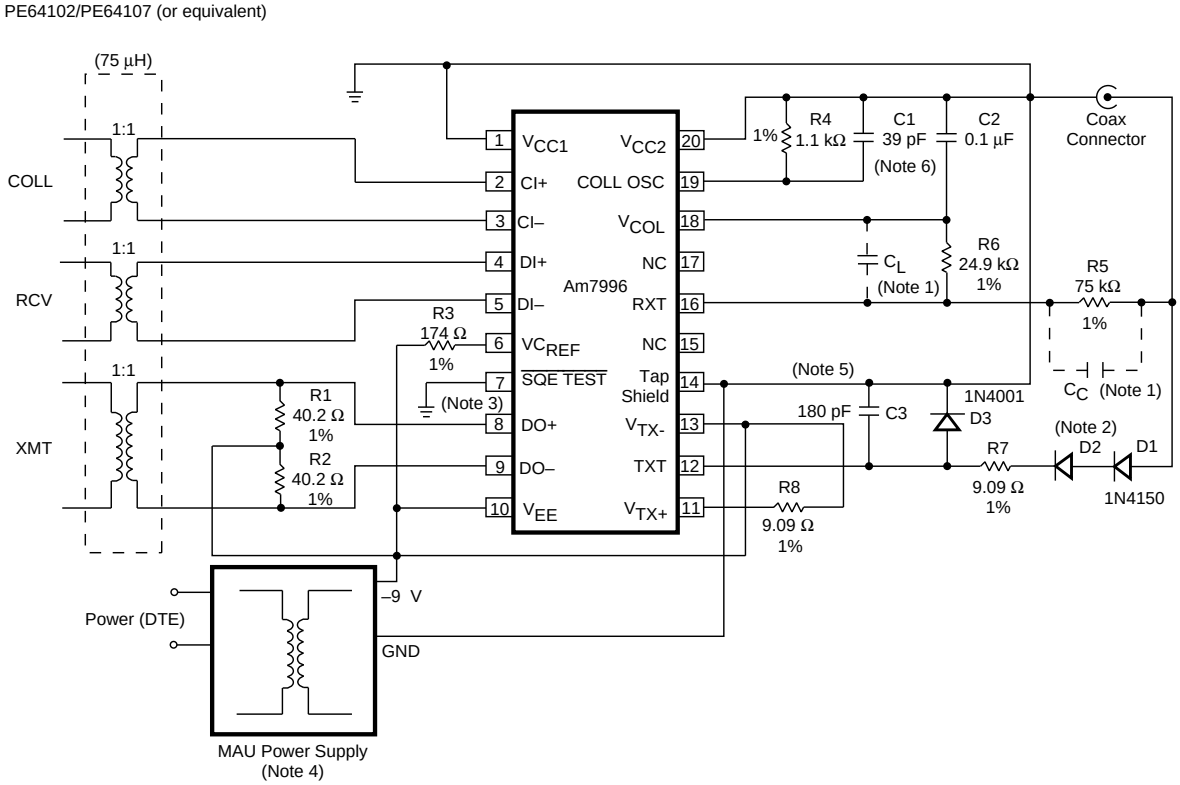
Table 3. Receive Mode Collision Detect Function Table

MAU Mode of Operation	Number of Transmitters		
	< 2	= 2	> 2
Transmitting	No	Yes	Yes
Not Transmitting	No	Yes	Yes

Table 4. IEEE 802.3 Recommended Receive Mode Collision Detect Thresholds

IEEE 802.3	Threshold Voltage Level	
	No Detect	Must Detect
10BASE5, Ethernet	–1.492 V	–1.629 V
10BASE2, Cheapernet	–1.404 V	–1.581 V

Figure 2 is an external component diagram showing how to implement the transmit mode collision detect levels recommended by IEEE 802.3. Figure 3 on the following page shows how to implement the receive mode collision detect levels recommended by IEEE 802.3. Receive mode collision detect threshold levels of the Am7996 are implemented by adding R9, R10 and C4. For the values of the components shown in Figure 3, a nominal receive mode collision detect threshold of –1.5 V, for a –1.404 V to –1.581 V window, is achieved.



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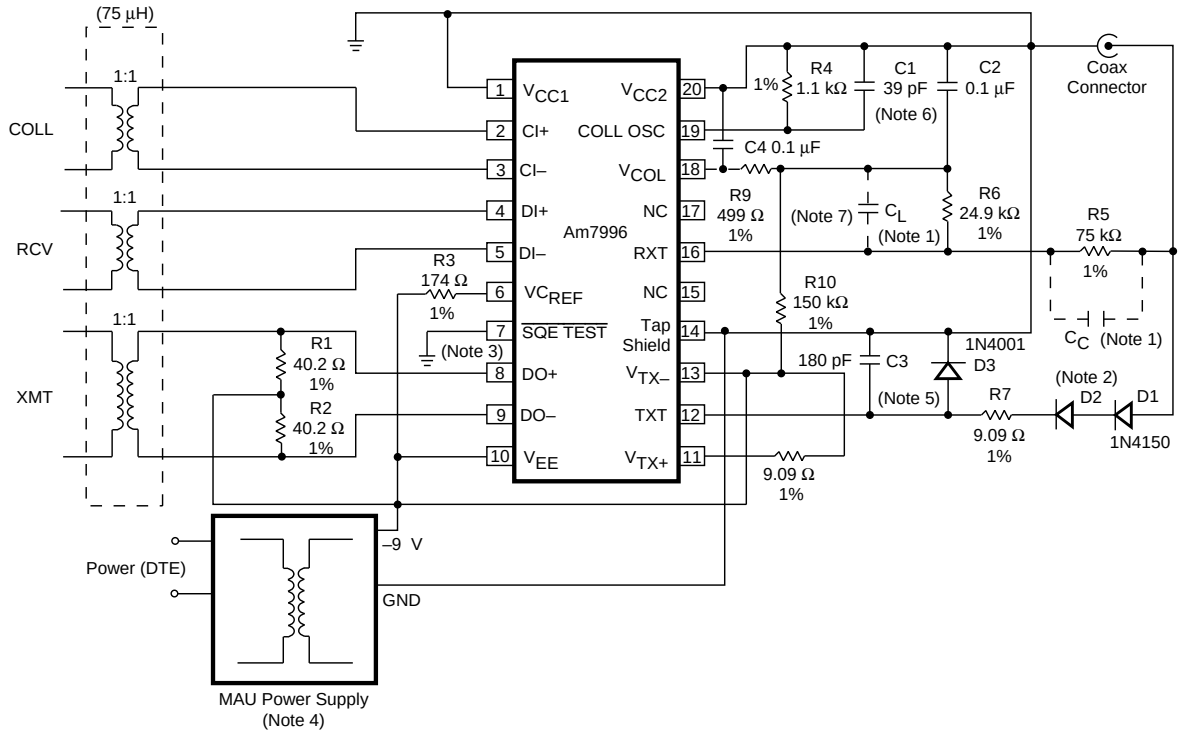
Notes:

1. *C_L is the effective load capacitance across R6; C_C is the compensation capacitance (C_C = 1/3 C_L).*
2. *D2 can be eliminated in Cheapernet (IEEE 802.3, 10BASE2) applications.*
3. *Shown with SQE Test disabled.*
4. *Discrete Power Supply or Hybrid-Hybrid DC-DC Converter Manufacturers include:*
   Ethernet (IEEE 802.3, 10BASE5)
   Reliability: 2E12R9
   Valor Electronics: PM1001
   Cheapernet (IEEE 802.3, 10BASE2)
   Reliability Inc: 2VP5U9
   Valor Electronics: PM7102
5. *The capacitance of C3, Am7996 package, D3 and the printed circuit board should add up to 180 pF ± 20%.*
6. *The capacitance of C1, Am7996 package and the printed circuit board should add up to 39 pF.*
7. *Figure 2 used for production testing of all parameters that are tested.*

Figure 2. Am7996 External Component Diagram for Transmit Mode Collision Detect



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Notes:

1. *C_L is the effective load capacitance across R6; C_C is the compensation capacitance (C_C = 1/3 C_L).*
2. *D2 can be eliminated in Cheapernet (IEEE 802.3, 10BASE2) applications.*
3. *Shown with SQE Test disabled.*
4. *Discrete Power Supply or Hybrid-Hybrid DC-DC Converter Manufacturers include:*
   Ethernet (IEEE 802.3, 10BASE5)
   Reliability: 2E12R9
   Valor Electronics: PM1001
   Cheapernet (IEEE 802.3, 10BASE2)
   Reliability Inc: 2VP5U9
   Valor Electronics: PM7102
5. *The capacitance of C3, Am7996 package, D3 and the printed circuit board should add up to 180 pF ± 20%.*
6. *The capacitance of C1, Am7996 package and the printed circuit board should add up to 39 pF.*
7. *R9, R10 and C4 are for Receive Mode Collision detection only.*

Figure 3. Am7996 External Component Diagram with Collision Threshold Modified for Receive Mode Collision Detect

LAYOUT CONSIDERATIONS

To protect the transceiver from the environment and to achieve optimum performance, the Am7996 is designed to be used with two sets of external components: the transmitter circuit consisting of components D1, D2, D3, R7, R8, and C3, and the receiver circuit consisting of components R5, R6, C_L, and C_C, (C_L is a parasitic capacitance rather than a discrete component). These two circuits are shown in both Figure 2 and in Figure 3 respectively. The resistor tolerances for these circuits are specified as 1% for temperature stability.

The only layout restriction for the transmitter circuit is that the longest current path from the TXT pin (Pin 12) to the coaxial cable's center conductor must be no longer than 4 inches.

The layout of the receiver circuit, however, is critical. To minimize parasitic capacitance that can degrade the received signal, the external receiver circuit should be isolated from power and ground planes. There must be no power or ground plane under the area of the PC board that includes pins 15 through 20, R5, R6, and the connector for the coaxial cable. If a power or ground plane extends under this area, the receiver will not function properly due to excessive crosstalk and under- or over-compensation of the R5, R6 attenuator. Also, the RXT pin (Pin 16) should be as close to the coaxial cable connector as possible.

Since there are no severe layout restrictions on the transmitter circuit, the layout can be simplified by omitting power and ground planes from the whole area on the right side of the Am7996 as shown in Figure 4-1.

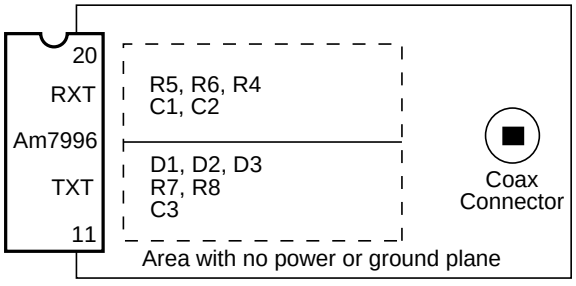

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Figure 4-1.

If the above layout rules are followed, the parasitic capacitance in parallel with R6 will be about 6 pF. This parasitic capacitance is shown in the schematics as C_L (Note that C_L is a parasitic capacitance. Do not add a discrete capacitor in parallel with R6). The capacitor labeled C_C in the schematics is the total capacitance in parallel with R5 including parasitic capacitance. The parasitic component of C_C will be about 1 pF. For optimum performance, the ratio of C_L to C_C should be the same as the ration of R5 to R6, which is 3 to 1. This means that an additional 1 pF of capacitance must be added in parallel with R5.

This additional capacitance can easily be added by building a parallel-plate capacitor for PC traces right under resistor R5. This capacitor can consist of a 0.200 in. by 0.200 in. square of conductor on each side of the board as shown in Figure 4-2 (These dimensions assume that the PC board is made from 0.060 in. thick G-10 material). The top plate of the capacitor should be connected to one lead of R5, and the bottom plate should be connected to the other lead. Figure 4-3 shows an example of this suggested layout for a four layer printed circuit board. Note that the component labeling used in Figure 4-3 is not intended to correspond with the component labeling used in Figure 2 and Figure 3.

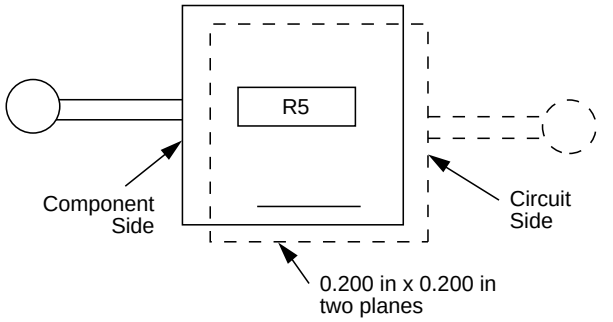

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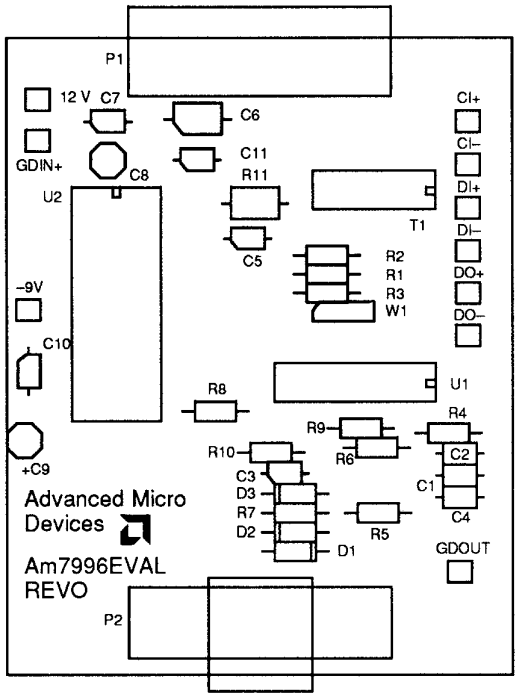
Figure 4-2.



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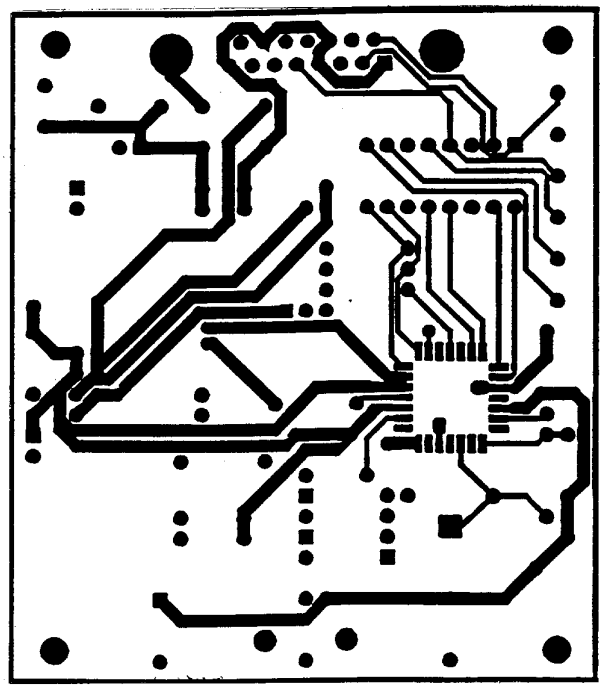
Component Side Silkscreen



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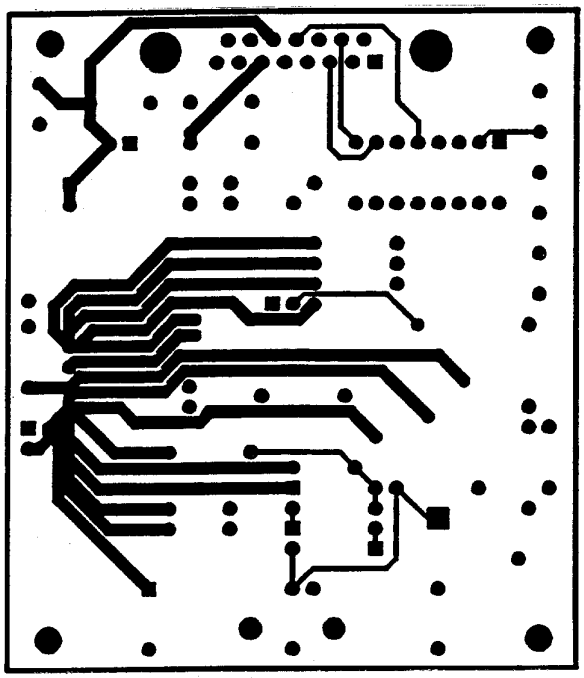
Component Side



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Solder Side

C11	CAP-0.01 µF
C2, C4, C7, C10	CAP-0.1 µF
C8	CAP-4.7 µF
C3	CAP-150 pF
C6	GAP CAP-0.001 µF
C1	CAP-39 pF
C5	CAP-1000 pF
D1, D2	DIODE 1N4153
D3	DIODE MUR120
P2	BNC
P1	15-Pin D Shell
R11	RES-1M
R4	RES-1.1K
R1	RES-40.2
R2	RES-40.2
R3	RES-174
R9	RES-499
R10	RES-150K
R6	RES-24.9K
R5	RES-75K with Trace Cap
R7	RES-9.09
R8	RES-9.09

Figure 4-3. Suggested Printed Circuit Board Layout for a Four Layer PCB Application

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C
Ambient Temperature
Under Bias . . . . . 0°C to +70°C
Supply Voltages (V_{EE}, V_{TX-}) . . . . . –12.0 V to +0.5 V
DC Input Voltage (D0+, D0–) . . . . –12.0 V to +0.5 V
DC Input Voltage (RXT) . . . . . –6 V to +0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . 0°C to +70°C
Supply Voltage (V_{EE}) . . . . . –8.1 V to –9.9 V

Operating ranges define those limits between which the functionality of the device is guaranteed

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions (Note 10)	Commercial Min	Commercial Typ	Commercial Max	Unit
Transmit Signals							
V_{TXTH}	Transmit Output HIGH Voltage (Note 1)		R_{LX} = 25 Ω	0	–0.05	–0.425	V
V_{TXTL}	Transmit Output LOW Voltage (Note 1)		R_{LX} = 25 Ω	–1.625	–2.0	–2.2	V
V_{TXT}	Transmit Average DC Voltage with 50% Duty-Cycle into DO+, DO– (Note 1)		R_{LX} = 25 Ω	–0.925	–1.0	–1.1	V
V_{ICM}	DO+, DO– Common Mode Bias Voltage		I_{IN} = 0	V_{EE} + 1.2	V_{EE} + 1.5	V_{EE} + 1.8	V
V_{IDC}	Differential Input Squelch Threshold (DO+, DO–) (Note 9)			–175	–225	–275	mV
I_{TXTL}	Transmit Current (Note 9)		V_{TXT} = –5.5 V	–65		–88	mA
I_{ILD}	Input Current (DO+, DO–)	V_{EE} = Max	V_{IN} = V_{EE} Max			–2.0	mA
I_{IHD}			V_{IN} = 0			2.5	
R_{IDF}	Differential Input Resistance (DO+, DO–)		V_{IN} = 0 to V_{EE}	6	8		kΩ
R_{ICM}	Common-Mode Input Resistance (DO+, DO–)		V_{IN} = 0 to V_{EE}	1.5	2		kΩ
Receive/Collision Signals							
V_{OD}	Differential Output Voltage (DI+, DI–; CI+, CI–)	R_L = 78 Ω	V_{OD+}	+550	+670	+850	mV
			$V_{OD–}$	–550	–670	–850	
V_{CMT}	Common-Mode Output (DI+, DI–; CI+, CI–)		R_L = 78 Ω	–1.0	–2.0	–3.0	V
V_{ODI}	Differential Output Voltage Imbalance (DI+, DI–; CI+, CI–) $\|\|V_{OD}\| - \|\overline{V}_{OD}\|\|$ (Note 6)		R_L = 78 Ω		5	20	mV
V_{OD} OFF	Differential Output Idle Voltage (DI+, DI–; CI+, CI–)		R_L = 78 Ω, V_{EE} = Max	–20	0	+20	mV
V_{CAT}	Carrier Sense Threshold		V_{IN} = 5 MHz Preamble	–400	–500	–600	mV
V_{COT}	Collision Sense Threshold (Note 5)			–1515	–1600	–1700	mV
I_{RXT}	RXT Input Bias Current		V_{IN} = 1 V to –2.5 V; V_{EE} = Max	–0.5	0	+0.5	µA
I_{OD} OFF	Differential Output Idle Current (DI+, DI–; CI+, CI–)		R_L = 0	–0.5	0	+0.5	mA
Global							
I_{EE}	Supply Current–Non-Transmitting		R_{LX} = 25 Ω (Note 4)		–88	–105	mA
	Supply Current–Transmitting				–128	–155	

CAPACITANCE* (T_A = 25°C; V_{EE} = 0; Pins 15, 17—No Connections)

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
C_{RXT}	RXT Input Capacitance	Ceramic DIP		1.7		pF
		Plastic DIP/PLCC		1.1		

Notes:

See notes following Switching Characteristics section.

**Parameters are not "Tested."*

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

No	Parameter Symbol	Parameter Description	Test Conditions	Commercial			Unit
				Min	Typ	Max	
Receiver Specification							
1	t_{PWREJ}	DO± Input Pulse Width to Reject ($DO± \geq V_{IDC}$, Max)	(Note 1)		15	7	ns
2	t_{PWTON}	DO± Input Pulse Width to Turn On ($DO± > V_{IDC}$, Max)	(Note 1)	20	15		ns
3	t_{PWSON}	DO± Input Pulse Width to Stay On ($DO± \geq V_{IDC}$, Max)	(Note 1)			105	ns
4	t_{PWOFF}	DO± Input Pulse Width to Turn Off ($DO± \geq V_{IDC}$, Max)	(Note 1)	160			ns
5	t_{TON}	Transmit Driver Turn-On Delay	(Note 1)			200	ns
7	t_{TSD}	Transmit Static Delay (Zero Crossing to 50% Point to Coax)	(Note 1)		30	50	ns
8	t_{TXTR}	Transmit Driver Rise Time	(Notes 1, 7)	20	25	30	ns
9	t_{TXTF}	Transmit Driver Fall Time	(Notes 1, 7)	20	25	30	ns
10	t_{DRF}	Difference in Driver Rise and Fall Times $\lvert t_{TXTR} - t_{TXTF} \rvert$	(Notes 1, 7)			1.0	ns
11	t_{SKEW}	Output Driver Skew—Transmit Data Symmetry	(Note 1)	–2.0		+2.0	ns
12	t_{JCT}	Jabber Control Time	(Note 1)	20	26	35	ms
13	t_{JRT}	Jabber Reset Time	(Note 1)	340	419	500	ms
14	t_{JREC}	Jabber Recovery Time	(Note 1)			1.0	µs
Receive/Collision Specification							
15	t_{RON}	Receiver Turn-On Delay	$V_{tap} > V_{CAT}$ Max		250	500	ns
16	t_{ROFF}	Receiver Turn-Off Delay	$V_{tap} < V_{CAT}$ Min			1000	ns
17	t_{RSD}	Receiver Static Delay	50% Point at RXT at Zero Crossing at DI± Outputs			50	ns
18	t_{RS}	Receive Data Symmetry		–2		+2	%
19	t_{RR}	DI± and CI± Rise Time	20%–80%, $R_L = 78\ \Omega$			7	ns
20	t_{RF}	DI± and CI± Fall Time	80%–20%, $R_L = 78\ \Omega$			7	ns
21	t_{CON}	CI± Turn-On Delay	$V_{tap} > V_{COT}$ Max			900	ns
22	t_{COFF}	CI± Turn-Off Delay	$V_{tap} < V_{COT}$ Min			2000	ns
23	t_{CL}	CI± LOW Time		35	50	70.5	ns
24	t_{CH}	CI± HIGH Time		35	50	70.5	ns
25	f_{CI}	Collision Frequency	(Note 8)	8.5	10.0	11.5	MHz
26	t_{STD}	SQE Test Delay Time	$F_{CI} = 10.0$ MHz	600		1000	ns
27	t_{STL}	SQE Test Length	$F_{CI} = 10.0$ MHz	600	800	1000	ns

Notes:

1. *Parameters are measured at coax tap. In production test, parameters are measured across at 25 Ω load equivalent to the coax tap.*
2. *For conditions shown as Min or Max, use the appropriate value specified under Operating Range for the applicable device type.*
3. *Typical values are at V_{EE} = –9.0 V, 25°C ambient.*
4. *V_{TX-} wired to V_{EE}.*
5. *This threshold can be modified externally (see Figure 3).*
6. *Parameter not tested.*
7. *Tested on a 5 Mbps preamble (continuous 1010 pattern) measured between 20% and 80% points, test limits correlated to 10% and 90% data sheet limits shown.*
8. *Determined by Am7966 External Component Diagrams values for R4 and C1.*
9. *In production test, input signal applied thru transformer to DO± inputs.*
10. *Figure 2 used for production testing of all parameters.*

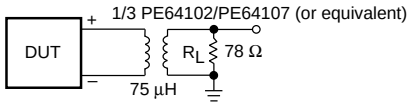
**Notes listed correspond to the respective references made in DC Characteristics and Switching Characteristics tables.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

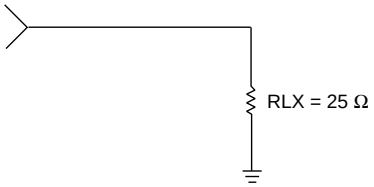
KS000010

SWITCHING TEST CIRCUIT



07506E-12

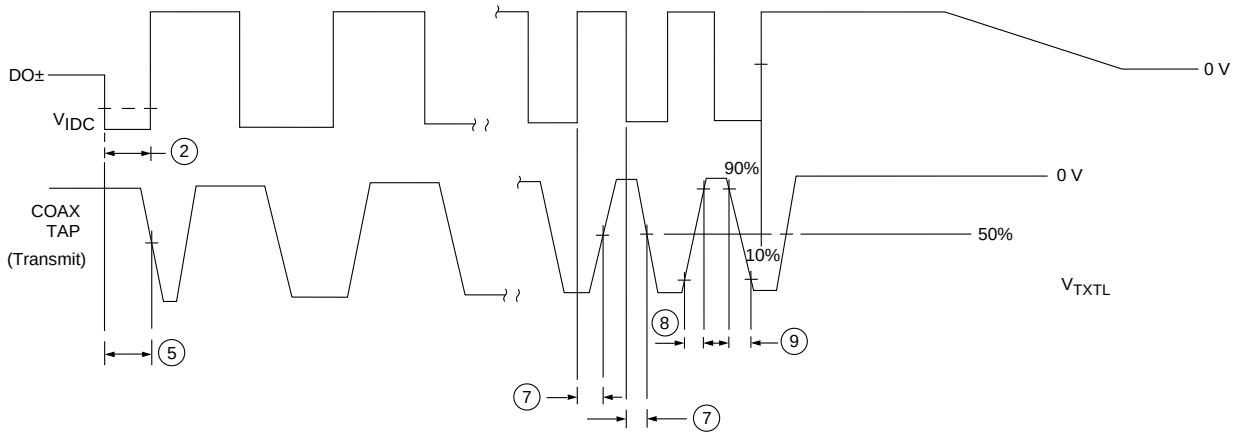
A. AUI Transmit (DI+, DI–,; CI+, CI–)



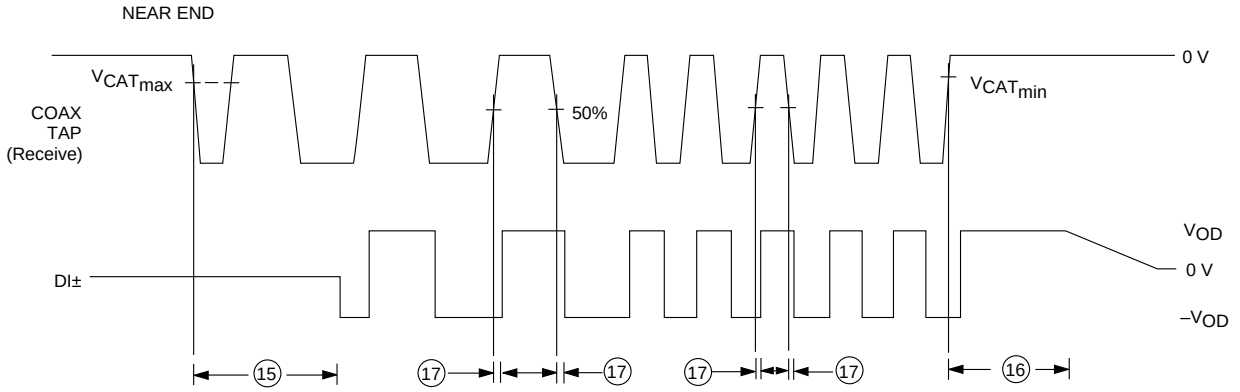
07506E-13

B. Test Load (TXT)

SWITCHING WAVEFORMS

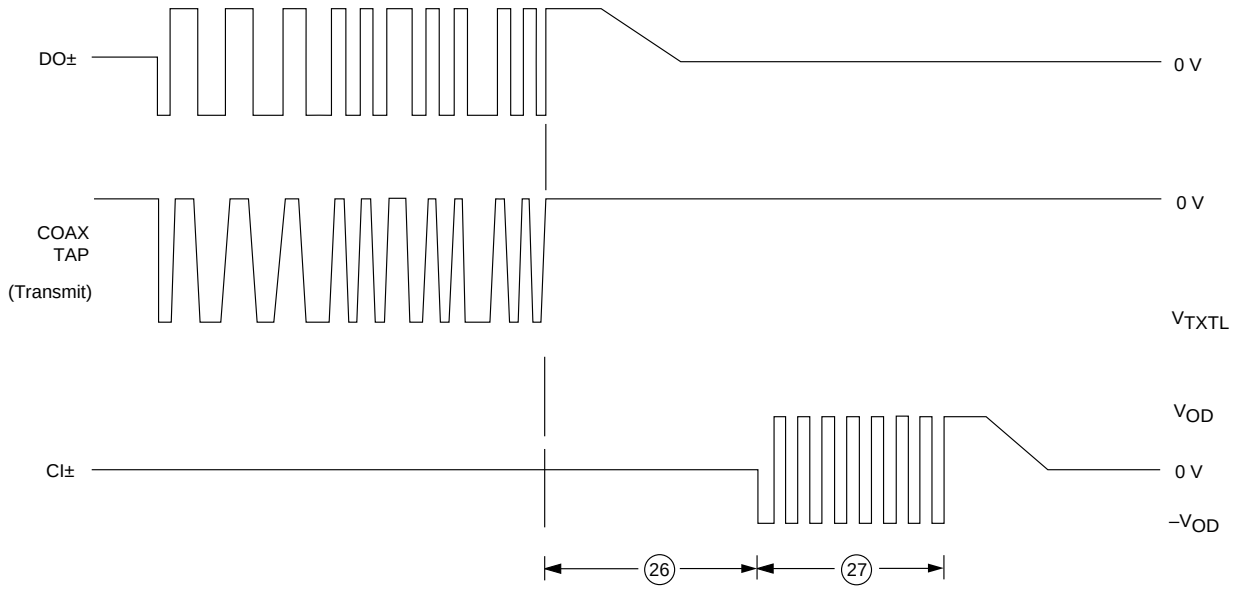


Transmit Function



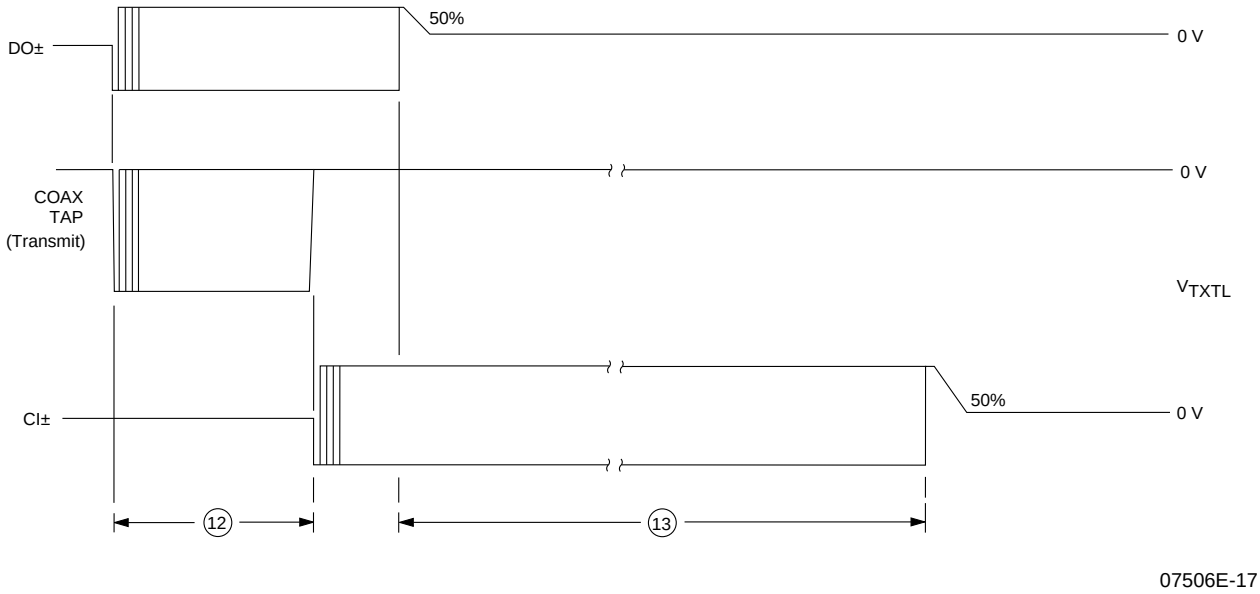
Receiver Function

SWITCHING WAVEFORMS



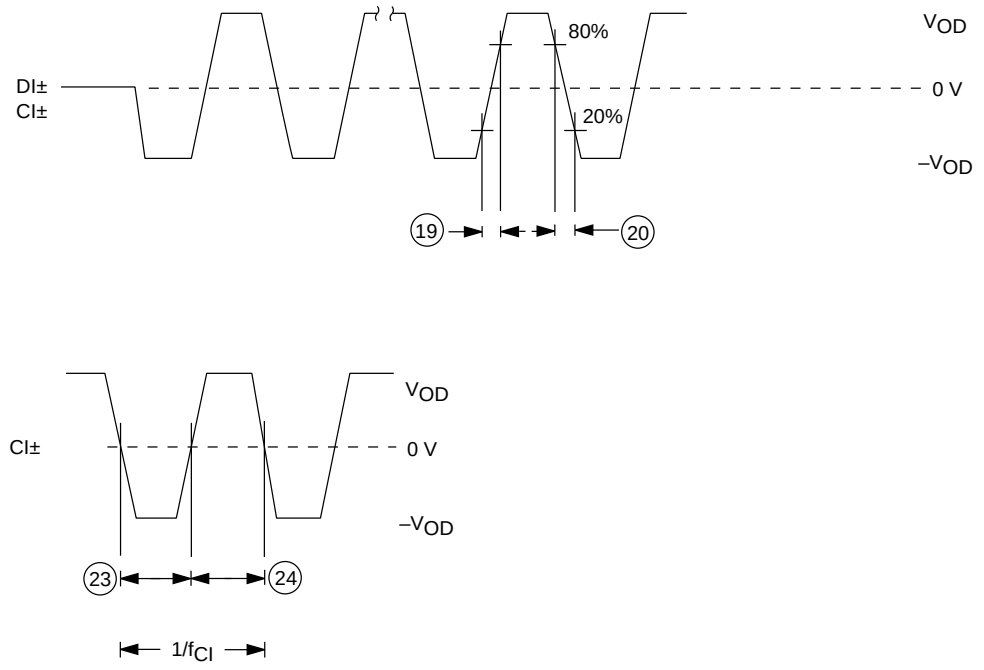
SQE Test*

*$\overline{\text{SQE TEST}}$ *pin connected to* V_{EE}



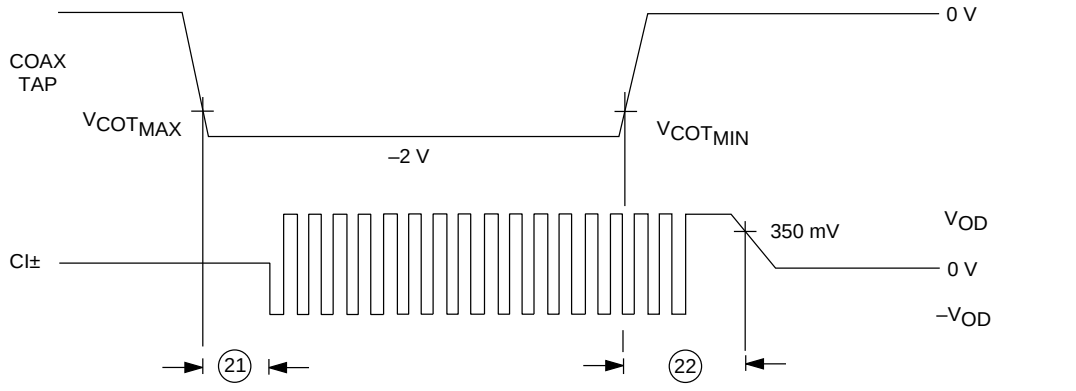
Jabber Function

SWITCHING WAVEFORMS



07506E-18

DI±/CI± Parameters



07506E-19

Collision Detect Timing

Note:

This signal is used for test purposes. It represents the average value of the signal that might be seen on the coax tap when a collision occurs.