

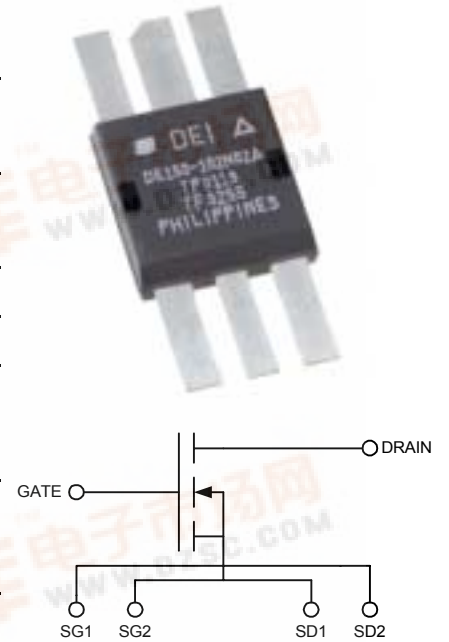
N-Channel Enhancement Mode  
Avalanche Rated  
Low  $Q_g$  and  $R_g$   
High  $dv/dt$   
Nanosecond Switching

Preliminary Data Sheet

$V_{DSS} = 1000\text{ V}$   
 $I_{D25} = 1.5\text{ A}$   
 $R_{DS(on)} = 11\ \Omega$   
 $P_{DHS} = 80\text{ W}$

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	1000	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ ; $R_{GS} = 1\text{ M}\Omega$	1000	V
$V_{GS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_c = 25^\circ\text{C}$	1.5	A
$I_{DM}$	$T_c = 25^\circ\text{C}$ , pulse width limited by $T_{JM}$	9	A
$I_{AR}$	$T_c = 25^\circ\text{C}$	1.5	A
$E_{AR}$	$T_c = 25^\circ\text{C}$	6	mJ
$dv/dt$	$I_S \leq I_{DM}$ , $di/dt \leq 100\text{ A}/\mu\text{s}$ , $V_{DD} \leq V_{DSS}$ , $T_J \leq 150^\circ\text{C}$ , $R_G = 0.2\ \Omega$	3	V/ns
	$I_S = 0$	>200	V/ns
$P_{DHS}$	$T_c = 25^\circ\text{C}$ Derate $4.4\text{ W}/^\circ\text{C}$ above $25^\circ\text{C}$	80	W
$P_{DAMB}$	$T_c = 25^\circ\text{C}$	3.5	W
$T_J$		-55...+150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55...+150	$^\circ\text{C}$
$T_L$	1.6mm (0.063 in) from case for 10 s	300	$^\circ\text{C}$
<b>Weight</b>		2	g

Symbol	Test Conditions	Characteristic Values		
		$T_J = 25^\circ\text{C}$ unless otherwise specified		
		min.	typ.	max.
$V_{DSS}$	$V_{GS} = 0\text{ V}$ , $I_D = 3\text{ ma}$	1000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 4\text{ ma}$	2.5		V
$I_{GSS}$	$V_{GS} = \pm 20\text{ V}_{DC}$ , $V_{DS} = 0$			$\pm 100\text{ nA}$
$I_{DSS}$	$V_{DS} = 0.8\text{ V}_{DSS}$ , $T_J = 25^\circ\text{C}$ $V_{GS} = 0$ , $T_J = 125^\circ\text{C}$			50 $\mu\text{A}$
				500 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 15\text{ V}$ , $I_D = 0.5I_{D25}$ Pulse test, $t \leq 300\ \mu\text{s}$ , duty cycle $d \leq 2\%$			11 $\Omega$
$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 0.5I_{D25}$ , pulse test	0.8	1.5	S



**Features**

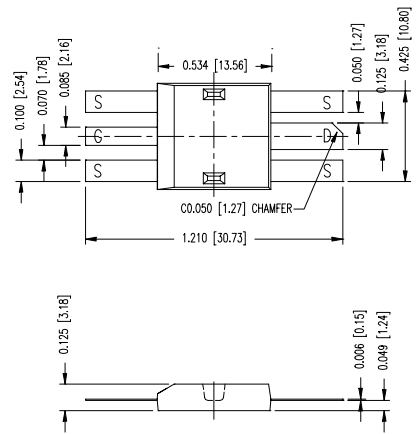
- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced low  $Q_g$  process
- Low gate charge and capacitances
  - easier to drive
  - faster switching
- Low  $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

**Advantages**

- Optimized for RF and high speed switching at frequencies to >100MHz
- Easy to mount—no insulators needed
- High power density



Symbol	Test Conditions	Characteristic Values		
		(T <sub>J</sub> = 25°C unless otherwise specified)		
		min.	typ.	max.
R <sub>G</sub>				5 Ω
C <sub>iSS</sub>			500	pF
C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0.8 V <sub>DSS(max)</sub> , f = 1 MHz		20	pF
C <sub>rSS</sub>			3	pF
T <sub>d(on)</sub>			4	ns
T <sub>on</sub>	V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0.8 V <sub>DSS</sub> I <sub>D</sub> = 0.5 I <sub>DM</sub>		4	ns
T <sub>d(off)</sub>	R <sub>G</sub> = 0.2 Ω (External)		4	ns
T <sub>off</sub>			4	ns
Q <sub>g(on)</sub>			23	nC
Q <sub>gs</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 0.5 V <sub>DSS</sub> I <sub>D</sub> = 0.5 I <sub>D25</sub>		4.5	nC
Q <sub>gd</sub>			14	nC
R <sub>thJHS</sub>			1.5	K/W



Symbol	Test Conditions	Characteristic Values		
		(T <sub>J</sub> = 25°C unless otherwise specified)		
		min.	typ.	max.
I <sub>S</sub>	V <sub>GS</sub> = 0 V			1.5 A
I <sub>SM</sub>	Repetitive; pulse width limited by T <sub>JM</sub>			9 A
V <sub>SD</sub>	I <sub>F</sub> = I <sub>S</sub> , V <sub>GS</sub> = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.8 V
T <sub>rr</sub>			710	ns

Directed Energy, Inc. reserves the right to change limits, test conditions and dimensions.  
DEI MOSFETS are covered by one or more of the following U.S. patents:

4,835,592	4,850,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				

**102N02A DE-SERIES SPICE Model**

The DE-SERIES SPICE Model is illustrated in Figure 1. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms  $L_G$ ,  $L_S$  and  $L_D$ .  $R_d$  is the  $R_{DS(ON)}$  of the device,  $R_{ds}$  is the resistive leakage term. The output capacitance,  $C_{OSS}$ , and reverse transfer capacitance,  $C_{RSS}$  are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via  $R_{on}$  and  $R_{off}$ .

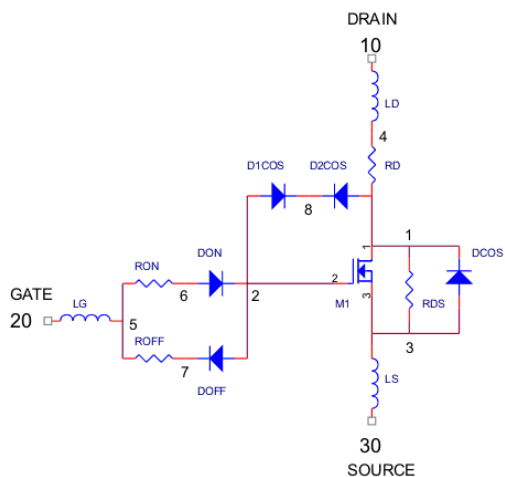


Figure 1 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the DEI web site at [www.directedenergy.com/spice.htm](http://www.directedenergy.com/spice.htm)

Net List:

```
*SYM=POWMOSN
.SUBCKT 102N02A 10 20 30
* TERMINALS: D G S
* 1000 Volt 1.5 Amp 11.0 ohm N-Channel Power MOSFET 10-30-2001
M1 1 2 3 3 DMOS L=1U W=1U
RON 5 6 4.0
DON 6 2 D1
ROFF 5 7 2.0
DOFF 2 7 D1
D1CRS 2 8 D2
D2CRS 1 8 D2
CGS 2 3 500Pf
RD 4 1 11
DCOS 3 1 D3
RDS 1 3 5.0MEG
LS 3 30 .5N
LD 10 4 1N
LG 20 5 1N
.MODEL DMOS NMOS (LEVEL=3 VTO=3 KP=.3)
.MODEL D1 D (IS=.5F CJO=10P BV=100 M=.5 VJ=.2 TT=1N)
.MODEL D2 D (IS=.5F CJO=100P BV=1000 M=.6 VJ=.6 TT=1N RS=10M)
.MODEL D3 D (IS=.5F CJO=150P BV=1000 M=.35 VJ=.6 TT=400N RS=10M)
.ENDS
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