

# TOSHIBA

# TC55257DPI/DFI/DFTI/DTRI-70L,-85L

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

32,768-WORD BY 8-BIT STATIC RAM

## DESCRIPTION

The TC55257DPI/DFI/DFTI/DTRI is a 262,144-bit static random access memory (SRAM) organized as 32,768 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5 V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 5 mA/MHz (typ) and a minimum cycle time of 70 ns. It is automatically placed in low-power mode at 0.3 μA standby current (typ) when chip enable (CE) is asserted high. There are two control inputs.  $\overline{CE}$  is used to select the device and for data retention control, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of - 40° to 85°C, the TC55257DPI/DFI/DFTI/DTRI can be used in environments exhibiting extreme temperature conditions. The TC55257DPI/DFI/DFTI/DTRI is available in a plastic 28-pin dual-in-line package (DIP), plastic 28-pin small-outline package (SOP) and normal and reverse pinout plastic 28-pin thin-small-outline package (TSOP).

## FEATURES

- Low-power dissipation  
Operating: 27.5 mW/MHz (typical)
- Standby current of 2 μA (maximum) at Ta = 25°C
- Single power supply voltage of 5 V ± 10%
- Power down features using  $\overline{CE}$ .
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of - 40° to 85°C

- Access Times (maximum):

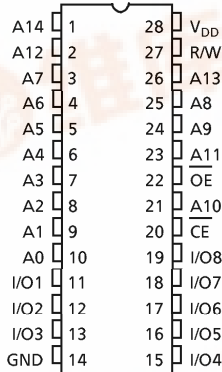
	TC55257DPI/DFI/DFTI/DTRI	
	-70L	-85L
Access Time	70 ns	85 ns
$\overline{CE}$ Access Time	70 ns	85 ns
$\overline{OE}$ Access Time	35 ns	45 ns

- Packages:

DIP28-P-600-2.54 (DPI) (Weight: 4.42 g typ)  
 SOP28-P-450-1.27 (DFI) (Weight: 0.79 g typ)  
 TSOP I 28-P-0.55 (DFTI) (Weight: 0.22 g typ)  
 TSOP I 28-P-0.55A (DTRI) (Weight: 0.22 g typ)

## PIN ASSIGNMENT (TOP VIEW)

### ○ 28 PIN DIP & SOP



### ○ 28 PIN TSOP

(Normal pinout)



(Reverse pinout)



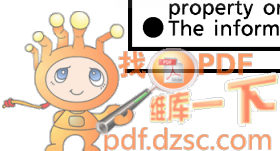
## PIN NAMES

A0 to A14	Address Input
R/W	Read/Write Control
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
I/O1 to I/O8	Data Input/Output
V <sub>DD</sub>	Power (+ 5 V)
GND	Ground

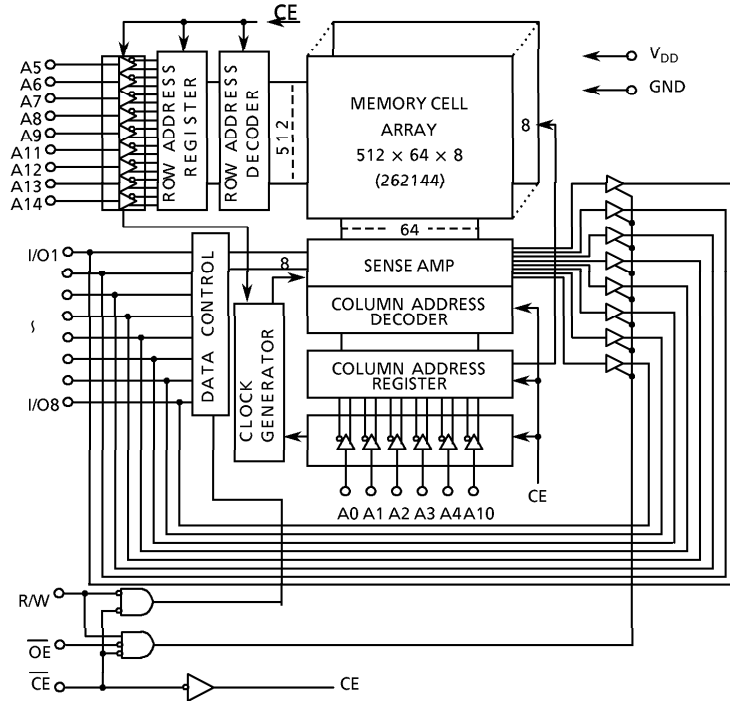
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A <sub>11</sub>	A <sub>9</sub>	A <sub>8</sub>	A <sub>13</sub>	R/W	V <sub>DD</sub>	A <sub>14</sub>	A <sub>12</sub>	A <sub>7</sub>	A <sub>6</sub>	A <sub>5</sub>	A <sub>4</sub>	A <sub>3</sub>
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A <sub>10</sub>

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**BLOCK DIAGRAM**



**OPERATION MODE**

MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D <sub>OUT</sub>	I <sub>DDO</sub>
Write	L	x	L	D <sub>IN</sub>	I <sub>DDO</sub>
Outputs Disabled	L	H	H	High-Z	I <sub>DDO</sub>
Standby	H	x	x	High-Z	I <sub>DDS</sub>

Note: x = don't care. H = logic high. L = logic low.

**ABSOLUTE MAXIMUM VALUES**

SYMBOL	RATING	VALUE	UNIT
V <sub>DD</sub>	Power Supply Voltage	- 0.3 to 7.0	V
V <sub>IN</sub>	Input Voltage	- 0.3* to 7.0	V
V <sub>I/O</sub>	Input/Output Voltage	- 0.5* to V <sub>DD</sub> + 0.5	V
P <sub>D</sub>	Power Dissipation	1.0/0.6**	W
T <sub>solder</sub>	Soldering Temperature (10 s)	260	°C
T <sub>strg</sub>	Storage Temperature	- 55 to 150	°C
T <sub>opr</sub>	Operating Temperature	- 40 to 85	°C

\* - 3.0 V when measured at a pulse width of 50 ns  
 \*\* SOP

**DC RECOMMENDED OPEVALUE CONDITIONS (Ta = - 40° to 85°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Power Supply Voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	Input High Voltage	2.4	-	V <sub>DD</sub> + 0.3	
V <sub>IL</sub>	Input Low Voltage	- 0.3*	-	0.6	
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	

\* - 3.0 V when measured at a pulse width of 50 ns

**DC CHARACTERISTICS (Ta = - 40° to 85°C, V<sub>DD</sub> = 5 V ± 10%)**

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT	
I <sub>IL</sub>	Input Leakage Current	V <sub>IN</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA	
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = 2.4 V	- 1.0	-	-	mA	
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.4 V	4.0	-	-	mA	
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V <sub>IL</sub> or $\overline{OE} = V_{IH}$ V <sub>OUT</sub> = 0 V to V <sub>DD</sub>	-	-	± 1.0	μA	
I <sub>DDO1</sub>	Operating Current	$\overline{CE} = V_{IL}$ R/W = V <sub>IH</sub> , I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>IH</sub> /V <sub>IL</sub>	t <sub>cycle</sub> = 1 μs	-	10	-	mA
			t <sub>cycle</sub> = min	-	-	70	
I <sub>DDO2</sub>	Operating Current	$\overline{CE} = 0.2$ V R/W = V <sub>DD</sub> - 0.2 V, I <sub>OUT</sub> = 0 mA Other Inputs = V <sub>DD</sub> - 0.2 V, 0.2 V	t <sub>cycle</sub> = 1 μs	-	5	-	mA
			t <sub>cycle</sub> = min	-	-	60	
I <sub>DDS1</sub>	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA
I <sub>DDS2</sub>		$\overline{CE} = V_{DD} - 0.2$ V V <sub>DD</sub> = 2.0 to 5.5 V	Ta = - 40° to 85°C	-	-	30	μA
		Ta = 25°C	-	0.3	2		

**CAPACITANCE (Ta = 25°C, f = 1 MHz)**

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = GND	10	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

**AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = - 40° to 85°C, V<sub>DD</sub> = 5 V ± 10%)**

**READ CYCLE**

SYMBOL	PARAMETER	TC55257DPI/DFI/DFTI/DTRI				UNIT
		-70L		-85L		
		MIN	MAX	MIN	MAX	
t <sub>RC</sub>	Read Cycle Time	70	-	85	-	ns
t <sub>ACC</sub>	Address Access Time	-	70	-	85	
t <sub>CO</sub>	Chip Enable Access Time	-	70	-	85	
t <sub>OE</sub>	Output Enable Access Time	-	35	-	45	
t <sub>COE</sub>	Chip Enable Low to Output Active	5	-	5	-	
t <sub>OEE</sub>	Output Enable Low to Output Active	0	-	0	-	
t <sub>OD</sub>	Chip Enable High to Output High-Z	-	25	-	30	
t <sub>ODO</sub>	Output Enable High to Output High-Z	-	25	-	30	
t <sub>OH</sub>	Output Data Hold Time	10	-	10	-	

**WRITE CYCLE**

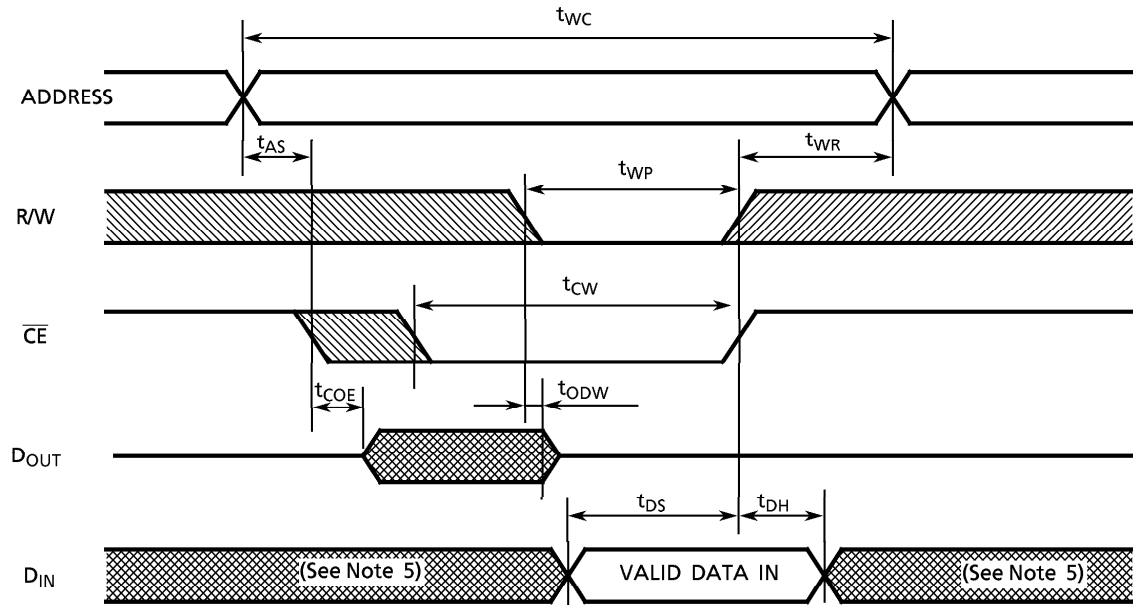
SYMBOL	PARAMETER	TC55257DPL/DFL/DFTL/DTRL				UNIT
		-70L		-85L		
		MIN	MAX	MIN	MAX	
t <sub>WC</sub>	Write Cycle Time	70	-	85	-	ns
t <sub>WP</sub>	Write Pulse Width	50	-	60	-	
t <sub>CW</sub>	Chip Enable to End of Write	60	-	65	-	
t <sub>AS</sub>	Address Setup Time	0	-	0	-	
t <sub>WR</sub>	Write Recovery Time	0	-	0	-	
t <sub>ODW</sub>	R/W Low to Output High-Z	-	25	-	30	
t <sub>OEW</sub>	R/W High to Output Active	0	-	0	-	
t <sub>DS</sub>	Data Setup Time	30	-	40	-	
t <sub>DH</sub>	Data Hold Time	0	-	0	-	

**AC TEST CONDITIONS**

Output load: 100 pF + one TTL gate  
 Input pulse level: 0.4 V, 2.6 V  
 Timing measurements: 1.5 V  
 ReferenChip Enable level: 1.5 V  
 t<sub>R</sub>, t<sub>F</sub>: 5 ns



WRITE CYCLE 2 ( $\overline{CE}$  CONTROLLED) (See Note 4)



Note: (1) R/W remains HIGH for the read cycle.

(2) If  $\overline{CE}$  goes LOW coincident with or after R/W goes LOW, the outputs will remain at high impedance.

(3) If  $\overline{CE}$  goes HIGH coincident with or before R/W goes HIGH, the outputs will remain at high impedance.

(4) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

(5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

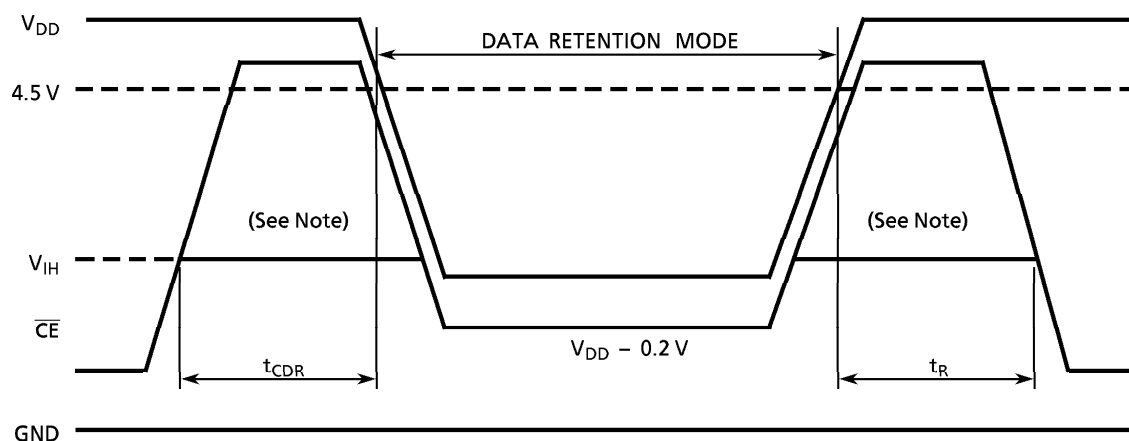
**DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V <sub>DH</sub>	Data Retention Supply Voltage	2.0	-	5.5	V
I <sub>DD2</sub>	Standby Current	V <sub>DH</sub> = 3.0 V	-	15*	μA
		V <sub>DH</sub> = 5.5 V	-	30	μA
t <sub>CDR</sub>	Chip Deselect to Data Retention Mode Time	0	-	-	
t <sub>R</sub>	Recovery Time	t <sub>RC</sub> (See Note)	-	-	ns

\* 2 μA (max) at Ta = - 40° to 40°C

Note: Read cycle time.

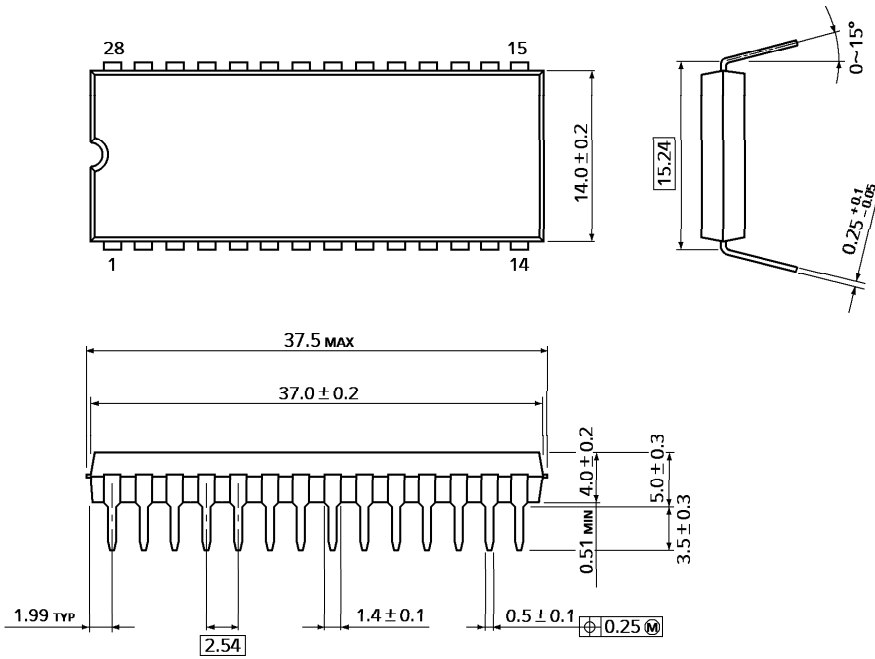
**CE CONTROLLED DATA RETENTION MODE**



Note: When  $\overline{CE}$  is operating at the V<sub>IH</sub> level (2.4 V), the standby current is given by I<sub>DD1</sub> during the transition of V<sub>DD</sub> from 4.5 to 2.6 V.

PACKAGE DIMENSIONS (DIP28-P-600-2.54)

Units in mm

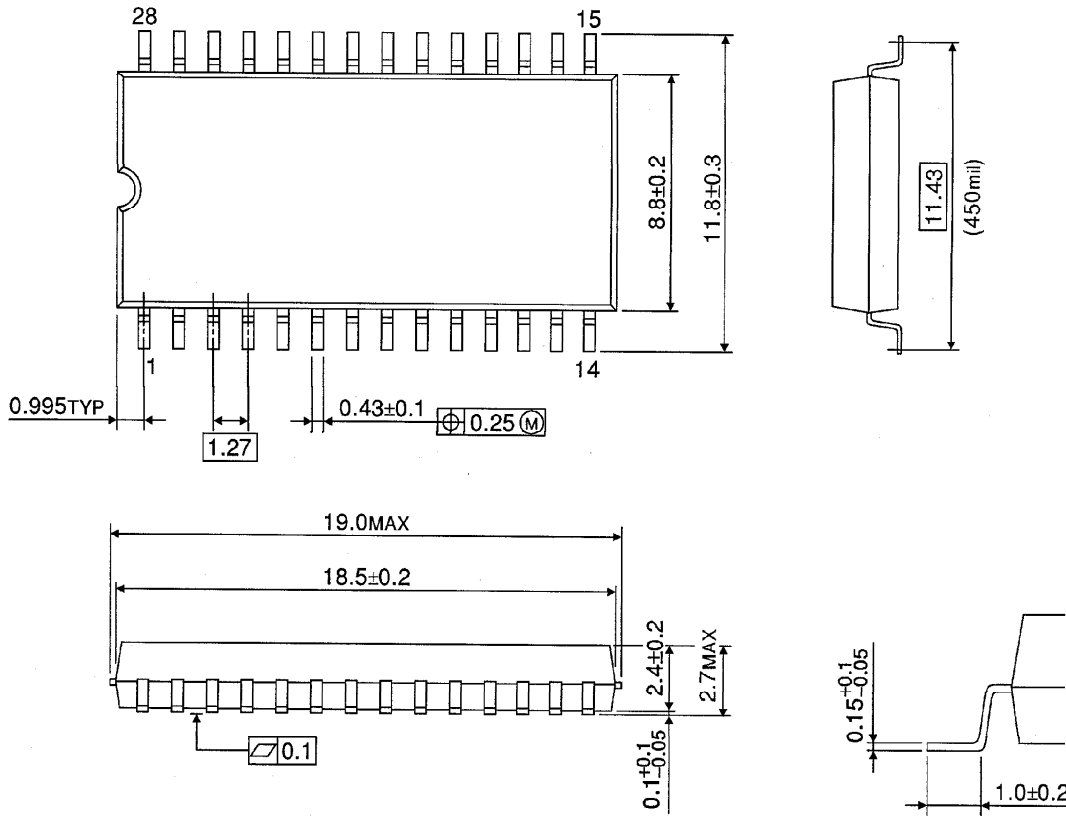


Weight: 4.42 g (typ)



PACKAGE DIMENSIONS (SOP28-P-450-1.27)

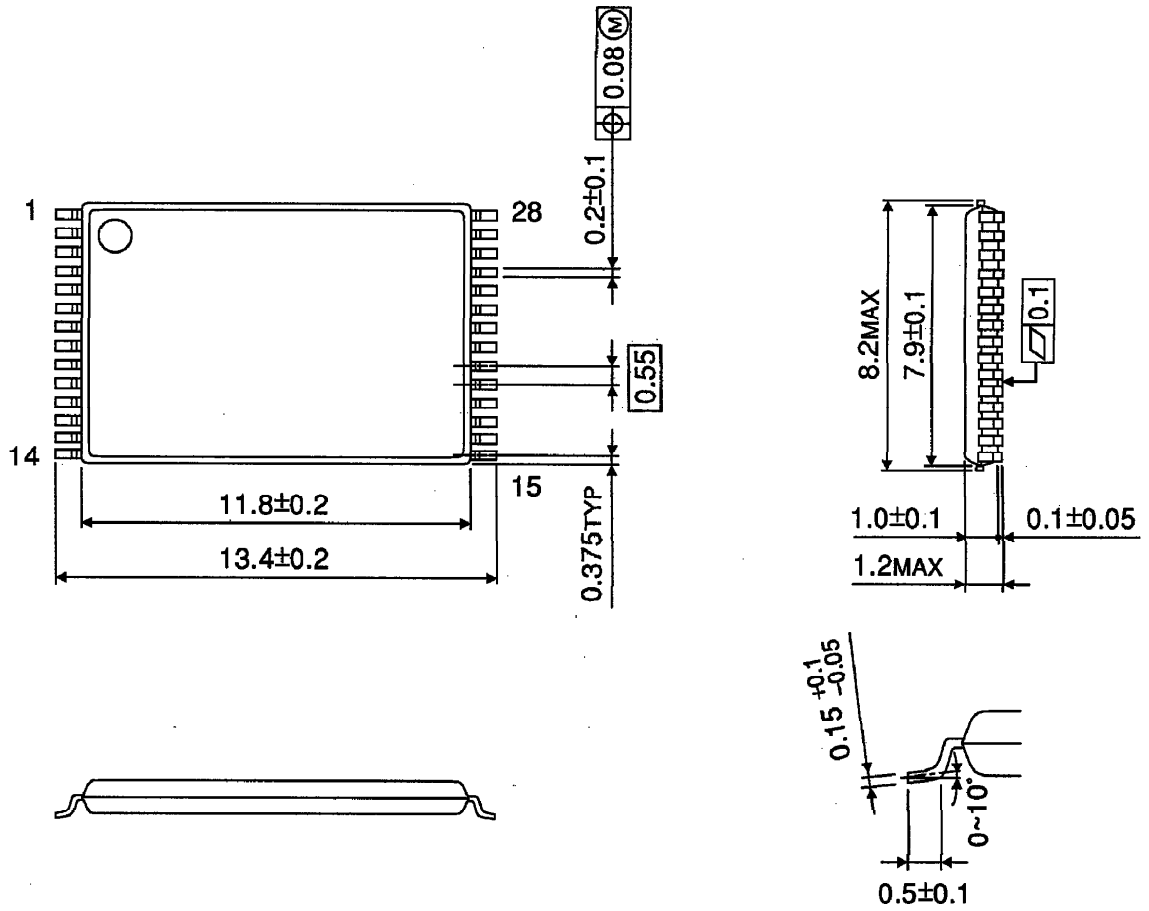
Units in mm



Weight: 0.79 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55)

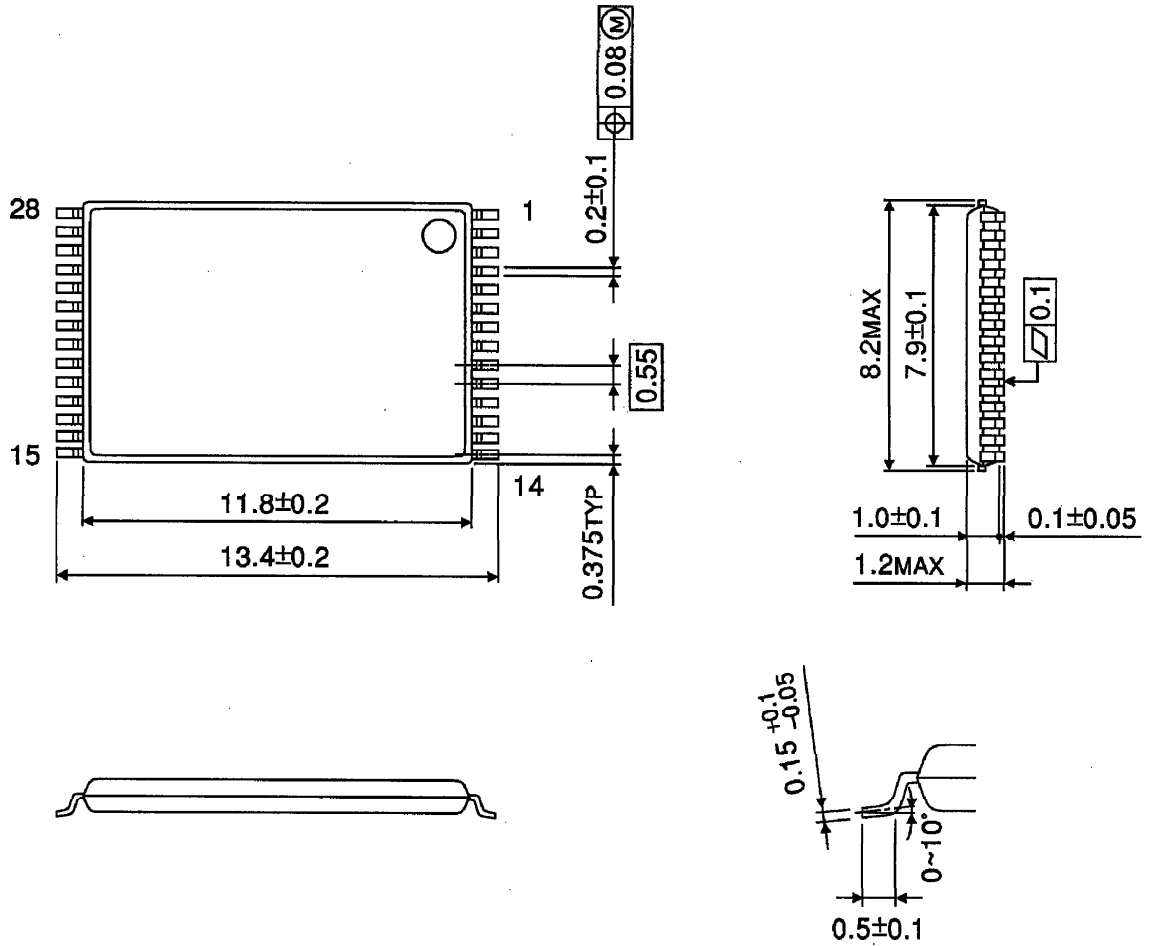
Units in mm



Weight: 0.22 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55A)

Units in mm



Weight: 0.22 g (typ)