

TOSHIBA**TC55257DPI/DFI/DFTI/DTRI-70V,-85V**

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

32,768 WORDS×8 BIT STATIC RAM

DESCRIPTION

The TC55257DPI is 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 2.7~5.5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 5 mA / MHz (Typ.) and minimum cycle time of 70 ns.

When $\overline{CE}$ is a logical high, the device is placed in low power standby mode in which standby current is 0.3 μ A typically. The TC55257DPI has two control inputs. Chip enable ($\overline{CE}$) allows for device selection and data retention control, and an output enable input ($\overline{OE}$) provides fast memory access. Thus the TC55257DPI is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. And TC55257DPI guarantees $-40\sim 85^{\circ}\text{C}$ operating temperature, so TC55257DPI is suitable for use in wide operating temperature system.

The TC55257DPI is offered in a standard dual-in-line 28 pin plastic package (0.6 inch width), small-out-line plastic package and thin-small-out-line plastic package (forward type, reverse type).

FEATURES

- Low Power Dissipation
27.5 mW / MHz (Typ.) Operating
- Standby Current : 2 μ A (Max.) at $T_a = 25^{\circ}\text{C}$
- Single Power Supply : 2.7~5.5 V
- Power Down Feature : $\overline{CE}$
- Data retention Supply Voltage : 2.0~5.5 V
- Directly TTL Compatible
: All Inputs and Outputs
- Wide Temperature Operating : $-40\sim 85^{\circ}\text{C}$

- Access Time (Max.) :

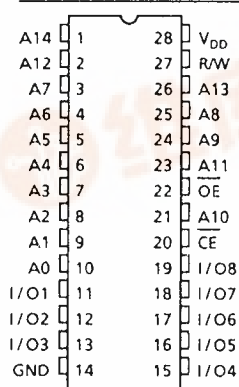
	5V $\pm$ 10%		2.7~5.5V	
	-70V	-85V	-70V	-85V
Access Time	70ns	85ns	120ns	150ns
$\overline{CE}$ Access Time	70ns	85ns	120ns	150ns
$\overline{OE}$ Access Time	35ns	45ns	70ns	75ns

- Package :

DIP28-P-600-2.54 (DPI) (Weight: 4.42 g typ)
 SOP28-P-450-1.27 (DFI) (Weight: 0.79 g typ)
 TSOP I 28-P-0.55 (DFTI) (Weight: 0.22 g typ)
 TSOP I 28-P-0.55A (DTRI) (Weight: 0.22 g typ)

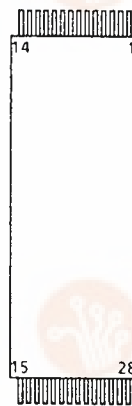
PIN CONNECTION (TOP VIEW)

○ 28 PIN DIP & SOP



○ 28 PIN TSOP

(forward type)



(reverse type)

**PIN NAME**

A0~A14	Address Inputs
R/W	Read / Write Control Input
$\overline{OE}$	Output Enable Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data Input / Output
V_{DD}	Power
GND	Ground

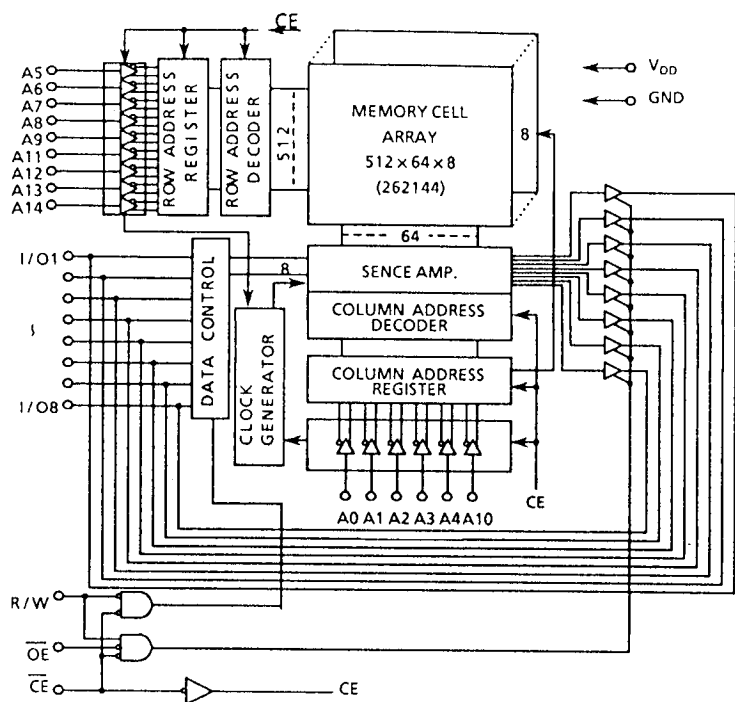
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
PIN NAME	$\overline{OE}$	A ₁₁	A ₉	A ₈	A ₁₃	R/W	V_{DD}	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄	A ₃
PIN NO.	15	16	17	18	19	20	21	22	23	24	25	26	27	28
PIN NAME	A ₂	A ₁	A ₀	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE}$	A ₁₀

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BLOCK DIAGRAM



OPERATION MODE

OPERATION MODE	$\overline{CE}$	$\overline{OE}$	R/W	I/O1~I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	*	L	D _{IN}	I _{DDO}
Output Deselect	L	H	H	High-Z	I _{DDO}
Standby	H	*	*	High-Z	I _{DDs}

* : H or L

ABSOLUTE MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V _{DD}	Power Supply Voltage	-0.3~7.0	V
V _{IN}	Input Voltage	-0.3*~7.0	V
V _{I/O}	Input and Output Voltage	-0.5*~V _{DD} +0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg}	Storage Temperature	-55~150	°C
T _{opr}	Operating Temperature	-40~85	°C

* : -3.0 V at pulse width 50 ns

** : SOP

D.C. RECOMMENDED OPERATING CONDITIONS ($T_a = -40 \sim 85^\circ\text{C}$)

SYMBOL	PARAMETER	5V $\pm$ 10%			2.7~5.5V			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{DD}	Power Supply Voltage	4.5	—	5.5	2.7	—	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 0.3$	$V_{DD} - 0.2$	—	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3*	—	0.6	-0.3*	—	0.2	
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	2.0	—	5.5	

*: -3.0V at pulse width at 50ns Max.

D.C. and OPERATING CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$, $V_{DD} = 5\text{V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{IL}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{OH}	Output High Current	$V_{OH} = 2.4\text{V}$	-1.0	—	—	mA
I_{OL}	Output Low Current	$V_{OL} = 0.4\text{V}$	4.0	—	—	mA
I_{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or $R/W = V_{IL}$ or $\overline{OE} = V_{IH}$, $V_{OUT} = 0 \sim V_{DD}$	—	—	± 1.0	μA
I_{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ $R/W = V_{IH}$, $I_{OUT} = 0\text{mA}$ Other Input = V_{IH} / V_{IL}	$t_{\text{cycle}} = 1\mu\text{s}$	—	10	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	
I_{DDO2}		$\overline{CE} = 0.2\text{V}$ $R/W = V_{DD} - 0.2\text{V}$, $I_{OUT} = 0\text{mA}$ Other Input = $V_{DD} - 0.2\text{V} / 0.2\text{V}$	$t_{\text{cycle}} = 1\mu\text{s}$	—	5	mA
			$t_{\text{cycle}} = \text{Min. cycle}$	—	—	
I_{DDs1}	Standby Current	$\overline{CE} = V_{IH}$	—	—	—	mA
I_{DDs2}		$\overline{CE} = V_{DD} - 0.2$ $V_{DD} = 2.0\text{V} \sim 5.5\text{V}$	$T_a = -40 \sim 85^\circ\text{C}$	—	—	μA
			$T_a = 25^\circ\text{C}$	—	0.3	

D.C. and OPERATING CHARACTERISTICS (Ta = -40~85 °C, V_{DD} = 3V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION			MIN.	TYP.	MAX.	UNIT
I _{IL}	Input Leakage Current	V _{IN} = 0 ~ V _{DD}			—	—	± 1.0	μA
I _{OH}	Output High Current	V _{OH} = V _{DD} - 0.2V			- 0.1	—	—	mA
I _{OL}	Output Low Current	V _{OL} = 0.2V			0.1	—	—	mA
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$, V _{OUT} = 0 ~ V _{DD}			—	—	± 1.0	μA
I _{DDO2}	Operating Current	$\overline{CE} = 0.2V$ R/W = V _{DD} - 0.2V, I _{OUT} = 0mA Other Input = V _{DD} - 0.2V / 0.2V	T _{cycle}	Min.	—	—	20	mA
				1μs	—	—	5	
I _{DD52}	Standby Current	$\overline{CE} = V_{DD} - 0.2V$	V _{DD} = 3V ± 10%	Ta = 25°C	—	1	1.5	μA
				Ta = -40 ~ 85°C	—	—	20	
			V _{DD} = 3.0V	Ta = 25°C	—	—	1	
				Ta = -40 ~ 40°C	—	—	2	
				Ta = -40 ~ 85°C	—	—	15	

CAPACITANCE (Ta = 25 °C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note : This parameter periodically sampled is not 100% tested.

A.C. CHARACTERISTICS (Ta = - 40~85 °C, V_{DD} = 5 V ± 10%)
Read Cycle

SYMBOL	PARAMETER	TC55257DPI / DFI / DFTI / DTRI				UNIT
		- 70V		- 85V		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	70	–	85	–	ns
t _{ACC}	Address Access Time	–	70	–	85	
t _{CO}	$\overline{\text{CE}}$ Access Time	–	70	–	85	
t _{OE}	Output Enable to Output in Valid	–	35	–	45	
t _{COE}	Chip Enable to Output in Low-Z	5	–	5	–	
t _{OOE}	Output Enable to Output in Low-Z	0	–	0	–	
t _{OD}	Chip Enable to Output in High-Z	–	25	–	30	
t _{ODO}	Output Enable to Output in High-Z	–	25	–	30	
t _{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

SYMBOL	PARAMETER	TC55257DPI / DFI / DFTI / DTRI				UNIT
		- 70V		- 85V		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	70	–	85	–	ns
t _{WP}	Write Pulse Width	50	–	60	–	
t _{CW}	Chip Selection to End of Write	60	–	65	–	
t _{AS}	Address Set up Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R / W to Output in High-Z	–	25	–	30	
t _{OEW}	R / W to Output in Low-Z	0	–	0	–	
t _{DS}	Data Set up Time	30	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

A.C. Test Conditions

Output Load : 100 pF + 1 TTL Gate (- 70V, - 85V)
 Input Pulse Level : 0.4 V, 2.6 V
 Timing Measurement : 1.5 V
 Reference Level : 1.5 V
 t_r, t_f : 5 ns

A.C. CHARACTERISTICS (Ta = -40 ~ 85°C, VDD = 2.7 ~ 5.5V)

Read Cycle

SYMBOL	PARAMETER	TC55257DPI / DFI / DFTI / DTRI				UNIT
		- 70V		- 85V		
		MIN.	MAX.	MIN.	MAX.	
t _{RC}	Read Cycle Time	120	–	150	–	ns
t _{ACC}	Address Access Time	–	120	–	150	
t _{CO}	$\overline{CE}$ Access Time	–	120	–	150	
t _{OE}	Output Enable to Output in Valid	–	70	–	75	
t _{COE}	Chip Enable to Output in Low-Z	5	–	5	–	
t _{OEE}	Output Enable to Output in Low-Z	0	–	0	–	
t _{OD}	Chip Enable to Output in High-Z	–	50	–	50	
t _{ODO}	Output Enable to Output in High-Z	–	50	–	50	
t _{OH}	Output Data Hold Time	10	–	10	–	

Write Cycle

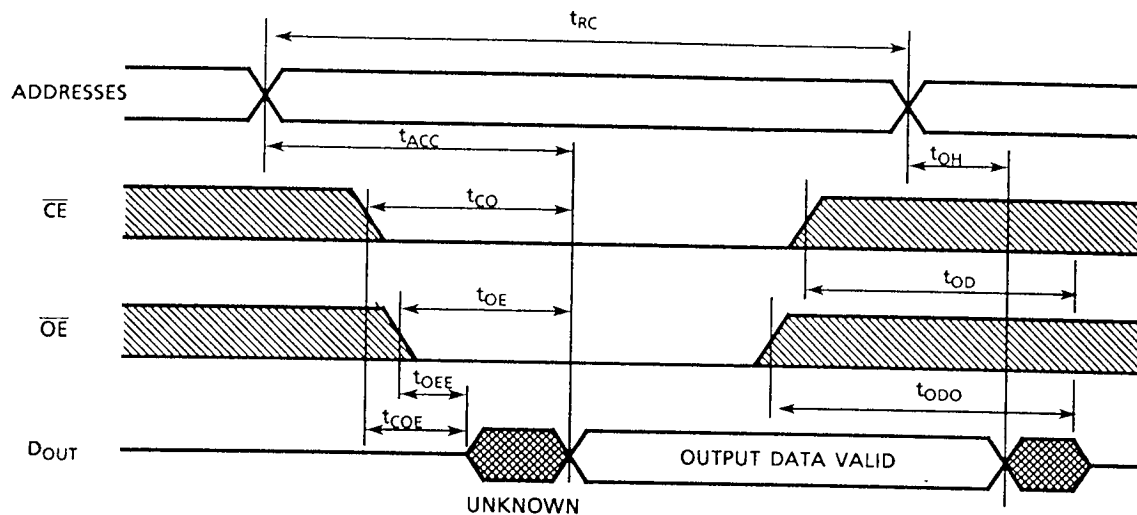
SYMBOL	PARAMETER	TC55257DPI / DFI / DFTI / DTRI				UNIT
		– 70V		– 85V		
		MIN.	MAX.	MIN.	MAX.	
t _{WC}	Write Cycle Time	120	–	150	–	ns
t _{WP}	Write Pulse Width	80	–	100	–	
t _{CW}	Chip Selection to End of Write	100	–	120	–	
t _{AS}	Address Set up Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W to Output in High-Z	–	50	–	50	
t _{OEW}	R/W to Output in Low-Z	0	–	0	–	
t _{DS}	Data Set up Time	50	–	60	–	
t _{DH}	Data Hold Time	0	–	0	–	

A.C. TEST CONDITIONS

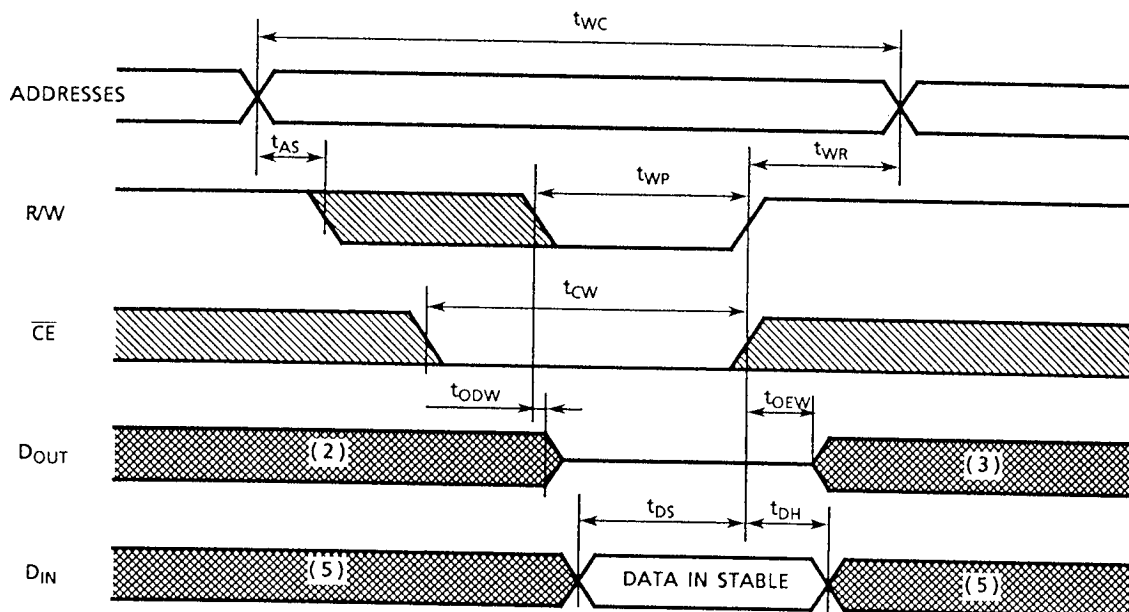
- Output Load : 100pF (Include Jig)
- Input Pulse Level : VDD - 0.2V / 0.2V
- Timing Measurement V_{IN} : 1.5V
Reference Level V_{OUT} : 1.5V
- t_r, t_f : 5ns

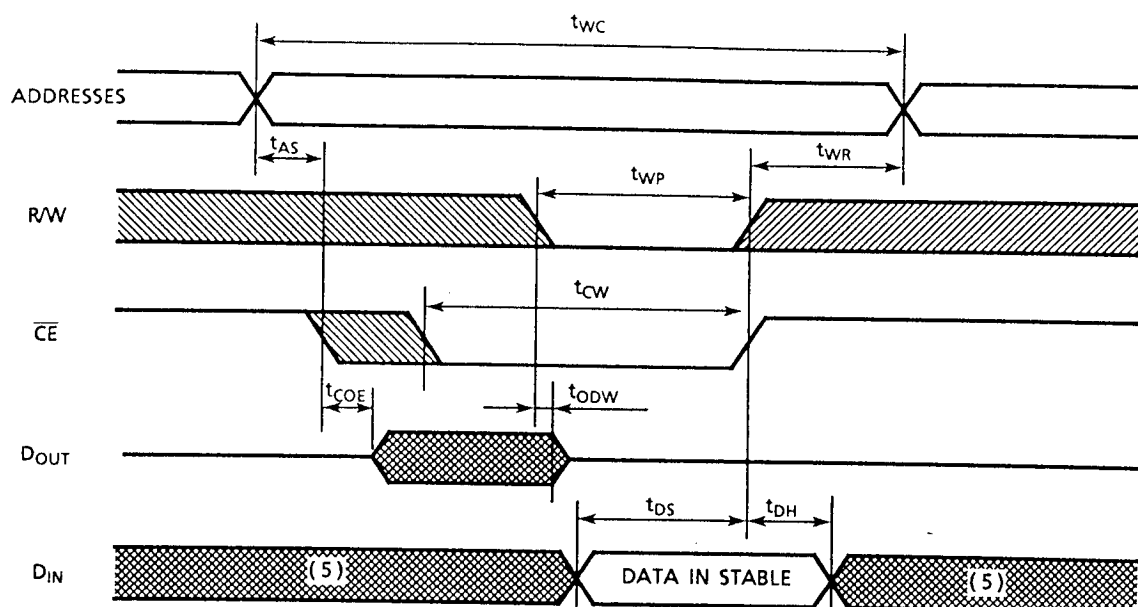
TIMING WAVEFORMS

Read Cycle (1)



Write Cycle 1 (4) (R/W Controlled Write)



Write Cycle 2 (4) ($\overline{\text{CE}}$ Controlled Write)


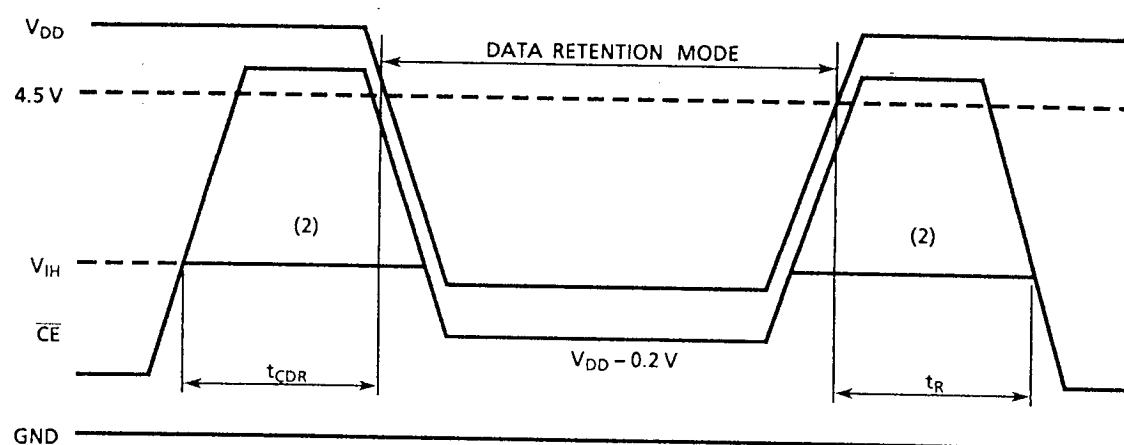
Note : (1) R/W is High for read cycle.

- (2) Assuming that $\overline{\text{CE}}$ low transition occurs coincident with or after R / W Low transition, Outputs remain a high impedance state.
- (3) Assuming that $\overline{\text{CE}}$ High transition occurs coincident with or prior to R / W High transition, Outputs remain a high impedance state.
- (4) Assuming that $\overline{\text{OE}}$ is High for Write Cycle, Outputs are in high impedance state during this period.
- (5) The I/O may be in the output state at this time, input signals of opposite phase must not be applied.

DATA RETENTION CHARACTERISTICS ($T_a = -40 \sim 85^\circ\text{C}$)

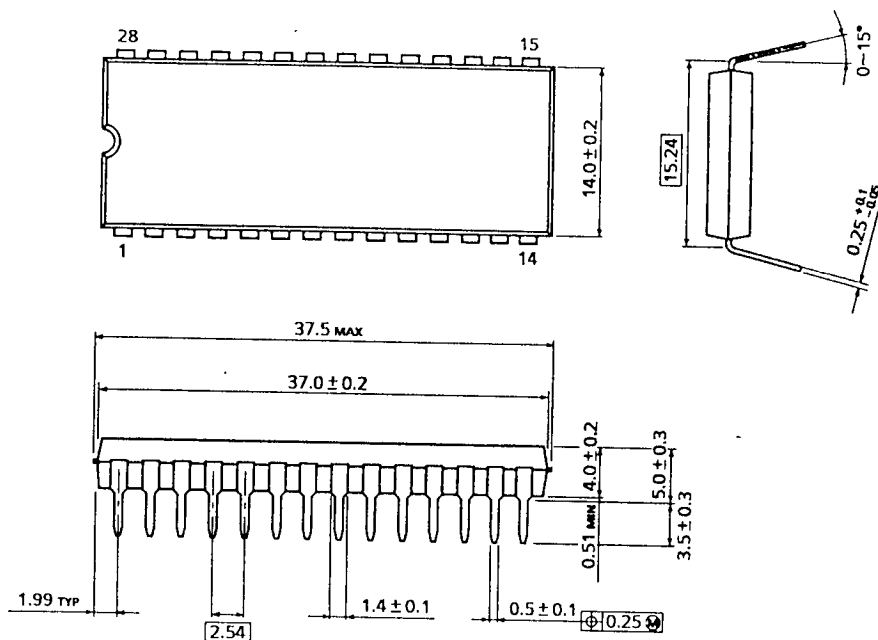
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DH}	Data Retention Supply Voltage	2.0	—	5.5	V
I_{DD52}	Standby Supply Current	$V_{DH} = 3.0\text{ V}$	—	15*	μA
		$V_{DH} = 5.5\text{ V}$	—	30	μA
t_{CDR}	Chip Deselection to Data Retention Mode	—	—	—	ns
t_R	Recovery Time	—	—	—	ns

Note (1) : Read Cycle Time.

 *) $2\mu\text{A}$ (Max.) $T_a = -40 \sim 40^\circ\text{C}$
 $\overline{\text{CE}}$ Controlled Data Retention Mode

 Note (2) : If the V_{IH} of $\overline{\text{CE}}$ is 2.4 V in operation, I_{DD51} current flows during the period that the V_{DD} voltage is going down from 4.5 V to 2.6 V

PACKAGE DIMENSIONS (DIP28-P-600-2.54)

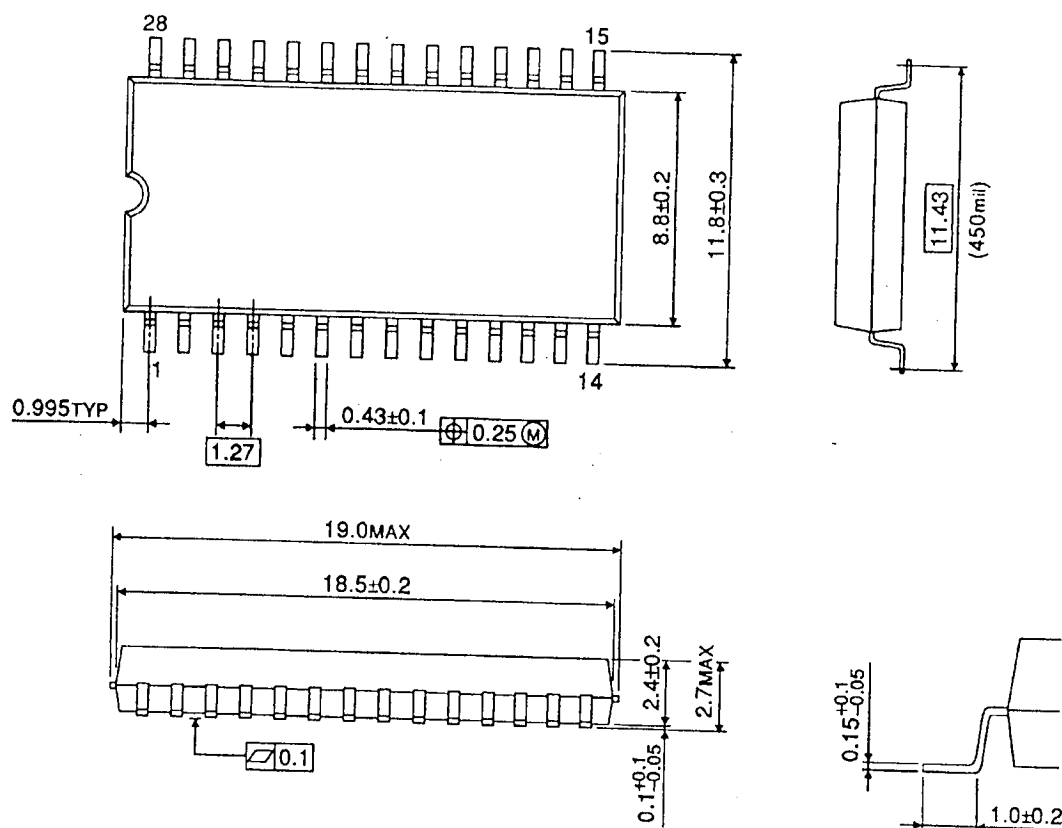
Units in mm



Weight: 4.42 g (typ)

PACKAGE DIMENSIONS (SOP28-P-450-1.27)

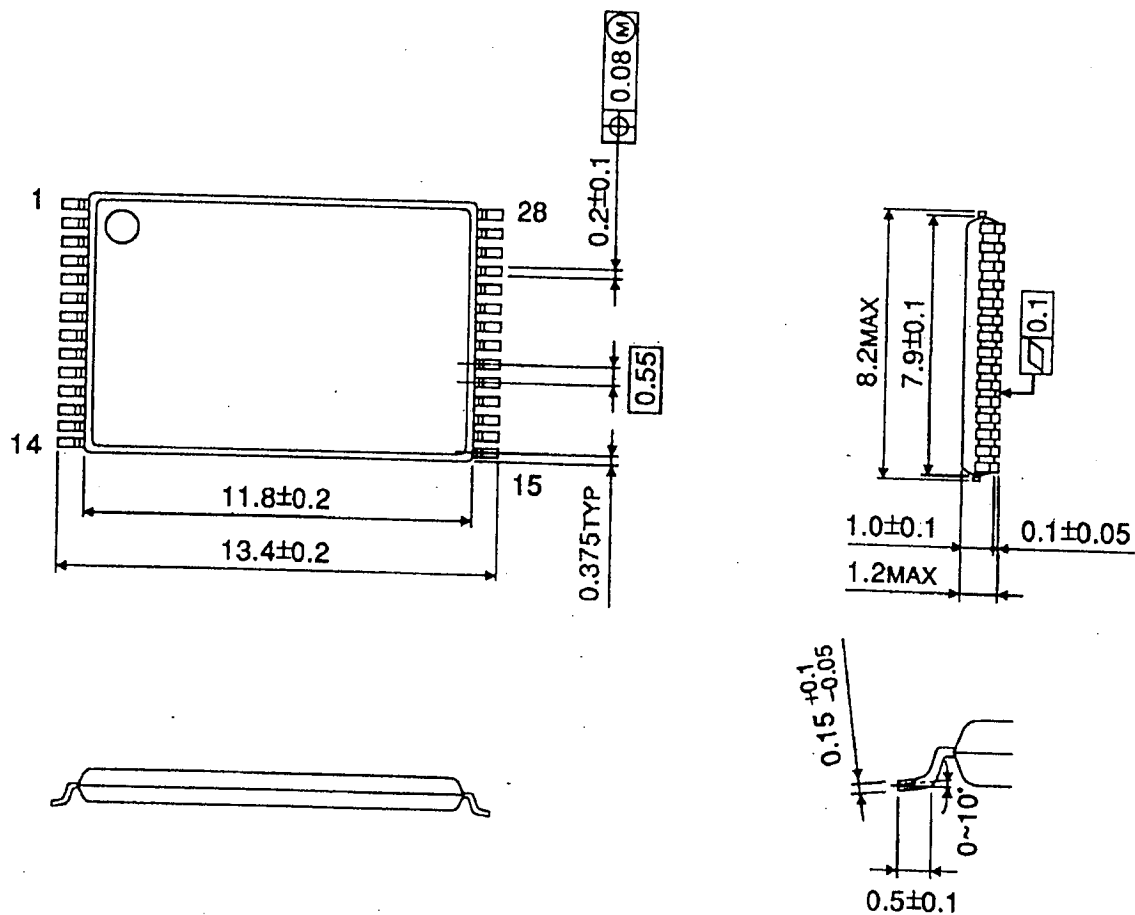
Units in mm



Weight: 0.79 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55)

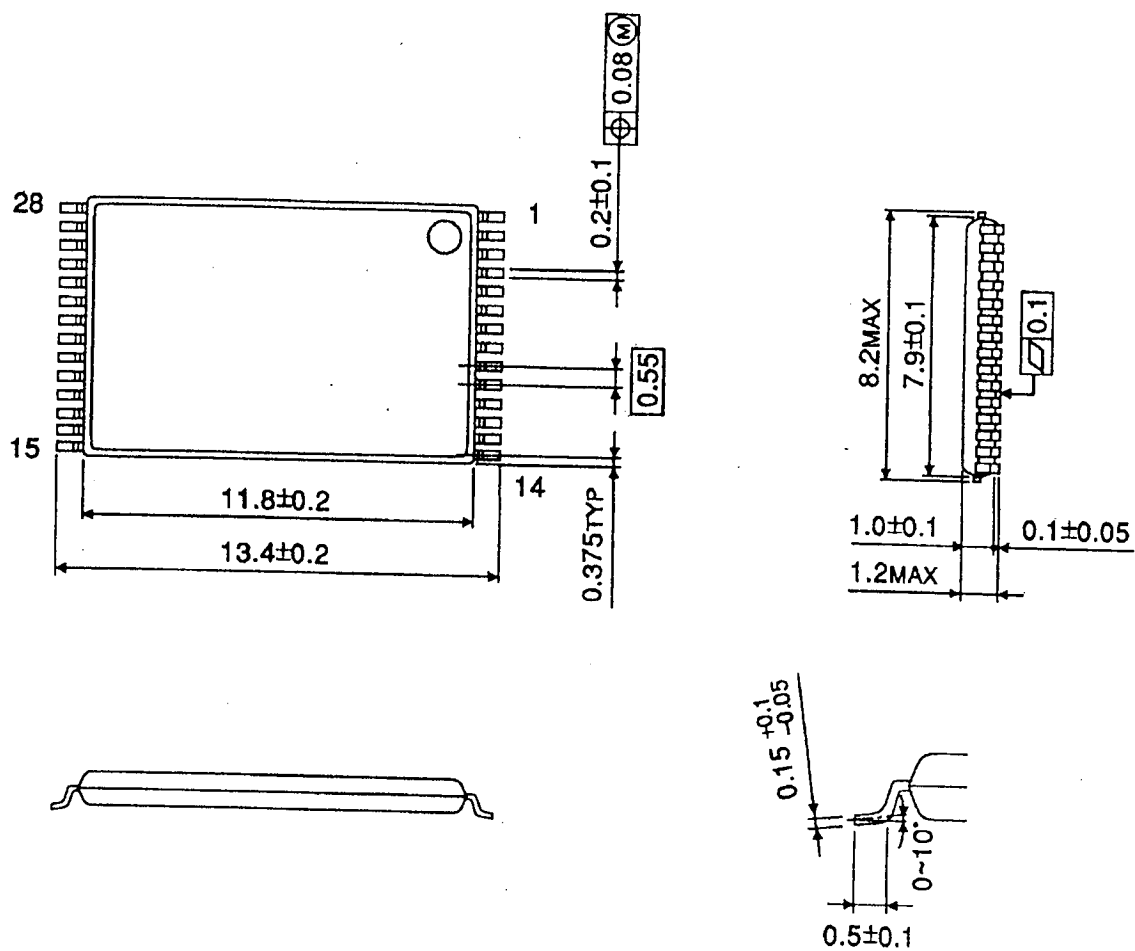
Units in mm



Weight: 0.22 g (typ)

PACKAGE DIMENSIONS (TSOP I 28-P-0.55A)

Units in mm



Weight: 0.22 g (typ)