



New Product

DG2012

Vishay Siliconix

Low-Voltage Single SPDT Analog Switch

FEATURES

- Low Voltage Operation (1.8 V to 5.5 V)
- Low On-Resistance - $r_{DS(on)}$: 1 Ω Typ.
- Fast Switching - t_{ON} : 17 ns, t_{OFF} : 13 ns
- Low Leakage
- TTL/CMOS Compatible
- 6-Pin SC-70 Package

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Cellular Phones
- Communication Systems
- Portable Test Equipment
- Battery Operated Systems
- Sample and Hold Circuits

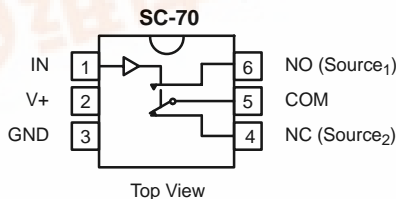
DESCRIPTION

The DG2012 is a single-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 17 ns, t_{OFF} : 13 ns), low on-resistance ($r_{DS(on)}$: 1 Ω) and small physical size (SC70), the DG2012 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2012 is built on Vishay Siliconix's low voltage submicron CMOS process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG2012.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Device Marking: E7xx

TRUTH TABLE

Logic	NC	NO
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION

Temp Range	Package	Part Number
-40 to 85°C	SC70-6	DG2012DL





ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (NO, NC and COM Pins)	± 100 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	± 300 mA
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages)^b

6-Pin SO70 ^c	250 mW
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Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 3.1 mW/°C above 70°C

SPECIFICATIONS (V+ = 2.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 2.0 V, ± 10%, V _{IN} = 0.4 or 1.6 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 1.8 V, V _{COM} = 0.2 V/0.9 V I _{NO} , I _{NC} = 10 mA	Room Full ^d		2.7 2.7	5.3 5.3	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 1.8 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			3	
r _{ON} Match ^d	Δr _{ON}		Room			0.25	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V+ = 2.2 V V _{NO} , V _{NC} = 0.5 V/1.5 V, V _{COM} = 1.5 V/0.5 V	Room Full ^d	-0.5 -5.0		0.5 5.0	nA
	I _{COM(off)}		Room Full ^d	-0.5 -5.0		0.5 5.0	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 2.2 V, V _{NO} , V _{NC} = V _{COM} = 0.5 V/1.5 V	Room Full ^d	-0.5 -5.0		0.5 5.0	
Digital Control							
Input High Voltage	V _{INH}		Full	1.6			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance ^d	C _{in}		Full		3		pF
Input Current ^f	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _{NO} or V _{NC} = 1.5 V, R _L = 300 Ω, C _L = 35 pF Figures 1 and 2	Room Full ^d		43	63 65	ns
Turn-Off Time ^d	t _{OFF}		Room Full ^d		23	45 46	
Break-Before-Make Time ^d	t _d		Room	2			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		7		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk ^d	X _{TALK}		Room		-64		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		22		pF
Channel-On Capacitance ^d	C _{ON}		Room		58		



SPECIFICATIONS (V+ = 3.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.6 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V, I _{NO} I _{NC} = 10 mA	Room Full		1.4 1.6	2.1 2.3	Ω
r _{ON} Flatness	r _{ON} Flatness	V+ = 2.7 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			0.85	
r _{ON} MatchFlat	Δr _{ON}		Room			0.25	
Switch Off Leakage Current ^f	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V V _{NO} , V _{NC} = 1 V/3 V, V _{COM} = 3 V/1 V	Room Full	-0.5 -5.0		0.5 5.0	nA
	I _{COM(off)}		Room Full	-0.5 -5.0		0.5 5.0	
Channel-On Leakage Current ^f	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 1 V/3 V	Room Full	-0.5 -5.0		0.5 5.0	
Digital Control							
Input High Voltage	V _{INH}		Full	2			V
Input Low Voltage	V _{INL}		Full			0.6	
Input Capacitance ^d	C _{in}		Full		3		pF
Input Current ^f	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		27	47 48	ns
Turn-Off Time	t _{OFF}		Room Full		17	37 38	
Break-Before-Make Time	t _d		Room	1			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		10		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk ^d	X _{TALK}		Room		-64		
NO, NC Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		21		pF
Channel-On Capacitance ^d	C _{ON}		Room		57		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V _{IN} = 0 or V+			0.01	1.0	μA



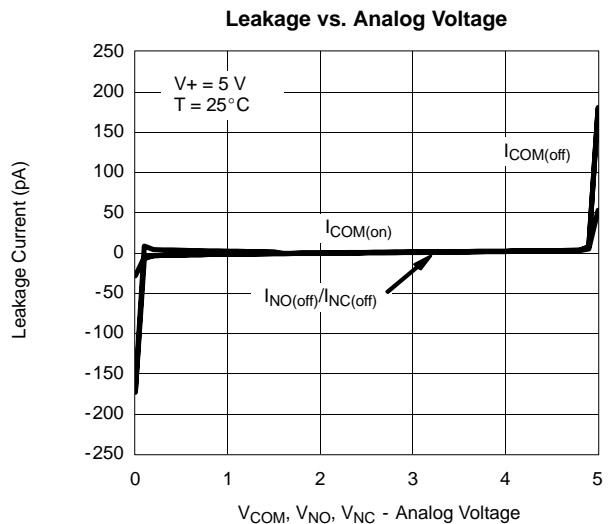
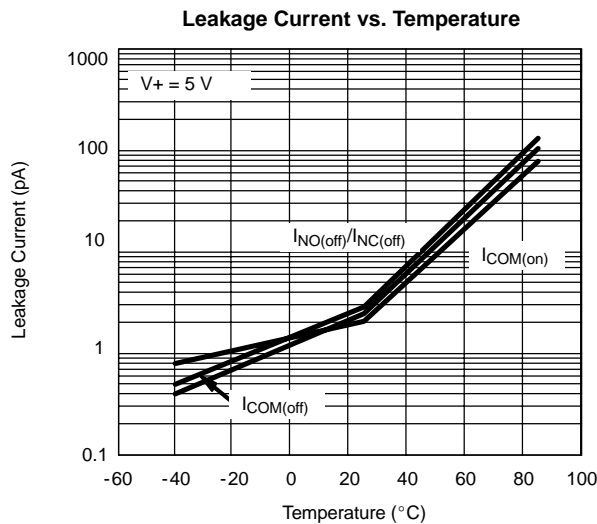
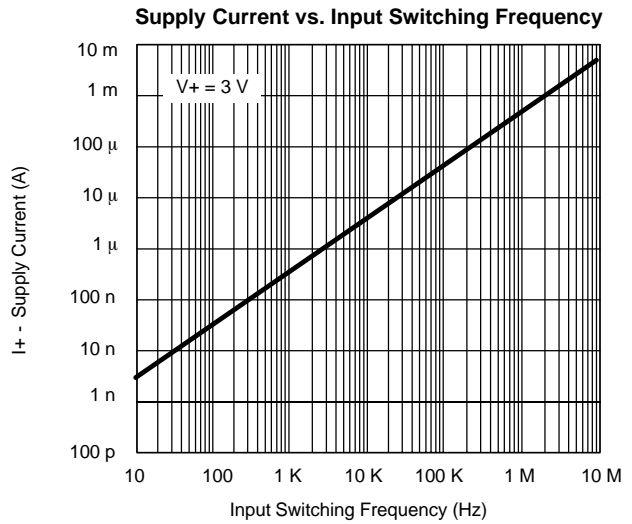
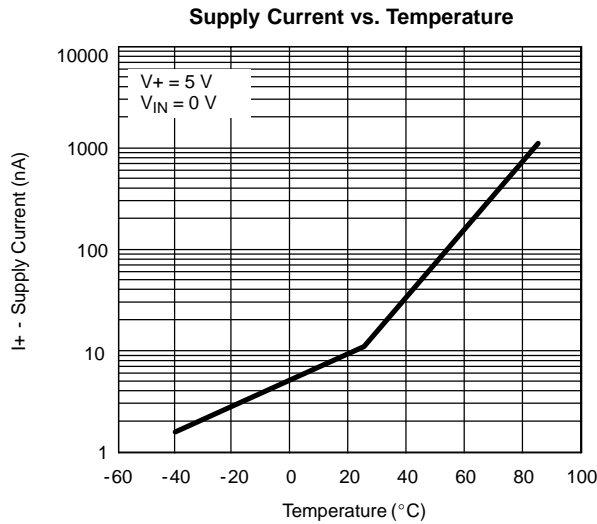
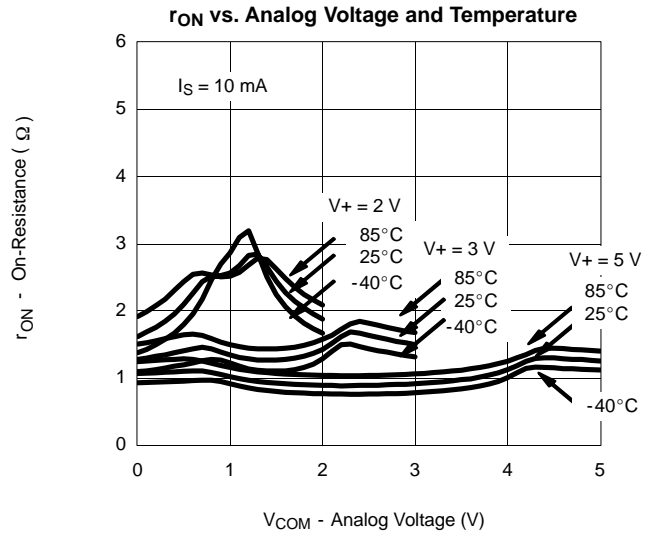
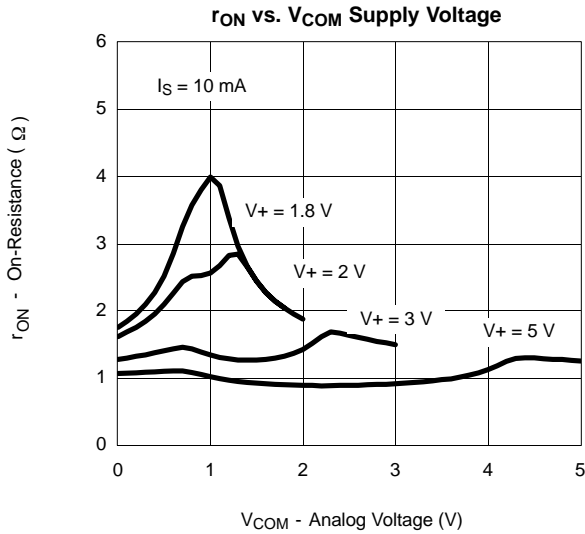
SPECIFICATIONS (V+ = 5.0 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, VIN = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 4.5 V, V _{COM} = 0.5 V/2.5 V I _{NO} , I _{NC} = 10 mA	Room Full		1.0 1.2	1.8 1.9	Ω
r _{ON} Flatness ^d	r _{ON} Flatness	V+ = 4.5 V, V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			0.55	
r _{ON} Match ^d	Δr _{ON}		Room			0.25	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 5.0 V V _{NO} , V _{NC} = 0.5 V/4.5 V, V _{COM} = 4.5 V/0.5 V	Room Full	-0.5 -5.0		0.5 5.0	nA
	I _{COM(off)}		Room Full	-0.5 -5.0		0.5 5.0	
Channel-On Leakage Current	I _{COM(on)}	V+ = 5.0 V, V _{NO} , V _{NC} = V _{COM} = 0.5 V/4.5 V	Room Full	-0.5 -5.0		0.5 5.0	
Digital Control							
Input High Voltage	V _{INH}		Full	2.4			V
Input Low Voltage	V _{INL}		Full			0.8	
Input Capacitance	C _{in}		Full		3		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	-1		1	μA
Dynamic Characteristics							
Turn-On Time ^d	t _{ON}	V _{NO} or V _{NC} = 3 V, R _L = 300 Ω, C _L = 35 pF Figure 1 and 2	Room Full		17	38 39	ns
Turn-Off Time ^d	t _{OFF}		Room Full		13	32 33	
Break-Before-Make Time ^d	t _d		Room	1			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω, Figure 3	Room		20		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-63		dB
Crosstalk ^d	X _{TALK}		Room		-64		
Source-Off Capacitance ^d	C _{NO(off)} , C _{NC(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		20		pF
Channel-On Capacitance ^d	C _{ON}		Room		56		

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 5-V leakage testing, not production tested.



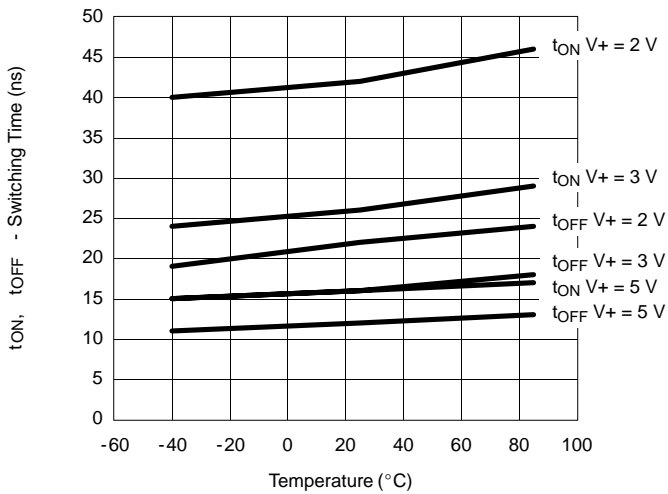
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



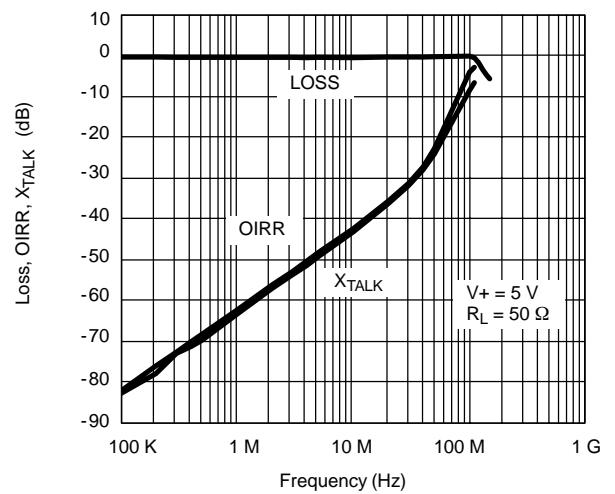


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

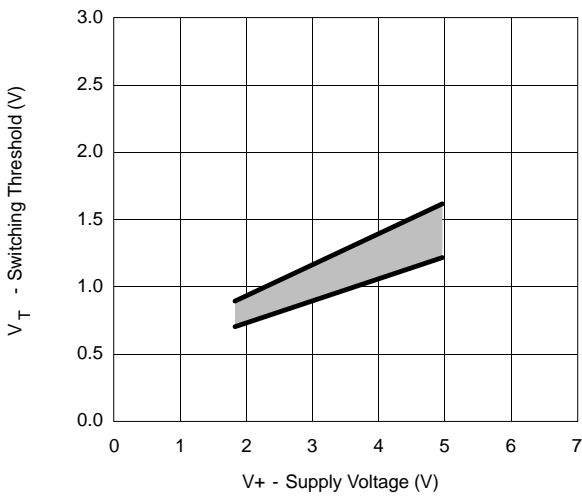
Switching Time vs. Temperature and Supply Voltage



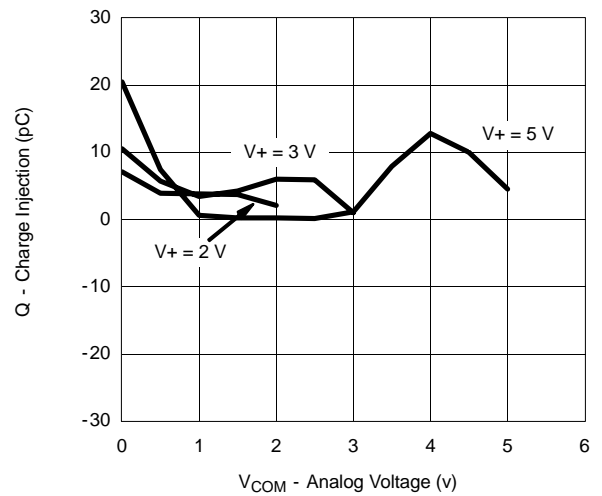
Insertion Loss, Off-Isolation, Crosstalk vs. Frequency



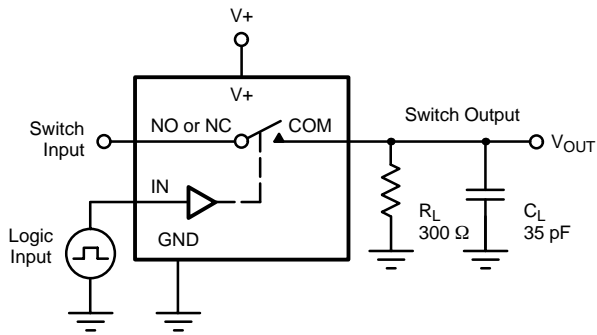
Switching Threshold vs. Supply Voltage



Charge Injection vs. Analog Voltage

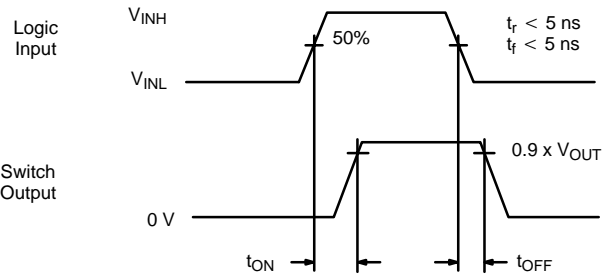


TEST CIRCUITS



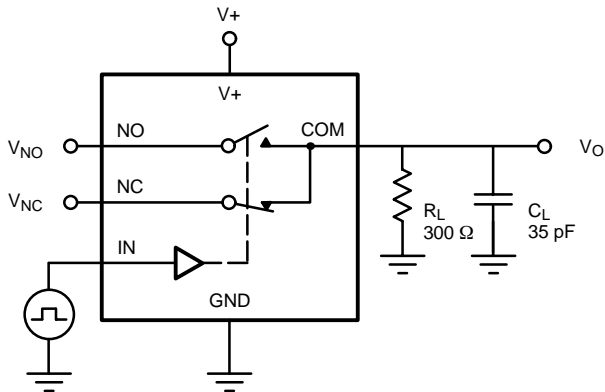
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

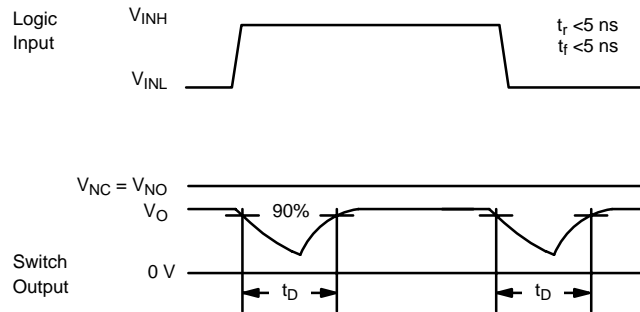
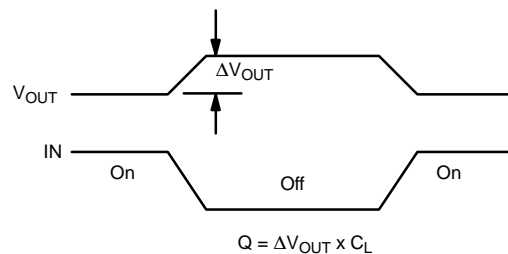
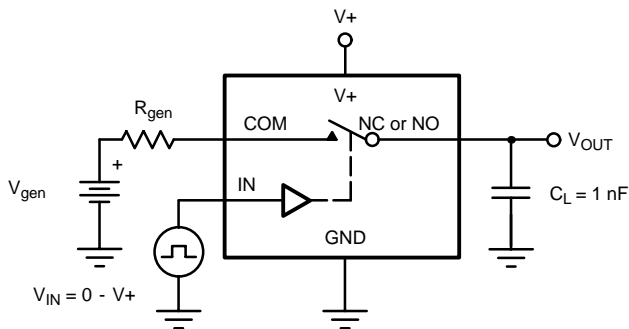


FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

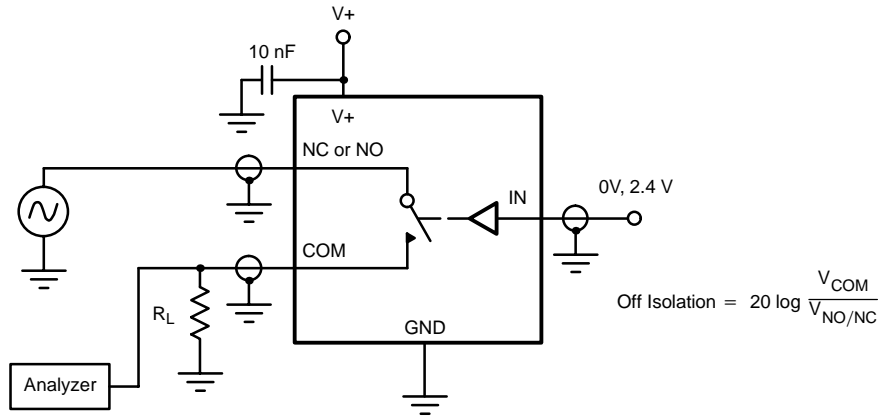


FIGURE 4. Off-Isolation

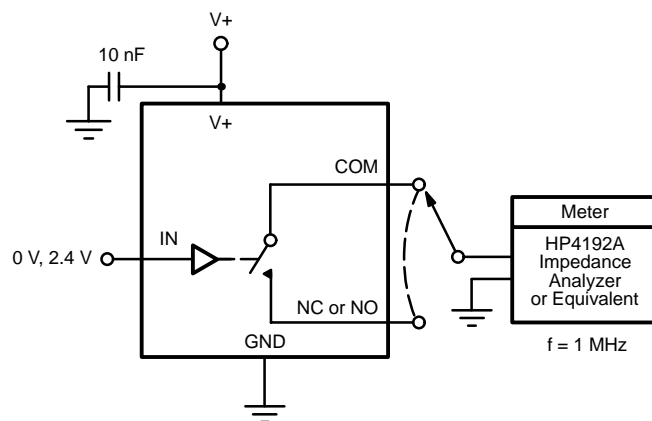


FIGURE 5. Channel Off/On Capacitance