



New Product

DG2032

Vishay Siliconix

High-Bandwidth, Low Voltage, Dual SPDT Analog Switch

FEATURES

- Single Supply (1.8 V to 5.5 V)
- Low On-Resistance - r_{ON} : 2.4 Ω
- Crosstalk and Off Isolation: -81 dB @ 1 MHz
- QFN-12 (3 x 3 mm) Package

BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- Low-Voltage Logic Compatible
- High Bandwidth

APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Low-Voltage Data Acquisition
- ATE

DESCRIPTION

The DG2032 is a monolithic CMOS dual single-pole/double-throw (SPDT) analog switch. It is specifically designed for low-voltage, high bandwidth applications.

The DG2032's on-resistance (3 Ω @ 2.7 V), matching and flatness are guaranteed over the entire analog voltage range. Wide dynamic performance is achieved with better than -80 dB for both cross-talk and off-isolation at 1 MHz.

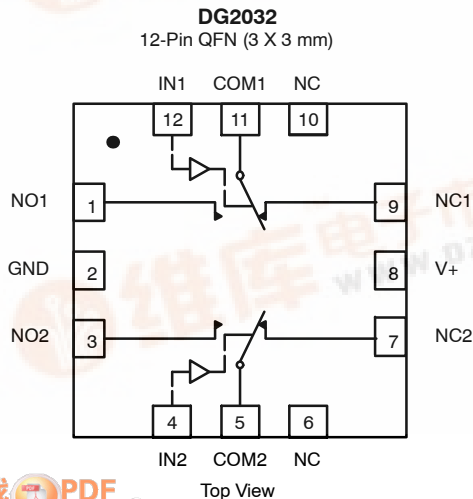
Both SPDT's operate with independent control logic, conduct equally well in both directions and block signals up to the

power supply level when off. Break-before-make is guaranteed.

With fast switching speeds, low on-resistance, high bandwidth, and low charge injection, the DG2032 is ideally suited for audio and video switching with high linearity.

Built on Vishay Siliconix's low voltage CMOS technology, the DG2032 contains an epitaxial layer which prevents latch-up.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	12-Pin QFN (3 x 3 mm)	DG2032DN





ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±50 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	±200 mA
Storage Temperature (D Suffix)	-65 to 150°C
Power Dissipation (Packages) ^b		
12-Pin QFN (3 x 3) ^c	1295 mW
Package Solder Reflow Conditions ^d		
12-Pin QFN (3 x 3)	240°C

Notes:

- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 16.2 mW/°C above 70°C
- Manual soldering with an iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V _{IN} = 0.4 or 2.0 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^b	Typ ^c	Max ^b	
Analog Switch							
Analog Signal Range ^d	V _{NO} , V _{NC} , V _{COM}		Full	0		V+	V
On-Resistance	r _{ON}	V+ = 2.7 V, V _{COM} = 0.2 V/1.5 V I _{NO} , I _{NC} = 10 mA	Room Full		3.0	5 6.5	Ω
r _{ON} Flatness	r _{ON} Flatness	V+ = 2.7 V V _{COM} = 0 to V+, I _{NO} , I _{NC} = 10 mA	Room			1.6	
r _{ON} Match Between Channels	Δr _{ON}		Room			0.4	
Switch Off Leakage Current	I _{NO(off)} , I _{NC(off)}	V+ = 3.3 V, V _{NO} , V _{NC} = 0.3 V/3 V V _{COM} = 3 V/0.3 V	Room Full	-1 -10	0.01	1 10	nA
	I _{COM(off)}		Room Full	-1 -10	0.01	1 10	
Channel-On Leakage Current	I _{COM(on)}	V+ = 3.3 V, V _{NO} , V _{NC} = V _{COM} = 0.3 V/3 V	Room Full	-1 -10	0.01	1 10	
Digital Control							
Input High Voltage	V _{INH}		Full	2.0			V
Input Low Voltage	V _{INL}		Full			0.4	
Input Capacitance	C _{in}		Full		5		pF
Input Current	I _{INL} or I _{INH}	V _{IN} = 0 or V+	Full	1		1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _{NO} or V _{NC} = 2.0 V, R _L = 50 Ω, C _L = 35 pF	Room Full		28	53 59	ns
Turn-Off Time	t _{OFF}		Room Full		13	38 38	
Break-Before-Make Time	t _d	V _{NO} or V _{NC} = 2.0 V, R _L = 50 Ω, C _L = 35 pF	Full	1			
Charge Injection ^d	Q _{INJ}	C _L = 1 nF, V _{GEN} = 0 V, R _{GEN} = 0 Ω	Room		38		pC
Off-Isolation ^d	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-78		dB
Crosstalk ^d	X _{TALK}		Room		-82		
No, Nc Off Capacitance ^d	C _{NO(off)}	V _{IN} = 0 or V+, f = 1 MHz	Room		15		pF
	C _{NC(off)}		Room		15		
Channel-On Capacitance ^d	C _{NO(on)}		Room		49		
	C _{NC(on)}		Room		45		
Power Supply							
Power Supply Current	I+	V _{IN} = 0 or V+	Full		0.01	1.0	μA

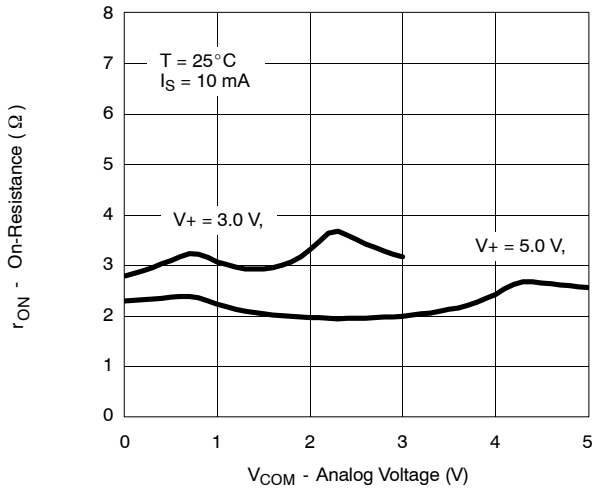
Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, nor subjected to production test.
- V_{IN} = input voltage to perform proper function.

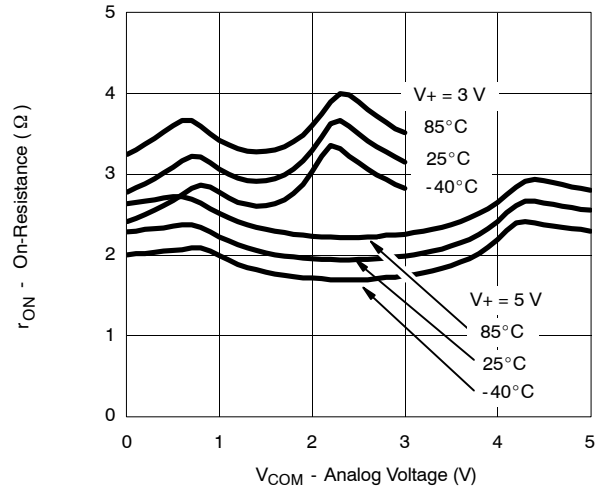


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

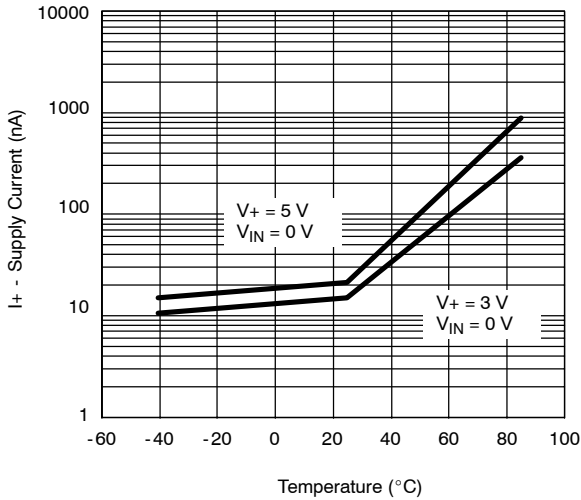
r_{ON} vs. V_{COM} and Supply Voltage



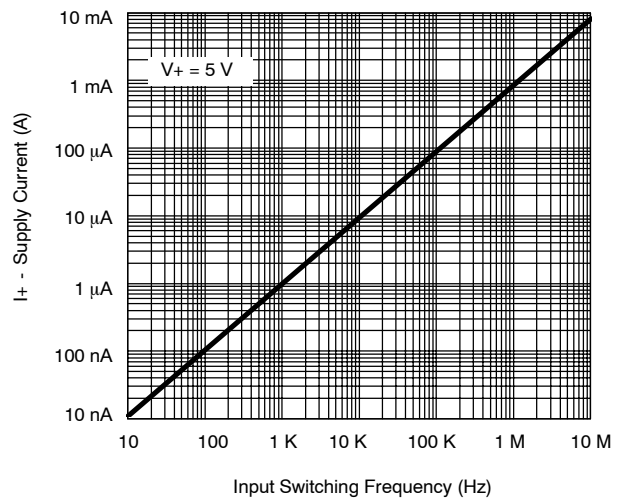
r_{ON} vs. Analog Voltage and Temperature



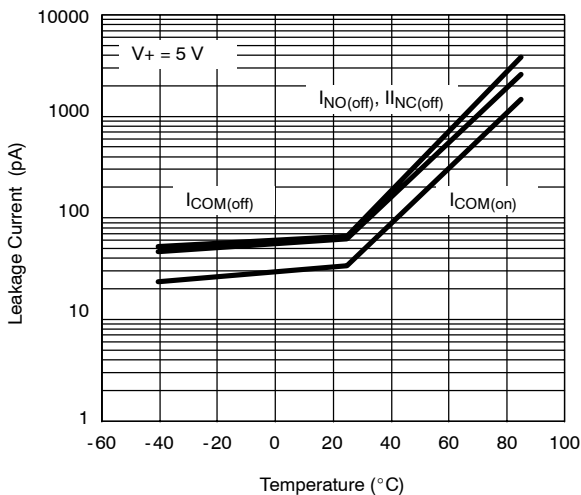
Supply Current vs. Temperature



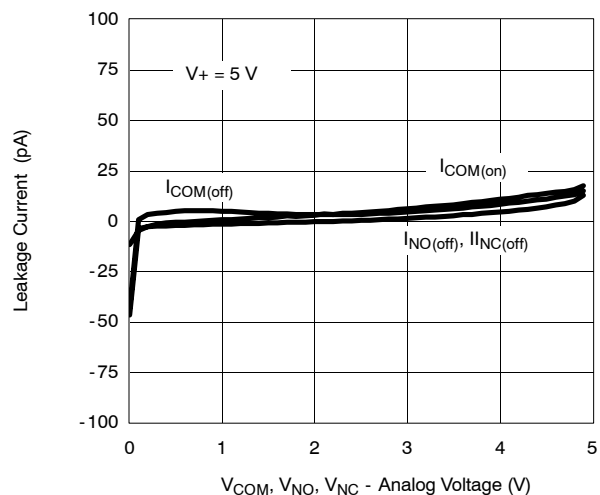
Supply Current vs. Input Switching Frequency



Leakage Current vs. Temperature

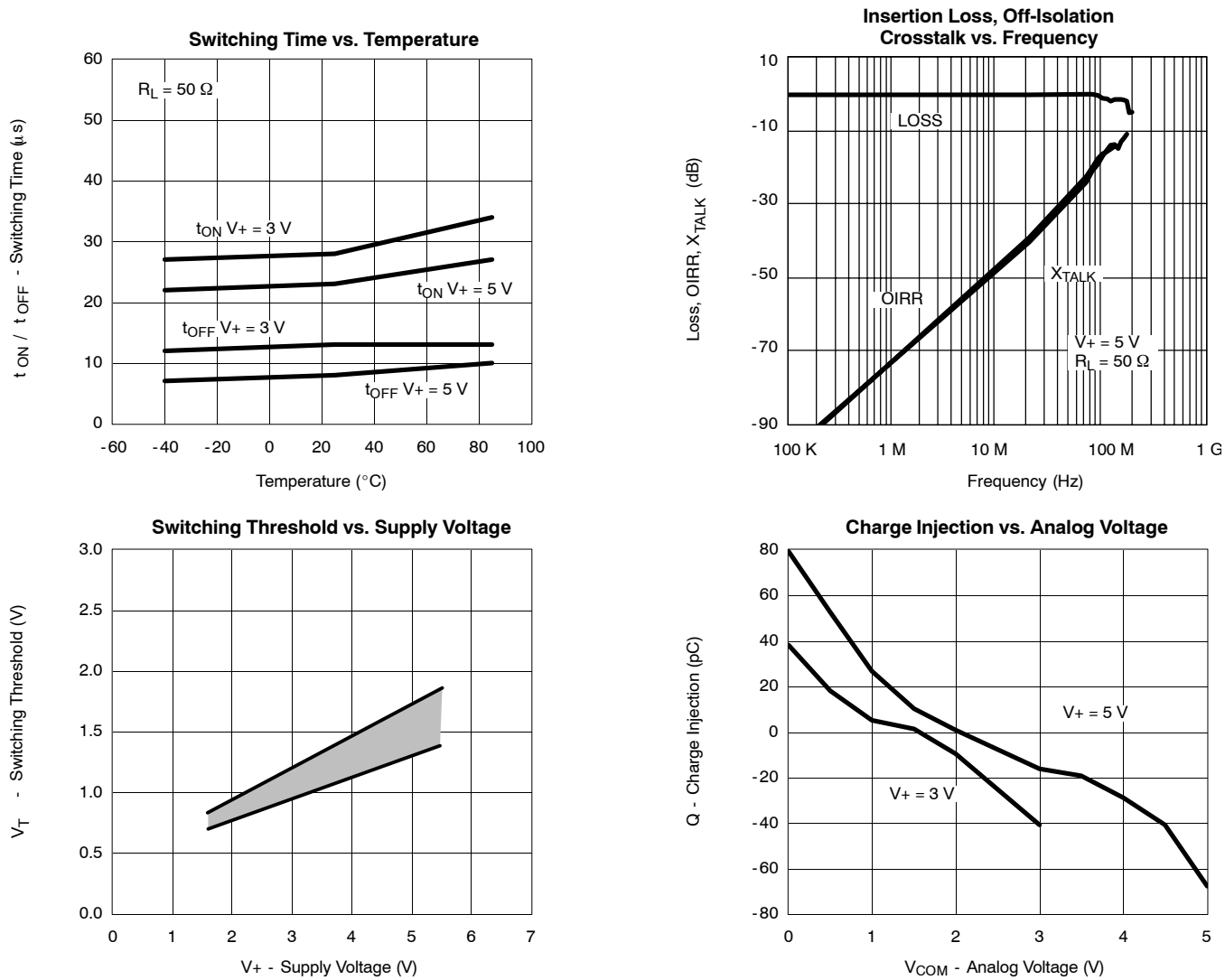


Leakage vs. Analog Voltage

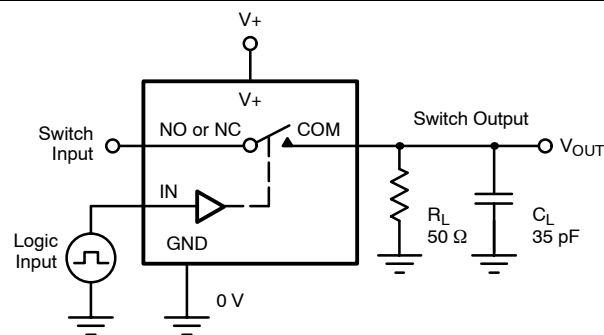




TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

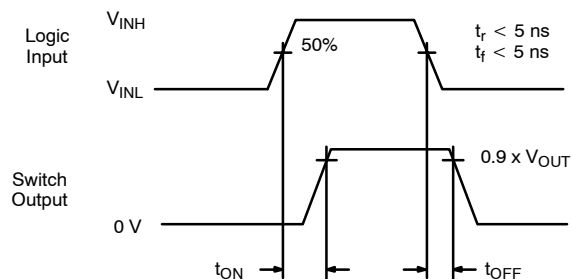


TEST CIRCUITS



C_L (includes fixture and stray capacitance)

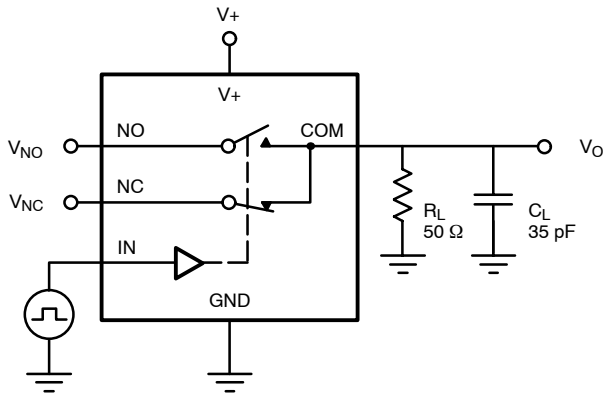
$$V_{OUT} = V_{COM} \left(\frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On
 Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

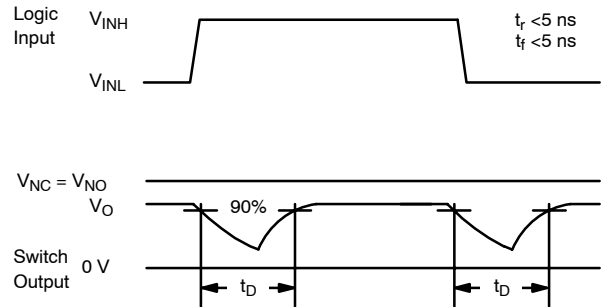
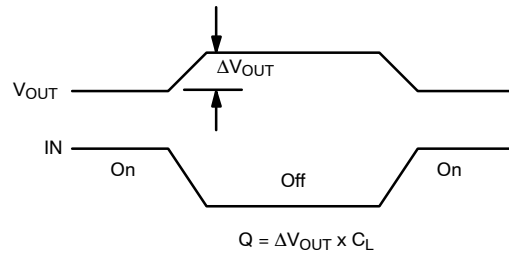
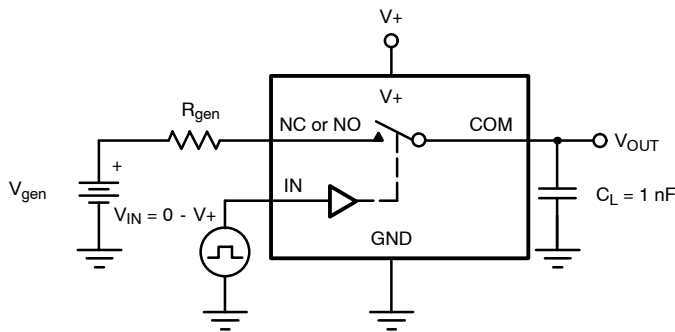


FIGURE 5. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 2. Charge Injection

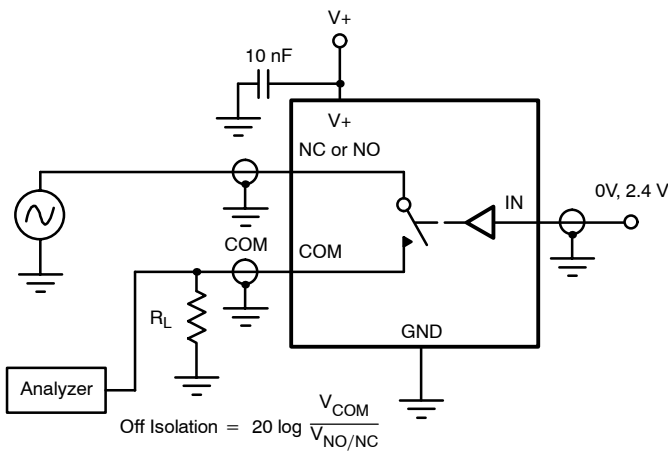


FIGURE 3. Off-Isolation

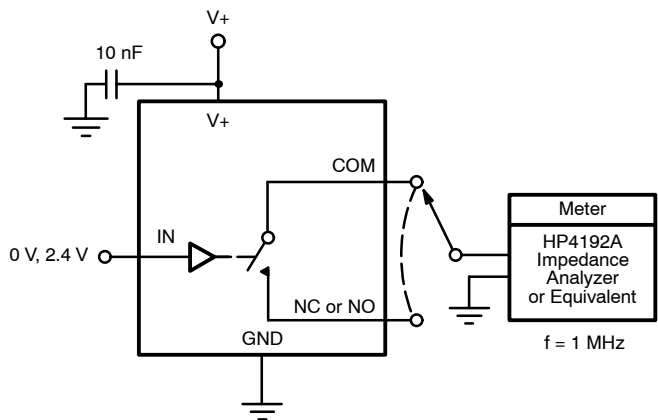


FIGURE 4. Channel Off/On Capacitance