Precision Monolithic Quad SPST Low-Voltage CMOS Analog Switches

FEATURES

- 2.7- thru 12-V Single Supply or ±3- thru ±6-Dual Supply
- On-Resistance—$r_{DS(on)}$: 17 Ω
- Fast Switching—t_{ON}: 19 ns
  —t_{OFF}: 12 ns
- TTL, CMOS Compatible
- Low Leakage: 0.25 nA
- 2000-V ESD Protection

BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- Precision Automatic Test Equipment
- Precision Data Acquisition
- Communication Systems
- Battery Powered Systems
- Computer Peripherals
- SDSL, DSLAM
- Audio and Video Signal Routing

DESCRIPTION

The DG411L/412L/413L are low voltage pin-for-pin compatible companion devices to the industry standard DG411/412/413 with improved performance

Using BiCMOS wafer fabrication technology allows the DG411L/412L/413L to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ±3 to ±6 V.

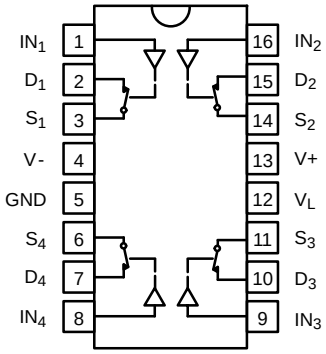
Combining high speed (t_{ON}: 19 ns), flat $r_{DS(on)}$ over the analog signal range (5 Ω), minimal insertion lose (-3 dB at 280 MHz), and excellent crosstalk and off-isolation performance (-50 dB at 50 MHz), the DG411L/412L/413L are ideally suited for audio and video signal switching.

The DG411L and DG412L respond to opposite control logic as shown in the Truth Table. The DG413L has two normally open and two normally closed switches.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG411L/412L

Dual-In-Line, TSSOP and SOIC



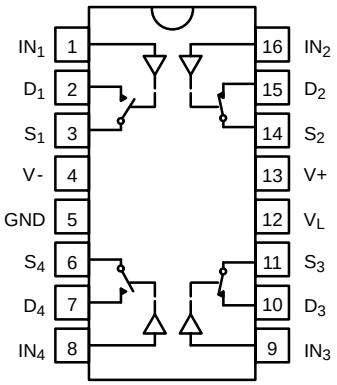
Top View

TRUTH TABLE		
Logic	**DG411L**	**DG412L**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG413L
Dual-In-Line, TSSOP and SOIC



Top View

TRUTH TABLE		
Logic	**SW_1, SW_4**	**SW_2, SW_3**
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
DG411L/412L		
-40 to 85°C	16-Pin Narrow SOIC	DG411LDY
		DG412LDY
	16-Pin TSSOP	DG411LDQ
		DG412LDQ
-55 to 125°C	16-Pin CerDIP	DG411LAK, DG411LAK/883
		DG412LAK, DG412LAK/883
	LCC-20	DG411LAZ/883
		DG412LAZ/883
DG413L		
-40 to 85°C	16-Pin Narrow SOIC	DG413LDY
	16-Pin TSSOP	DG413LDQ
-55 to 125°C	16-Pin CerDIP	DG413LAK, DG413LAK/883
	LCC-20	DG413LAZ/883

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... -0.3 TO 13 V

GND to V- ..... 7 V

V_L ..... (GND -0.3 V) to (V+) +0.3 V

I_N[a], V_S, V_D ..... -0.3 to (V+ +0.3 V) or 30 mA, whichever occurs first

Continuous Current (Any Terminal) ..... 30 mA

Peak Current, S or D (Pulsed 1 ms, 10% Duty Cycle) ..... 100 mA

Storage Temperature (DQ, DY Suffix) ..... -65 to 125°C
(AK Suffix) ..... -65 to 150°C

Power Dissipation (Package)[b]
16-Pin TSSOP[c] ..... 450 mW
16-Pin SOIC[d] ..... 650 mW
16-Pin CerDIP[e] ..... 900 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 7 mW/°C above 75°C
d. Derate 7.6 mW/°C above 75°C
e. Derate 12 mW/°C above 75°C

Document Number: 71397
S-03251—Rev. D, 17-Mar-03

SPECIFICATIONS[a] (SINGLE SUPPLY 12 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 12 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 125°C Min[d]	A Suffix Limits -55 to 125°C Max[d]	D Suffix Limits -40 to 85°C Min[d]	D Suffix Limits -40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 10.8 V, V- = 0 V I_S = 10 mA, V_D = 2/9 V	Room Full	20		30 45		30 40	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_D = 1/11 V, V_S = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 11/1 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.01	-1.5	1.5	-1	1	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V	Full		-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 5 V See Figure 2	Room Full	20		50 70		50 60	ns
Turn-Off Time	t_{OFF}		Room Full	12		30 48		30 40	
Break-Before-Make Time Delay	t_D	DG413L Only, V_S = 5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	71					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	95					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	5					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	6					
Channel On Capacitance[e]	$C_{D(on)}$		Room	15					
Power Supplies									
Positive Supply Current	I+	V_{IN} = 0 or 5 V	Room Full	0.02		1 7.5		1 5	µA
Negative Supply Current	I-		Room Full	-0.002	-1 -7.5		-1 -5		
Logic Supply Current	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current	I_{GND}		Room Full	-0.002	-1 -7.5		-1 -5		

SPECIFICATIONS[a] (DUAL SUPPLY ±5 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = -5 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 150°C Min[d]	A Suffix Limits -55 to 150°C Max[d]	D Suffix Limits -40 to 85°C Min[d]	D Suffix Limits -40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		-5	5	-5	5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 5 V, V- = -5 V I_S = 10 mA, V_D = ±3.5 V	Room Full	20		33 45		33 40	Ω
Switch Off Leakage Current[g]	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = ±4.5 V, V_S = ∓4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current[g]	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V V_S = V_D = ±4.5 V	Room Full		-1 -15	1 15	-1 -10	1 10	

SPECIFICATIONS[a] (DUAL SUPPLY ±5 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = -5 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 150°C Min[d]	A Suffix Limits -55 to 150°C Max[d]	D Suffix Limits -40 to 85°C Min[d]	D Suffix Limits -40 to 85°C Max[d]	Unit
Digital Control									
Input Current, V_{IN} Low[e]	I_{IL}	V_{IN} Under Test = 0.8 V	Full	0.05	-1.5	1.5	-1	1	µA
Input Current, V_{IN} High[e]	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.05	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ±3.5 V See Figure 2	Room Full	21		50 75		50 60	ns
Turn-Off Time[e]	t_{OFF}		Room Full	16		35 50		35 40	
Break-Before-Make Time Delay[e]	t_D	DG413L Only, V_S = 3.5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	5					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	9					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	9					
Channel On Capacitance[e]	$C_{D(on)}$		Room	20					
Power Supplies									
Positive Supply Current[e]	I+	V_{IN} = 0 or 5 V	Room Full	0.03		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Full	-0.002	-1 -7.5		-1 -5		
Logic Supply Current[e]	I_L		Room Full	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Full	-0.002	-1 -7.5		-1 -5		

SPECIFICATIONS[a] (SINGLE SUPPLY 5 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 150°C Min[d]	A Suffix Limits -55 to 150°C Max[d]	D Suffix Limits -40 to 85°C Min[d]	D Suffix Limits -40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full			5		5	V
Drain-Source On-Resistance[e]	$r_{DS(on)}$	V+ = 4.5 V, I_S = 5 mA V_D = 1 V, 3.5 V	Room Full	35		50 88		50 75	Ω
Dynamic Characteristics									
Turn-On Time[e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 3.5 V, See Figure 2	Room Hot	27		50 90		50 60	ns
Turn-Off Time[e]	t_{OFF}		Room Hot	15		30 55		30 40	
Break-Before-Make Time Delay[e]	t_D	DG413L Only, V_S = 3.5 V, R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	0.5					pC

SPECIFICATIONS[a] (SINGLE SUPPLY 5 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 5 V, V- = 0 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 150°C Min[d]	A Suffix Limits -55 to 150°C Max[d]	D Suffix Limits -40 to 85°C Min[d]	D Suffix Limits -40 to 85°C Max[d]	Unit
Power Supplies									
Positive Supply Current[e]	I+	V_{IN} = 0 or 5 V	Room Hot	0.02		1 7.5		1 5	µA
Negative Supply Current[e]	I-		Room Hot	-0.002	-1 -7.5		-1 -5		
Logic Supply Current[e]	I_L		Room Hot	0.002		1 7.5		1 5	
Ground Current[e]	I_{GND}		Room Hot	-0.002	-1 -7.5		-1 -5		

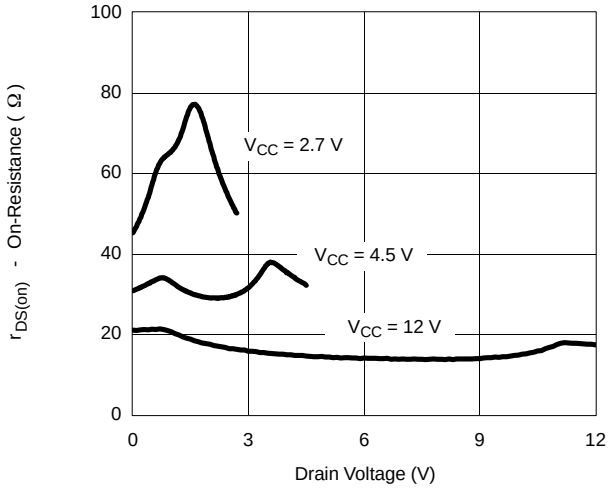
SPECIFICATIONS[a] (SINGLE SUPPLY 3 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 3 V, V- = 0 V V_L = 3 V, V_{IN} = 0.4 V[f]	Temp[b]	Typ[c]	A Suffix Limits -55 to 150°C Min[d]	A Suffix Limits -55 to 150°C Max[d]	Limits -40 to 85°C Min[d]	Limits -40 to 85°C Max[d]	Unit
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		0	3	0	3	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 2.7 V, V- = 0 V I_S = 5 mA, V_D = 0.5, 2.2 V	Room Full	65		80 115		80 100	Ω
Switch Off Leakage Current[g]	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 1, 2 V, V_S = 2, 1 V	Room Full		-1 -15	1 15	-1 -10	1 10	nA
	$I_{D(off)}$		Room Full		-1 -15	1 15	-1 -10	1 10	
Channel On Leakage Current[g]	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V V_S = V_D = 1, 2 V	Room Full		-1 -15	1 15	-1 -10	1 10	
Digital Control									
Input Current, V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.4 V	Full	0.005	-1.5	1.5	-1	1	µA
Input Current, V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V	Full	0.005	-1.5	1.5	-1	1	
Dynamic Characteristics									
Turn-On Time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 1.5 V See Figure 2	Room Full	50		85 150		85 110	ns
Turn-Off Time	t_{OFF}		Room Full	30		60 100		60 85	
Break-Before-Make Time Delay	t_D	DG413L Only, V_S = 1.5 V R_L = 300 Ω, C_L = 35 pF	Room	6					
Charge Injection[e]	Q	V_g = 0 V, R_g = 0 Ω, C_L = 10 nF	Room	1					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room	68					dB
Channel-to-Channel Crosstalk[e]	X_{TALK}		Room	85					
Source Off Capacitance[e]	$C_{S(off)}$	f = 1 MHz	Room	6					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	6					
Channel On Capacitance[e]	$C_{D(on)}$		Room	20					

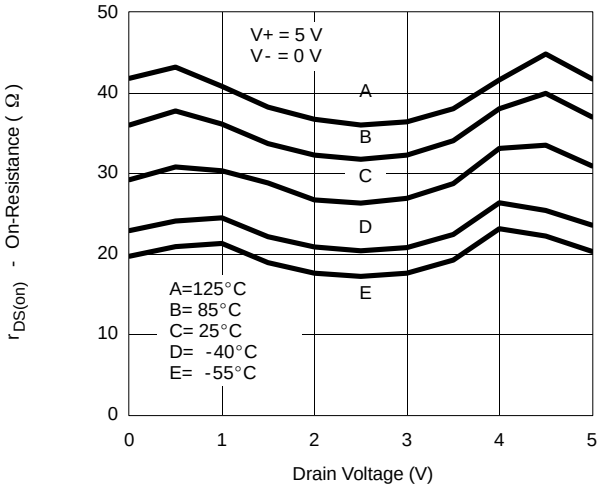
Notes:
a. Refer to PROCESS OPTION FLOWCHART.
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. Leakage parameters are guaranteed by worst case test conditions and not subject to test.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

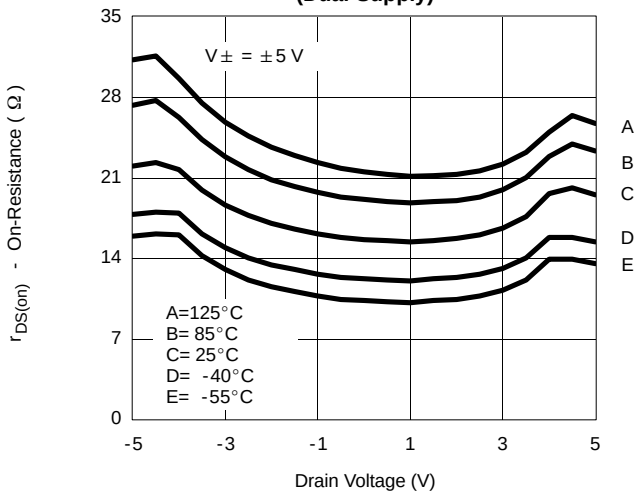
$r_{DS(on)}$ vs. Drain Voltage (Single Supply)



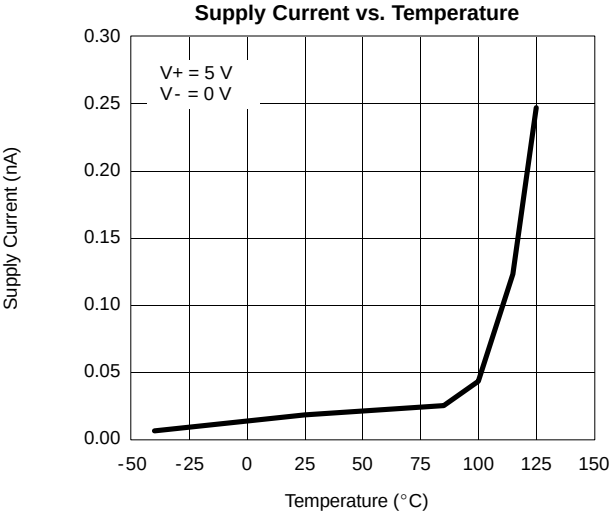
$r_{DS(on)}$ vs. Drain Voltage and Temperature (Single Supply)



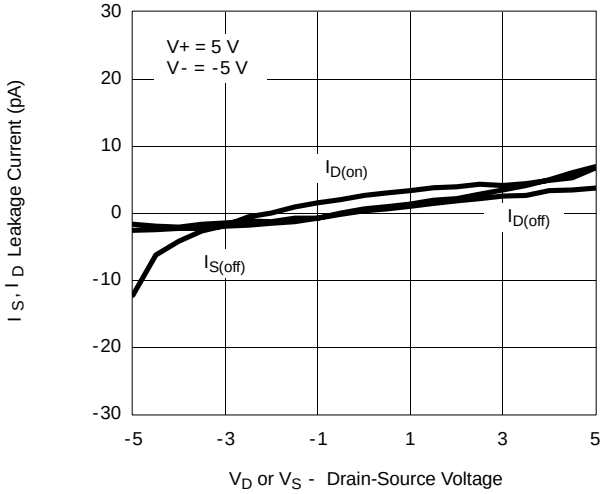
$r_{DS(on)}$ vs. Drain Voltage and Temperature (Dual Supply)



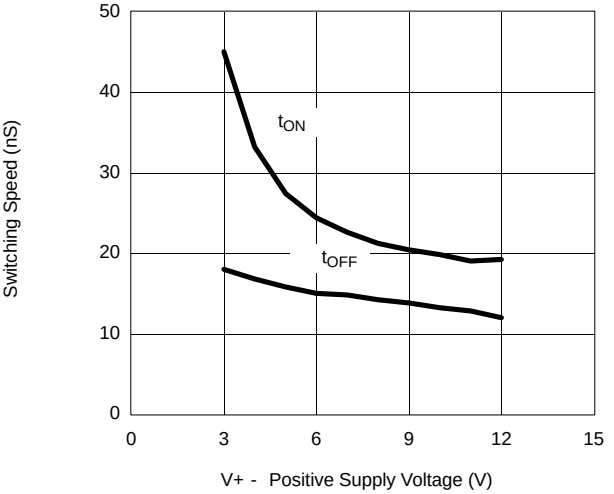
Supply Current vs. Temperature



Leakage Current vs. Analog Voltage (Dual Supply)



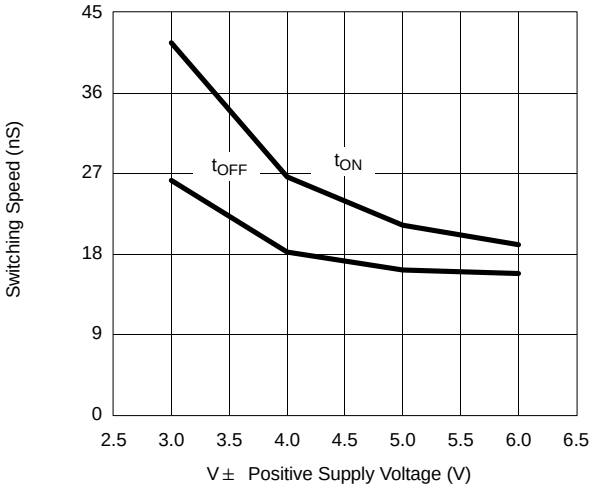
Switching Time vs. Single Supply



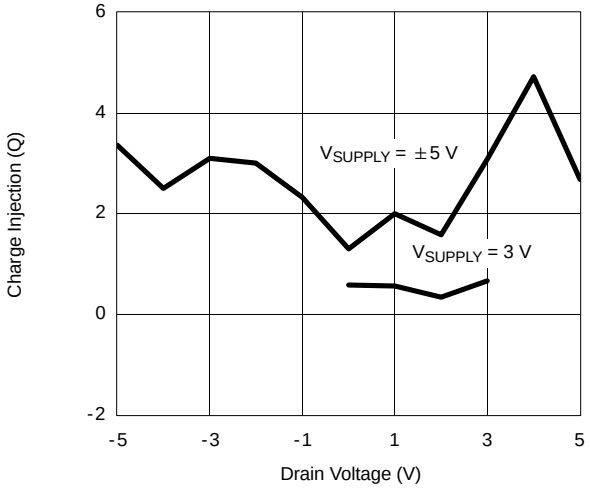
Document Number: 71397
S-03251—Rev. D, 17-Mar-03

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

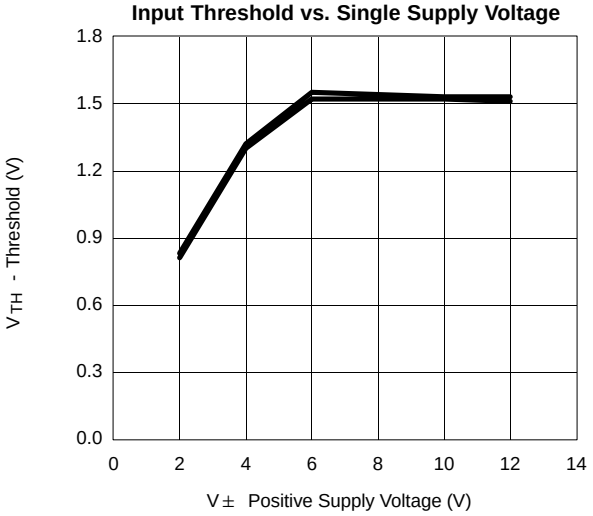
Switching Time vs. Dual Supply



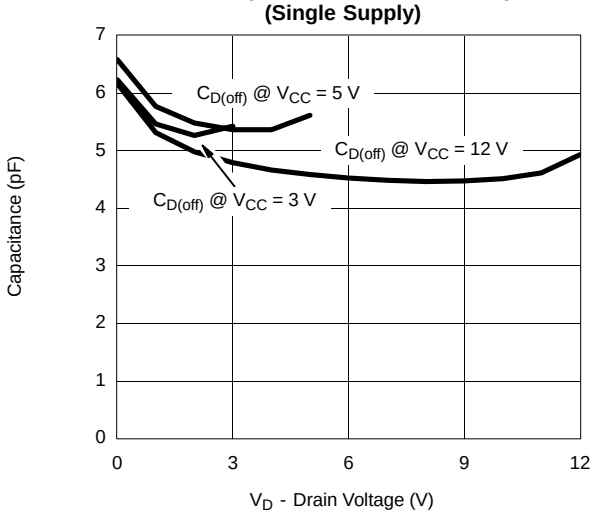
Charge Injection vs. Drain Voltage



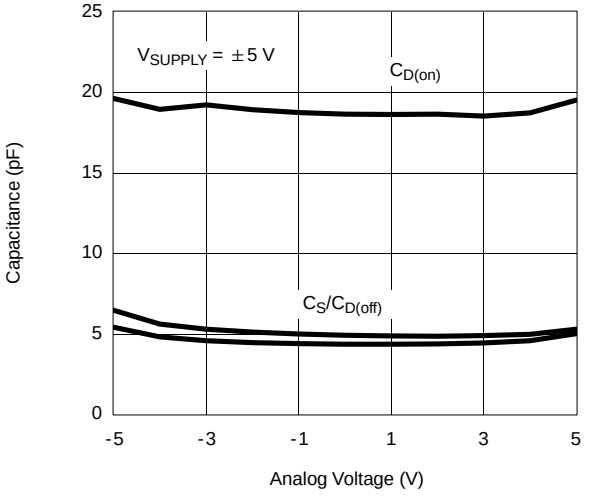
Input Threshold vs. Single Supply Voltage



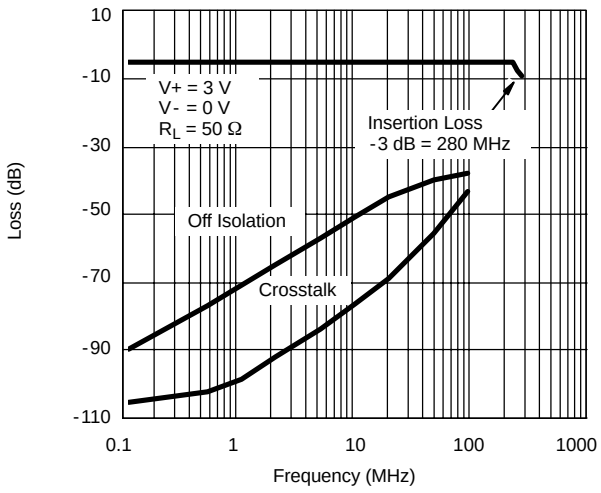
Drain Capacitance vs. Drain Voltage (Single Supply)



Capacitance vs. Analog Signal (Dual Supply)



Insertion Loss, Off Isolation and Crosstalk vs. Frequency (Single Supply)



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

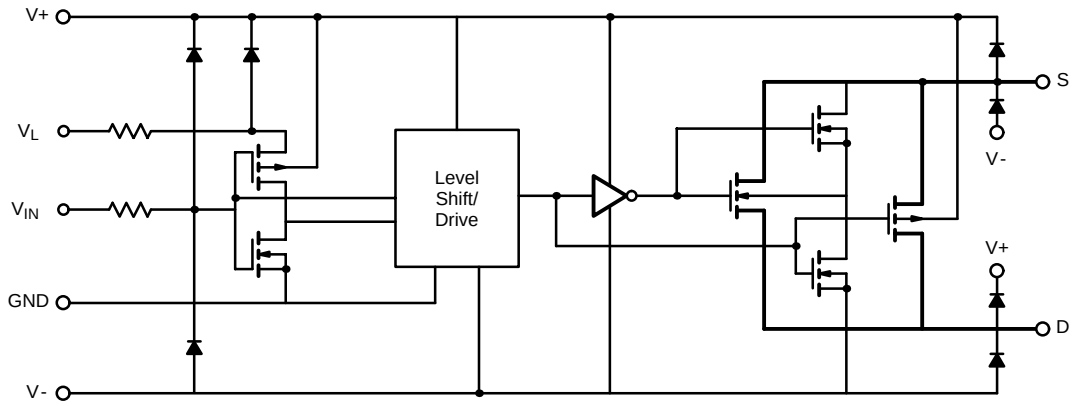
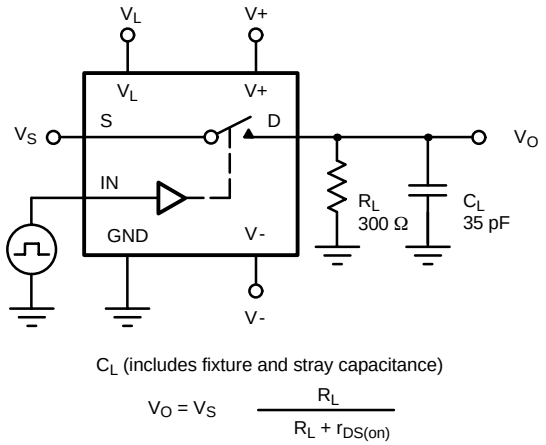


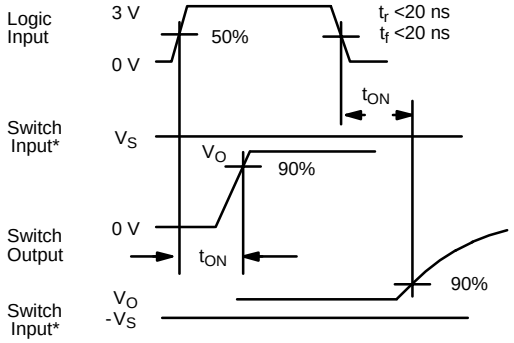
FIGURE 1.

TEST CIRCUITS



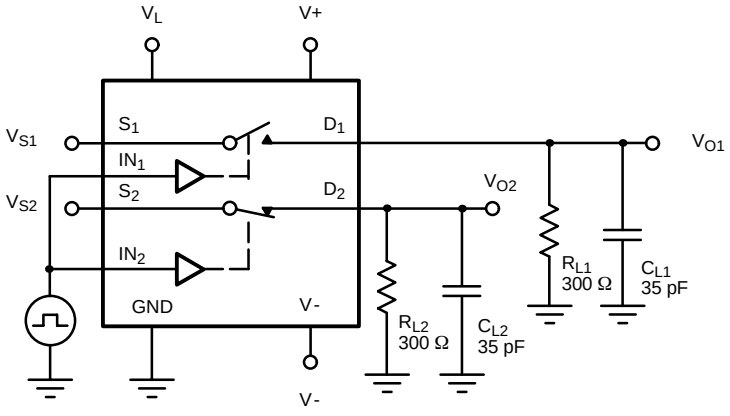
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

FIGURE 2. Switching Time



C_L (includes fixture and stray capacitance)

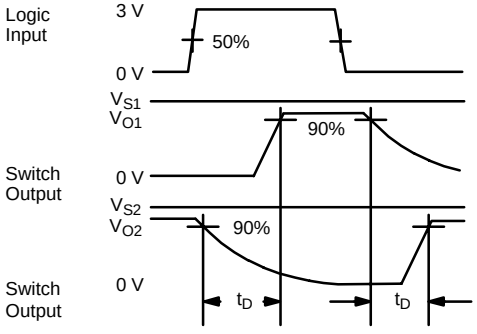
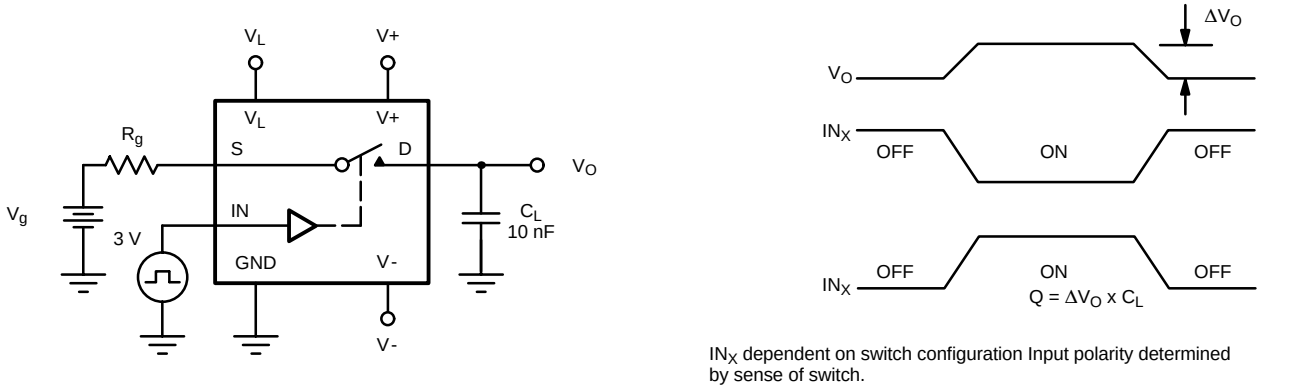


FIGURE 3. Break-Before-Make (DG413L)

TEST CIRCUITS



IN_X dependent on switch configuration Input polarity determined by sense of switch.

FIGURE 4. Charge Injection

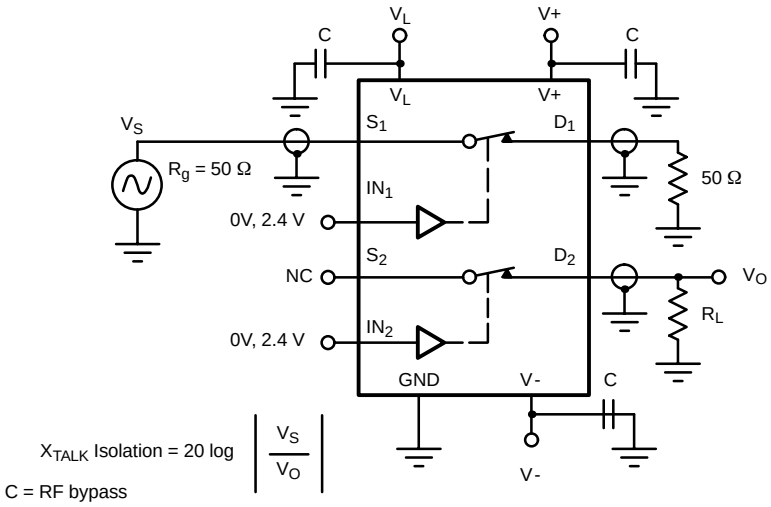


FIGURE 5. Crosstalk

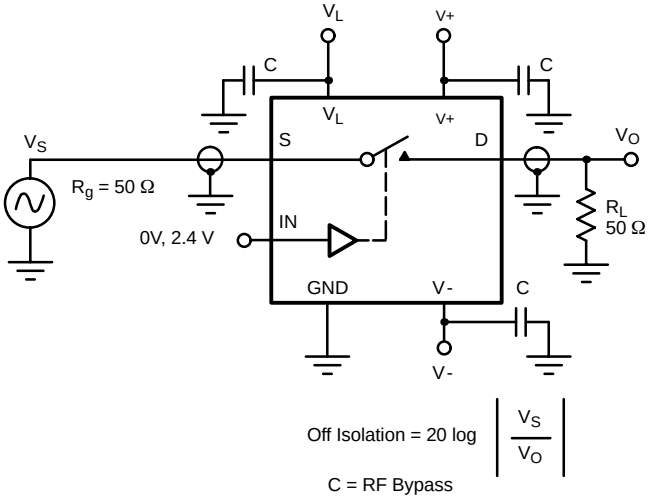


FIGURE 6. Off Isolation

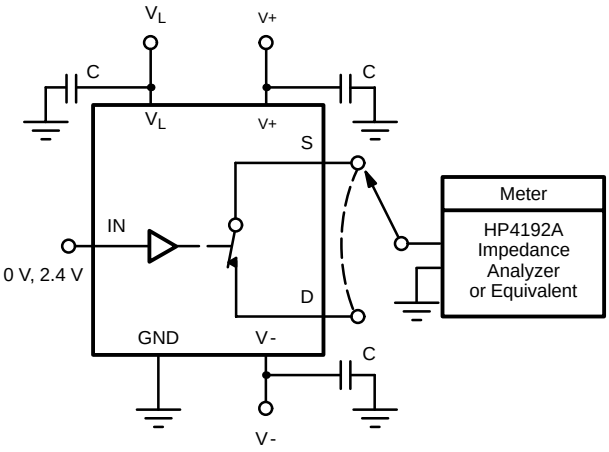


FIGURE 7. Source/Drain Capacitances

Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay's terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.