Monolithic General-Purpose CMOS Analog Switch

FEATURES

- ±15-V Input Range
- On-Resistance: <50 Ω
- Break-Before-Make Switching
- TTL and CMOS Compatible

BENEFITS

- Improved Signal Headroom
- Reduced Switching Errors
- No Shorting of Inputs
- Simple Interfacing

APPLICATIONS

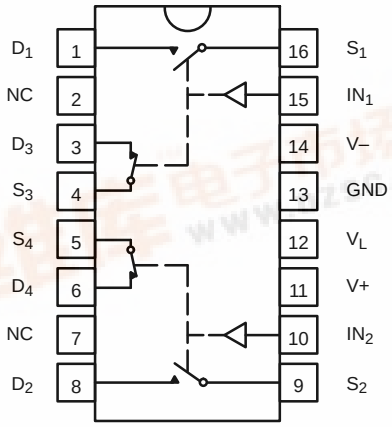
- Audio Switching
- Instrumentation
- Battery Powered Systems

DESCRIPTION

The DG5043 solid state analog switch is recommended for general purpose applications in instrumentation, and process control. Built on the Vishay Siliconix PLUS-40 high voltage CMOS process, this device provides ease-of-use and performance advantages to the system designer. Key performance features of the DG5043 are 1-µs switching, low power supply requirements, and break-before-make switching. Each switch conducts equally well in either direction, when on, and blocks up to 30 V peak-to-peak when off. Off leakage current is 1-nA maximum. An epitaxial layer prevents latch up. For new designs, DG403 is recommended.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

Dual-In-Line



Top View

TRUTH TABLE		
Logic	SW_1, SW_2	SW_3, SW_4
0	OFF	ON
1	ON	OFF

Logic “0” = ≤ 0.8 V
Logic “1” = ≥ 2 V

ORDERING INFORMATION		
Temp Range	Package	Part Number
0 to 70°C	16-Pin Plastic DIP	DG5043CJ

ABSOLUTE MAXIMUM RATINGS

V+ to V– ..... 44 V
GND to V– ..... 25 V
V_L ..... (GND – 0.3 V) to 44 V
Digital Inputs[a] V_S, V_D ..... (V–) –2 V to (V+ plus 2 V)
or 30 mA, whichever occurs first
Current (Any Terminal) Continuous ..... 30 mA
Current, S or D (Pulsed 1 ms 10% duty) ..... 100 mA
Storage Temperature ..... –65 to 125°C

Power Dissipation (Package)b
16-Pin Plastic DIP[c] ..... 470 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C

SPECIFICATIONS

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V– = –15 V V_L = 5 V, V_{IN} = 2 V, 0.8 V[e]	Temp[a]	C Suffix 0 to 70°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	VANALOG		Full	–15		15	V
Drain-Source On-Resistance	$r_{DS(on)}$	I_S = –10 mA, V_D = ±10 V	Room Full			50 75	Ω
Switch Off Leakage Current	$I_{S(off)}$	V_S = V_D = 14 V	Room Full	–1 –100		1 100	nA
		V_S = V_D = –14 V	Room Full	–1 –100		1 100	
Channel On Leakage Current	$I_{D(on)}$	V_S = V_D = 14 V	Room Full			2 200	
		V_S = V_D = –14 V	Room Full	–2 –200			
Digital Control							
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V	Full	–1		1	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2 V	Full	–1		1	
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_S = ±10 V, R_L = 1 kΩ, C_L = 35 pF See Figure 1	Room			1200	ns
Turn-Off Time	t_{OFF}		Room			700	
Charge Injection[d]	Q	C_L = 10 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		30		pC
Off Isolation[d]	OIRR	R_L = 75 Ω, C_L = 5 pF, f = 1 MHz	Room		75		dB
Crosstalk (Channel-to-Channel)[d]	X_{TALK}	R_L = 75 Ω, V_S = 2 V_{P-P}, f = 1 MHz	Room		89		
Source Off Capacitance	$C_{S(off)}$	V_D = V_S = 0 V, f = 1 MHz	Room		15		pF
Drain Off Capacitance[d]	$C_{D(off)}$		Room		17		
Channel On Capacitance[d]	$C_{D(on)}$		Room		45		
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 or 2.4 V	Full			300	µA
Negative Supply Current	I–		Full	–300			
Logic Supply Current	I_L	V_{IN} = 0 or 2.4 V	Full			300	
Ground Current	I_{GND}		Full	–300			

Notes:
a. Room = 25°C, Full = as determined by the operating temperature suffix.
b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guaranteed by design, not subject to production test.
e. V_{IN} = input voltage to perform proper function.

TEST CIRCUITS

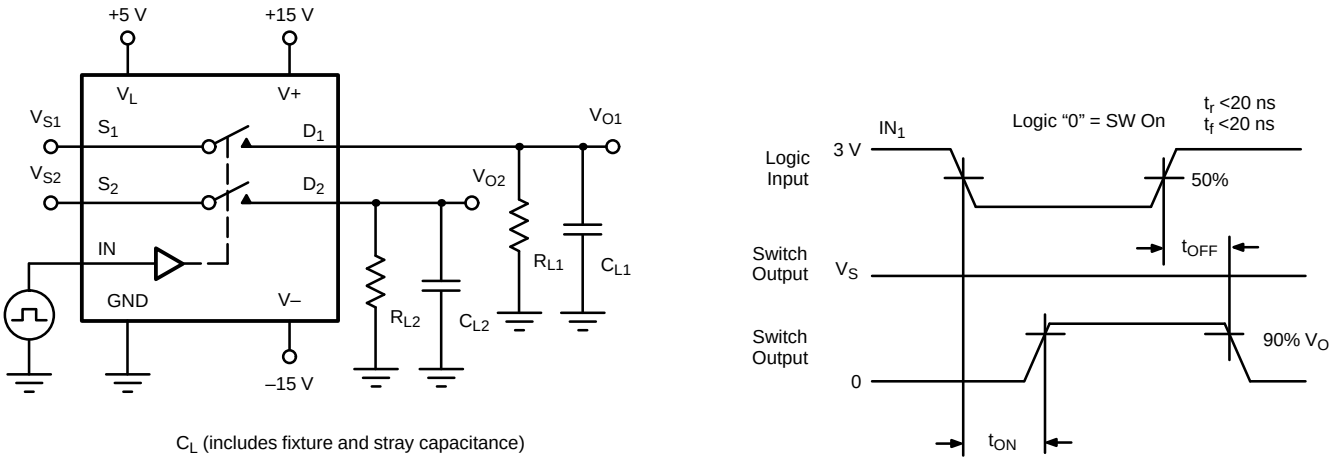


FIGURE 1. Switching Time

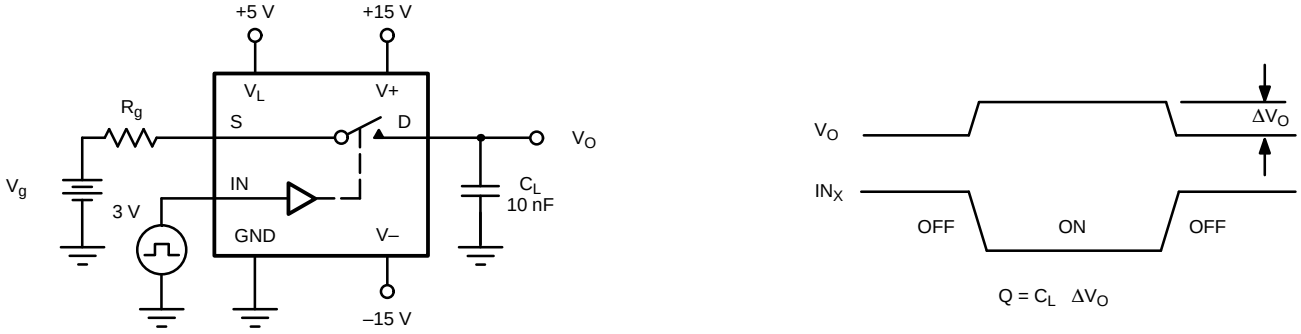


FIGURE 2. Charge Injection