



New Product

DG9432/9433/9434
Vishay Siliconix

Low-Voltage Dual SPST Analog Switch

FEATURES

- Wide Operation Voltage (+2.7 to +12 V)
- Low Charge Injection - Q_{INJ} : 1 pC
- Low Power Consumption
- TTL/CMOS Logic Compatible Over The Full Operating Voltage range
- Available in MSOP-8 and SOT23-8

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

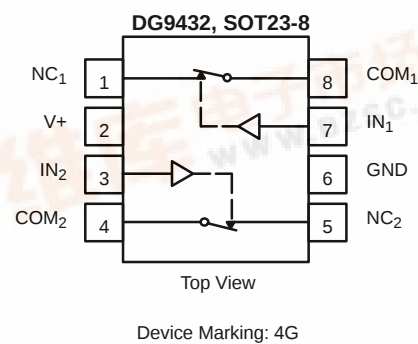
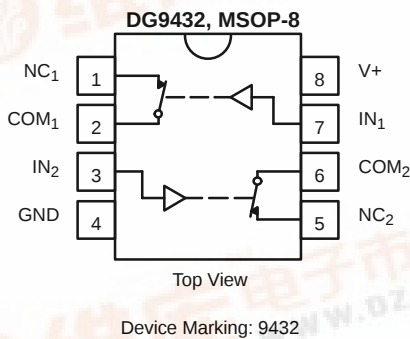
DESCRIPTION

The DG9432/9433/9434 is a dual single-pole/single-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed (t_{ON} : 25 ns, t_{OFF} : 20 ns), the DG9432/9433/9434 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG9432/9433/9434 is built on Vishay Siliconix's low voltage BCD-15 process. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9432/9433/9434.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9432



TRUTH TABLE DG9432

Logic	Switch
0	On
1	Off



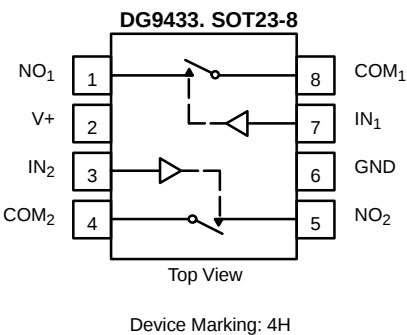
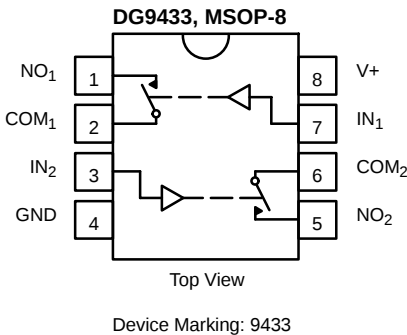
DG9432/9433/9434

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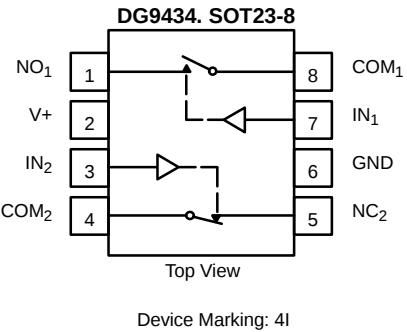
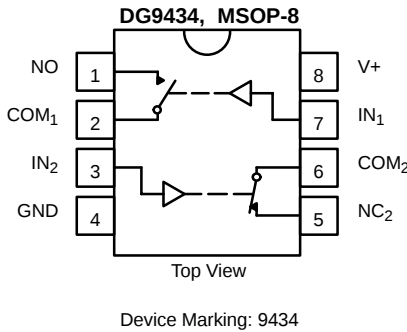
New Product



FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION—DG9433/DG9434



TRUTH TABLE DG9433	
Logic	Switch
0	Off
1	On



TRUTH TABLE DG9434		
Logic	Switch-1	Switch-2
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	MSOP-8	DG9432DQ
		DG9433DQ
		DG9434DQ
	SOT23-8	DG9432DS
		DG9433DS
		DG9434DS



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ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+	-0.3 to +13.5 V
IN, COM, NC, NO ^a	-0.3 to (V+ + 0.3 V)
Continuous Current (Any terminal)	±10 mA
Peak Current (Pulsed at 1ms, 10% duty cycle)	±20 mA
Storage Temperature (D Suffix)	-65 to 150°C

Power Dissipation (Packages)^b

MSOP-8 ^c	320 mW
SOT23-8 ^c	515 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75°C

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified $V^+ = 3.3\text{ V}$, $\pm 10\%$, $V_{\text{IN}} = 0.4$ or 1.8 V^{e}	Temp ^a	Limits -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	V_{ANALOG}		Full	V -		V +	V
Drain-Source On-Resistance	$r_{(\text{on})}$	$V^+ = 2.7\text{ V}$, $I_{\text{COM}} = 1\text{ mA}$, $V_{\text{COM}} = 1.5\text{ V}$	Room Full		81	100 120	Ω
$r_{(\text{on})}$ Match ^d	$\Delta r_{(\text{on})}$		Room		0.4	3.0	
Digital Control							
Input, High Voltage	V_{INH}	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	V_{INL}		Full			0.4	
Input Current	I_{INH}			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	t_{OPEN}	$V^+ = 3\text{ V}$, $R_{\text{L}} = 300\text{ }\Omega$ $V_{\text{NO}} = V_{\text{NC}} = 1.5\text{ V}$ $C_{\text{L}} = 35\text{ pF}$, $V_{\text{IN}} = 0\text{ V}$, 3 V	Room Full	1			ns
Turn-OnTime ^d	t_{ON}		Room Full		60	80 100	
Turn-OffTime ^d	t_{OFF}		Room Full		14	25 35	
Charge Injection ^d	Q	$C_{\text{L}} = 1\text{ nF}$, $R_{\text{GEN}} = 0\text{ }\Omega$, $V_{\text{g}} = 0\text{ V}$	Room		0.16		pC
Off-Isolation ^d	OIRR	$C_{\text{L}} = 5\text{ pF}$, $R_{\text{L}} = 50\text{ }\Omega$, $f = 1\text{ MHz}$	Room		77		dB
		$C_{\text{L}} = 5\text{ pF}$, $R_{\text{L}} = 50\text{ }\Omega$, $f = 10\text{ MHz}$	Room		55		
Crosstalk ^d	X_{TALK}	$R_{\text{L}} = 50\text{ }\Omega$, $f = 1\text{ MHz}$, $V^+ = 2.5\text{ V}$	Room		98		
Source Off Capacitance ^d	$C_{\text{NC/NO(off)}}$	$f = 1\text{ MHz}$, $V_{\text{NC/NO}} = 0\text{ V}$	Room		7.5		pF
Drain Off Capacitance ^d	$C_{\text{COM(off)}}$	$f = 1\text{ MHz}$, $V_{\text{COM}} = 0\text{ V}$	Room		7.8		
Drain On Capacitance ^d	$C_{\text{COM(on)}}$		Room		22		
Supply Current	I_{+}	$V^+ = 3.3\text{ V}$, $V_{\text{IN}} = 0$ or V^+	Room	-1		-1	μA

Notes:

- Room = 25°C, Full = as determined by the operating suffix.
- Typical values are for design aid only, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guarantee by design, not subjected to production test.
- V_{IN} = input voltage to perform proper function.
- Guaranteed by 12-V leakage testing, not production tested.
- Applies for DG9434 only.

SPECIFICATIONS (V+ = 5 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10%, VIN = 0.4 or 1.8 V ^e	Temp ^a	Limits -40 to 85 °C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	VANALOG		Full	V-		V+	V
Drain-Source On-Resistance	r(on)	V+ = 4.5 V, ICOM = 1 mA, VCOM = 2.5 or 3.5 V	Room Full		39	60 70	Ω
rDS(on) Match	Δr(on)	V+ = 4.5 V, ICOM = 1 mA,VCOM = 3.5 V	Room		0.3	3.0	
Switch Off Leakage Current ^f	INC/NO(off)	V+ = 5 V, VCOM = 0.5 V, 4.5 V VNC/NO = 4.5 V, 0.5 V	Room Full	-1 -10	0.3	1 10	nA
	ICOM(off)		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current ^f	ICOM(on)		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	VINH	V+ Ranges 2.7 to 5 V	Full	1.8			V
Input, Low Voltage	VINL		Full			0.4	
Input Current	IINH			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	tOPEN	V+ = 5 V, RL = 300 Ω VNO = VNC = 3 V CL = 35 pF, VIN = 0 V, 5 V	Room Full	1			ns
Turn-OnTime	tON		Room Full		33	60 70	
Turn-OffTime	tOFF		Room Full		10	20 30	
Charge Injection ^d	Q	CL = 1 nF, RGEN = 0 Ω, Vg = 0 V	Room		0.56		pC
Off-Isolation ^d	OIRR	CL = 5 pF, RL = 50 Ω, f = 1 MHz	Room		76		dB
		CL = 5 pF, RL = 50 Ω, f = 10 MHz, V+ = 5 V	Room		54		
Crosstalk ^d	XTALK	RL = 50 Ω, f = 1 MHz, V+ = 5 V	Room		96		
Source Off Capacitance ^d	CNC/NO(off)	f = 1 MHz, VNO/NC = 0 V	Room		7.5		pF
Drain Off Capacitance ^d	CCOM(off)	f = 1 MHz, VCOM = 0 V	Room		7.8		
Drain On Capacitance ^d	CCOM(on)		Room		22		
Supply Current	I+	V+ = 5.5 V, VIN = 0 or V+	Room	-1		-1	μA

Notes:

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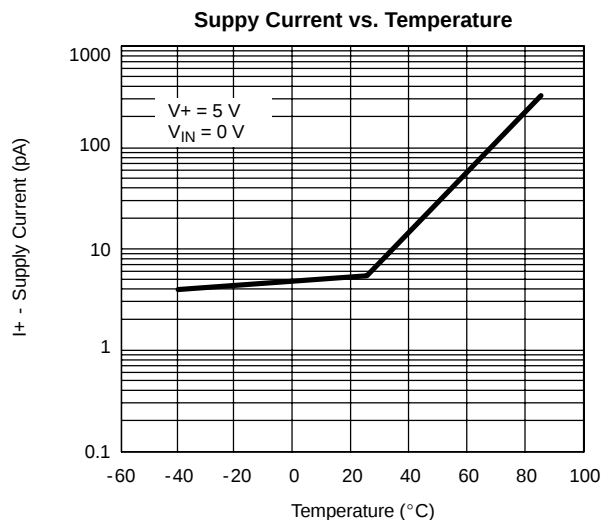
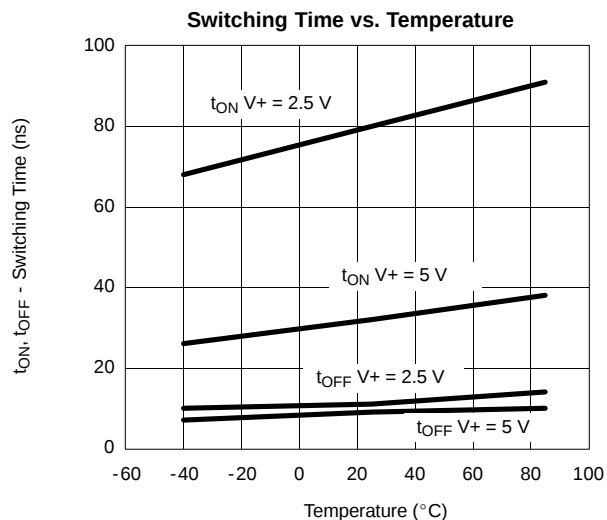
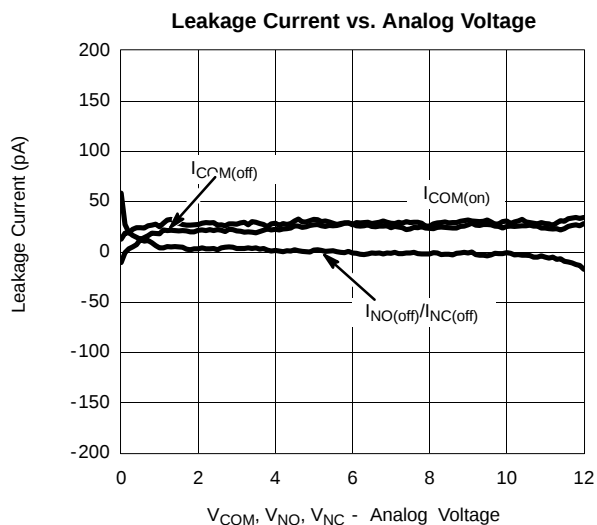
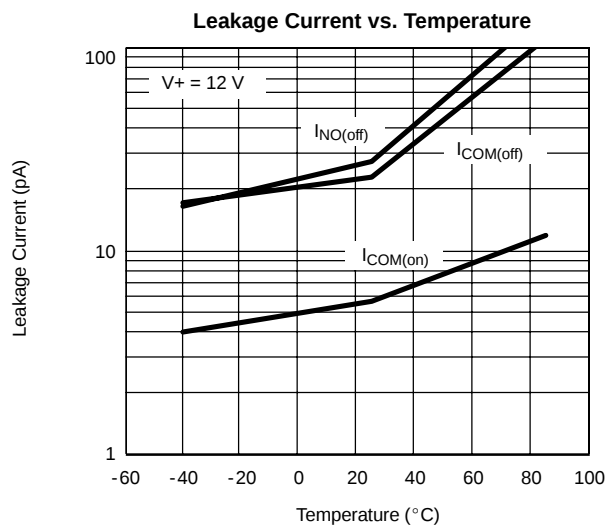
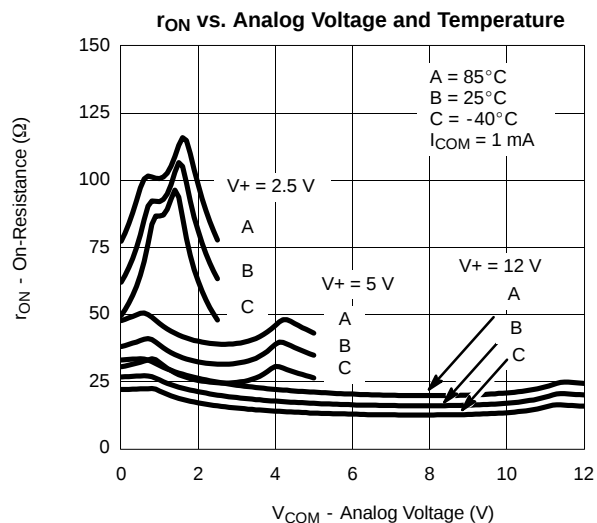
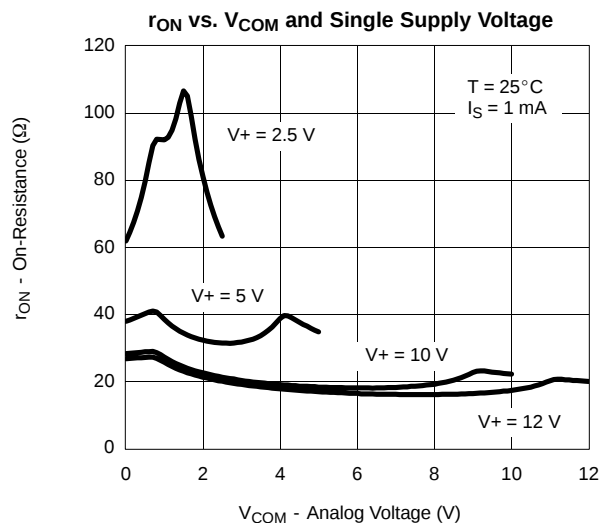
SPECIFICATIONS (V+ = 12 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V ₊ = 12 V, ±10%, V _{IN} = 0.8 or 2.4 V ^e	Temp ^a	Limits -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Switch On Resistance							
Analog Signal Range ^e	V _{ANALOG}		Full	V ₋		V ₊	V
Drain-Source On-Resistance	r _(on)	V ₊ = 10.8 V, I _{COM} = 1 mA,V _{COM} = 9 V	Room Full		19	30 40	Ω
r _{DS(on)} Match	Δr _(on)	V ₊ = 10.8 V, I _{COM} = 1 mA,V _{COM} = 9 V	Room		0.3	3.0	
Switch Off Leakage Current ^a	I _{NC/NO(off)}	V ₊ = 12 V, V _S = 1/11 V,V _{COM} = 11/1 V	Room Full	-1 -10	0.3	1 10	nA
	I _{COM(off)}		Room Full	-1 -10	0.3	1 10	
Channel On Leakage Current ^a	I _{COM(on)}		Room Full	-1 10	0.3	1 10	
Digital Control							
Input, High Voltage	V _{INH}	V+ = 12 V	Full			2.4	V
Input, Low Voltage	V _{INL}		Full	0.8			
Input Current	I _{INH}			-1		1	μA
Dynamic Characteristics							
Break-Before-Make ^{d,g}	t _{OPEN}	V ₊ = 12 V, R _L = 300 Ω V _{NO} = V _{NC} = 8 V C _L = 35 pF, V _{IN} = 0 V, 12 V	Room Full	1			ns
Turn-OnTime	t _{ON}		Room Full		21	35 40	
Turn-OffTime	t _{OFF}		Room Full		6	18 25	
Charge Injection ^d	Q	C _L = 1 nF, R _{GEN} = 0 Ω, V _g = 0 V, V ₊ = 5 V	Room		0.36		pC
Off-Isolation ^d	OIRR	C _L = 5 pF, R _L = 50 Ω, f = 1 MHz	Room		75		dB
		C _L = 5 pF, R _L = 50 Ω, f = 10 MHz	Room		53		
Crosstalk ^d	X _{TALK}	R _L = 50 Ω, f = 1 MHz, V ₊ = 5 V	Room		96		
Source Off Capacitance ^d	C _{NC/NO(off)}	f = 1 MHz, V _{NC/NO} = 0 V	Room		7.5		pF
Drain Off Capacitance ^d	C _{COM(off)}	f = 1 MHz, V _{COM} = 0 V	Room		7.8		
Drain On Capacitance ^d	C _{COM(on)}		Room		22		
Supply Current	I ₊	V ₊ = 12 V, V _{IN} =0 or V+	Room	-1		-1	μA

Notes:

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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



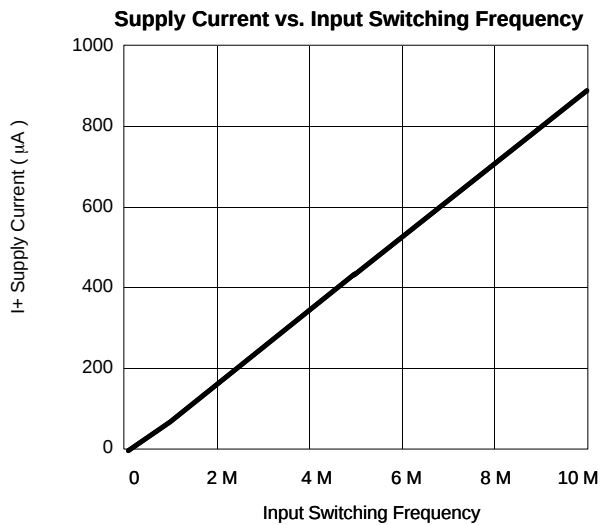
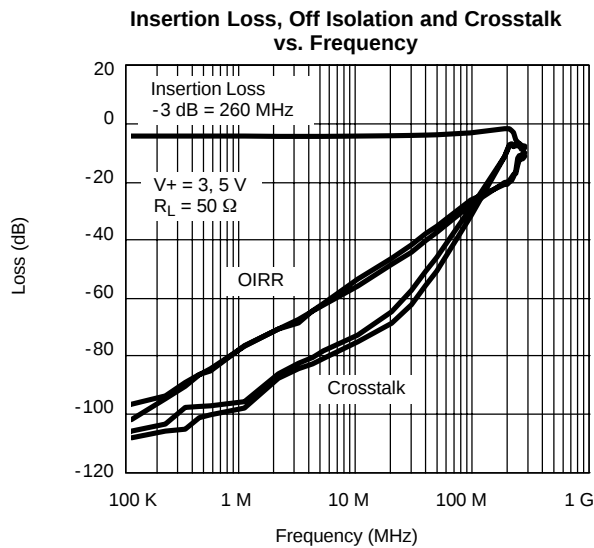
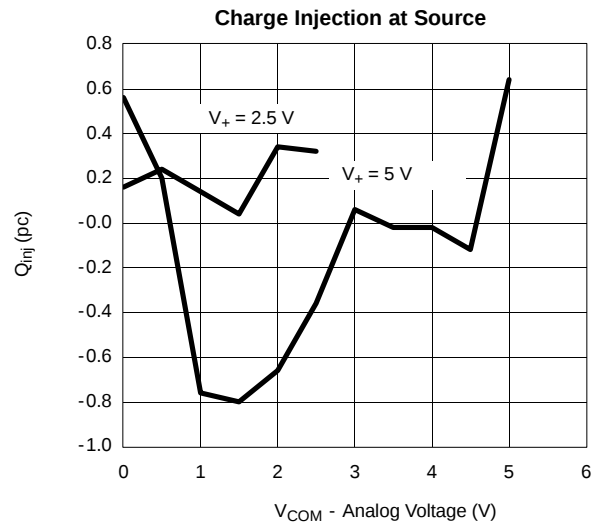
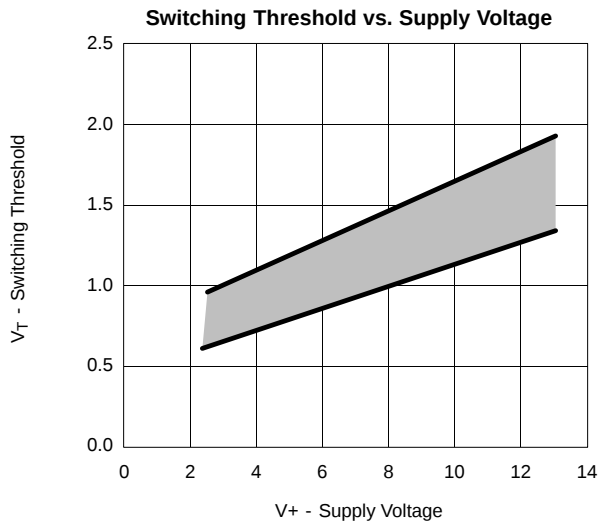


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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TEST CIRCUITS

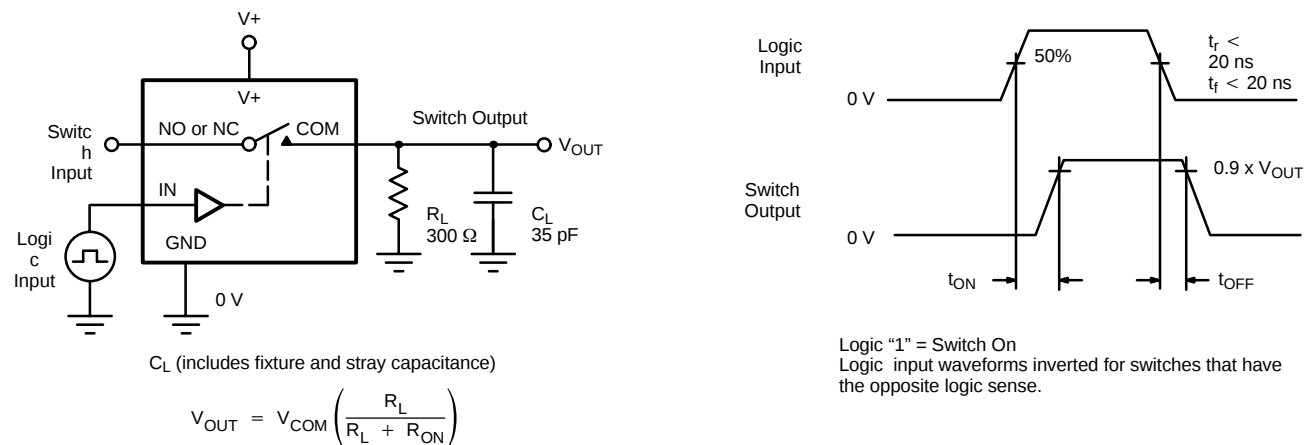


FIGURE 1. Switching Time

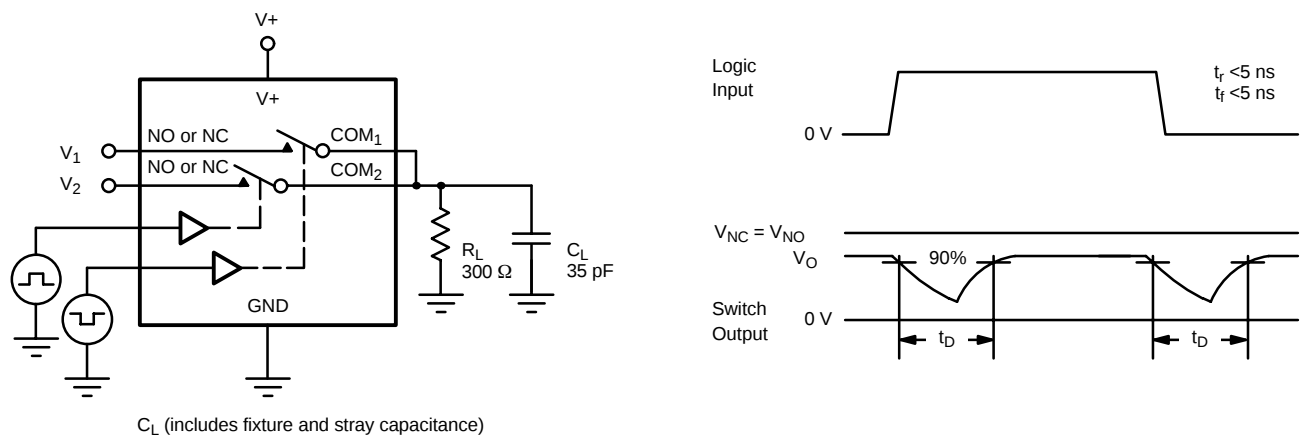


FIGURE 2. Break-Before-Make Interval

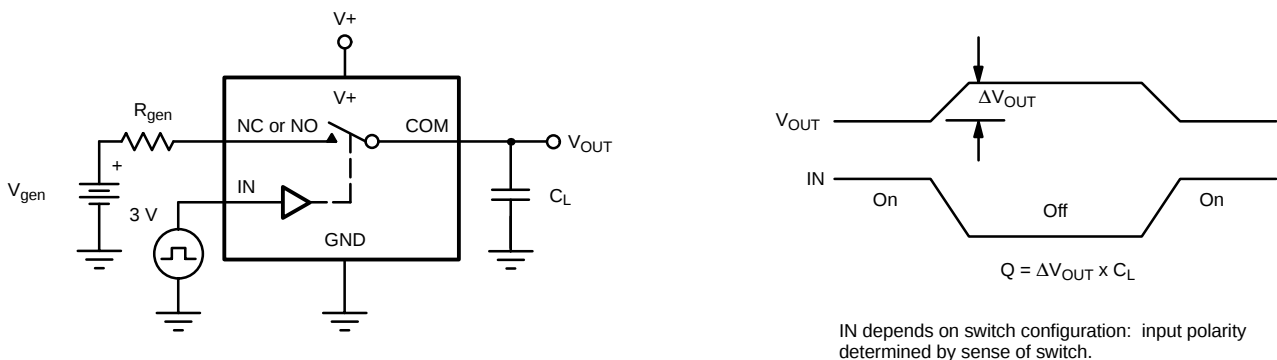


FIGURE 3. Charge Injection



TEST CIRCUITS

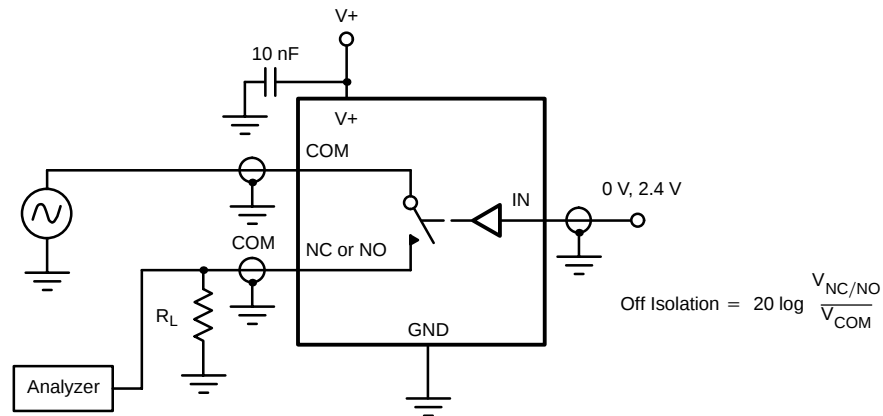


FIGURE 4. Off-Isolation

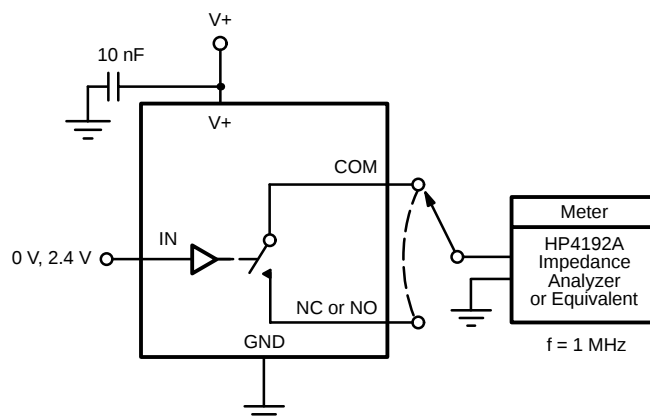


FIGURE 5. Channel Off/On Capacitance