Low-Voltage Single SPDT Analog Switch

FEATURES

Pb-free Available

- Low Voltage Operation (+2.7 to +5 V)
- Low On-Resistance - $r_{DS(on)}$: 20 Ω
- Fast Switching - t_{ON} : 35 ns, t_{OFF}: 20 ns
- Low Leakage - $I_{COM(on)}$: 200-pA max
- Low Charge Injection - Q_{INJ}: 1 pC
- Low Power Consumption
- TTL/CMOS Compatible
- ESD Protection > 2000 V (Method 3015.7)
- Available in TSOP-6 and SOIC-8
- Lead (Pb)-Free Version is RoHS Compliant

BENEFITS

- Reduced Power Consumption
- Simple Logic Interface
- High Accuracy
- Reduce Board Space (TSOP-6)

APPLICATIONS

- Battery Operated Systems
- Portable Test Equipment
- Sample and Hold Circuits
- Cellular Phones
- Communication Systems
- Military Radio
- PBX, PABX Guidance and Control Systems

DESCRIPTION

The DG9431 is a single-pole/double-throw monolithic CMOS analog device designed for high performance switching of analog signals. Combining low power, high speed (t_{ON}: 35 ns, t_{OFF}: 20 ns), low on-resistance ($r_{DS(on)}$: 20 Ω) and small physical size (TSOP-6), the DG9431 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

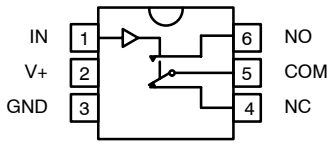
The DG9431 is built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7, is 2000 V. An epitaxial layer prevents latchup. Break-before -make is guaranteed for DG9431.

Each switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with the lead (Pb)-free device terminations. For analog switching products manufactured with 100% matte tin device terminations, the lead (Pb)-free "—E3" suffix is being used as a designator.

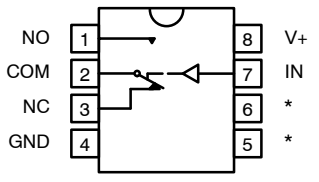
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

TSOP-6



Top View

SOIC-8



Top View

*Not Connected

TRUTH TABLE		
Logic	**NC**	**NO**
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

ORDERING INFORMATION		
Temp Range	**Package**	**Part Number**
-40 to 85°C	TSOP-6	DG9431DV-T1 DG9431DV-T1—E3 (Lead (Pb)-Free)
	SOIC-8	DG9431DY-T1 DG9431DY-T1—E3 (Lead (Pb)-Free)

ABSOLUTE MAXIMUM RATINGS

Reference to GND

V+ . . . . . -0.3 to +13 V

IN, COM, NC, NO[a] . . . . . -0.3 to (V+ + 0.3 V)

Continuous Current (Any terminal) . . . . . ±20 mA

Peak Current . . . . . ±40 mA

(Pulsed at 1ms, 10% duty cycle)

ESD (Method 3015.7) . . . . . > 2000 V

Storage Temperature (D Suffix) . . . . . -65 to 125°C

Power Dissipation (Packages)[b]

8-Pin Narrow Body SOIC[c] . . . . . 400 mW

Notes:
a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6.5 mW/°C above 75°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	D Suffix –40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		3	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V, V+ = 2.7 V, I_{COM} = 5 mA	Room Full		30	50 80	Ω
$r_{DS(on)}$ Match[d]	$\Delta r_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room		0.4	2	Ω
$r_{DS(on)}$ Flatness[f]	$r_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1 and 2 V	Room		4	8	Ω
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V / 2 V, V_{COM} = 2 V / 1 V	Room Full	-100 –5000	5	100 5000	pA
COM Off Leakage Current[g]	$I_{COM(off)}$	V_{COM} = 1 V / 2 V, V_{NO} or V_{NC} = 2 V / 1 V	Room Full	-100 –5000	5	100 5000	pA
Channel-On Leakage Current[g]	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V / 2 V	Room Full	-200 –10000	10	200 10000	pA
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V	Room Full		50	120 200	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 120	ns
Break-Before-Make Time	t_d		Room	3	20		ns
Charge Injection	Q_{INJ}	C_L = 1 nF, Vgen = 0 V, Rgen = 0 Ω	Room		1	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		–74		dB
Source-Off Capacitance	$C_{S(off)}$	f = 1 MHz	Room		7		pF
Channel-On Capacitance	$C_{D(on)}$	f = 1 MHz	Room		32		pF
Power Supply							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 3.3 V, V_{IN} = 0 or 3.3 V				1	µA

Notes:

a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 5-V leakage testing, not production tested.

SPECIFICATIONS (V+ = 5 V)

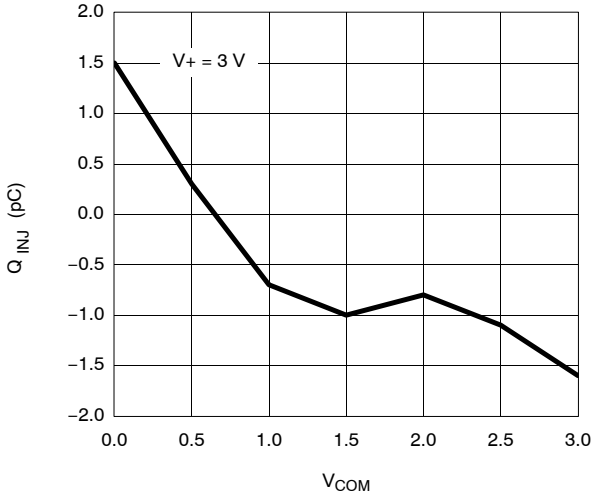
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ±10%, V_{IN} = 0.8 or 2.4 V[e]	Temp[a]	D Suffix −40 to 85°C Min[c]	Typ[b]	Max[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		5	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_{NO} or V_{NC} = 3.5 V, V+ = 4.5 V, I_{COM} = 5 mA	Room Full		20	30 50	Ω
$r_{DS(on)}$ Match[d]	$\Delta r_{DS(on)}$	V_{NO} or V_{NC} = 1.5 V	Room		0.4	2	Ω
$r_{DS(on)}$ Flatness[f]	$r_{DS(on)}$ Flatness	V_{NO} or V_{NC} = 1, 2, and 3 V	Room		2	6	Ω
NO or NC Off Leakage Current	$I_{NO/NC(off)}$	V_{NO} or V_{NC} = 1 V / 4 V, V_{COM} = 4 V / 1 V	Room Full	-100 −5000	10	100 5000	pA
COM Off Leakage Current	$I_{COM(off)}$	V_{COM} = 1 V / 4 V, V_{NO} or V_{NC} = 4 V / 1 V	Room Full	-100 −5000	10	100 5000	pA
Channel-On Leakage Current	$I_{COM(on)}$	V_{COM} = V_{NO} or V_{NC} = 1 V / 4 V	Room Full	-200 −10000		200 10000	pA
Digital Control							
Input Current	I_{INL} or I_{INH}		Full		1		µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3.0 V	Room Full		35	75 150	ns
Turn-Off Time	t_{OFF}		Room Full		20	50 100	ns
Break-Before-Make Time	t_d		Room	3	10		ns
Charge Injection	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω	Room		2	5	pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		−74		dB
NC and NO Capacitance	$C_{(off)}$	f = 1 MHz	Room		−7		pF
Channel-On Capacitance	$C_{D(on)}$		Room		32		pF
Power Supply							
Power Supply Range	V+			2.7		12	V
Power Supply Current	I+	V+ = 5.5 V, V_{IN} = 0 or 5.5 V				1	µA

Notes:

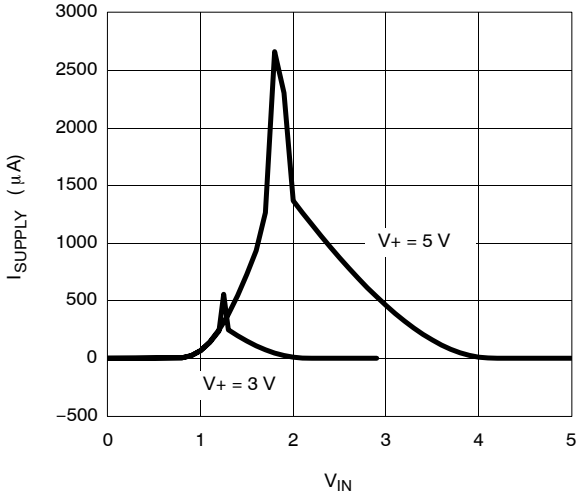
a. Room = 25°C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

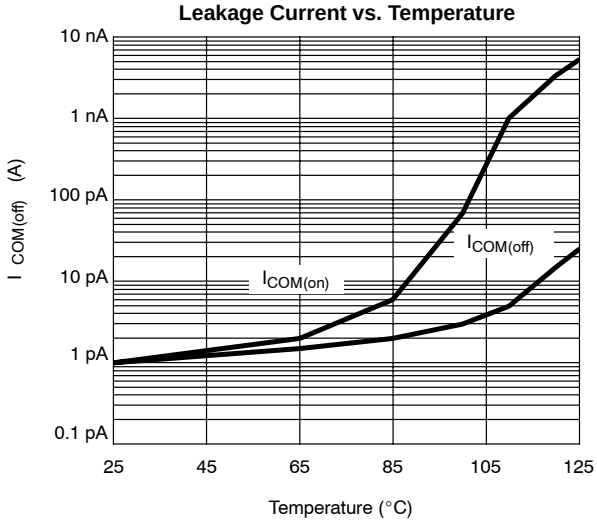
Charge Injection



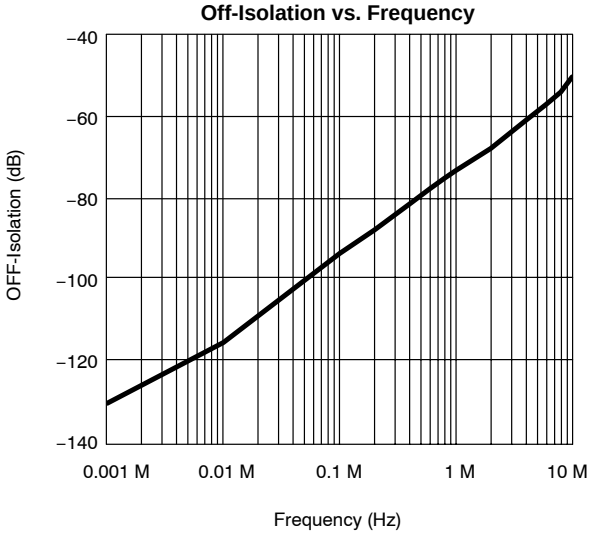
Supply Current vs. V_{IN}



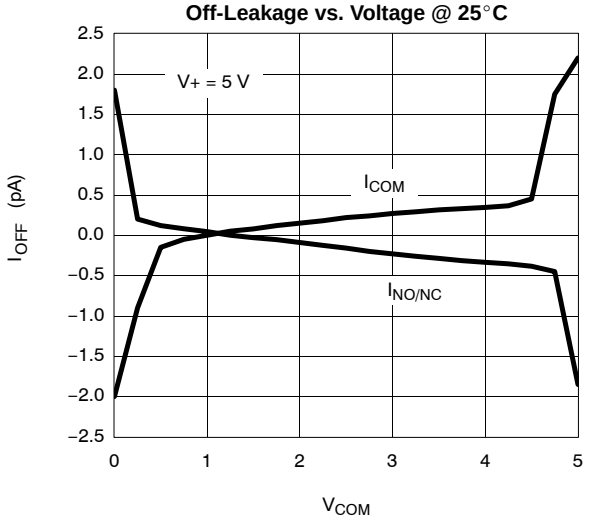
Leakage Current vs. Temperature



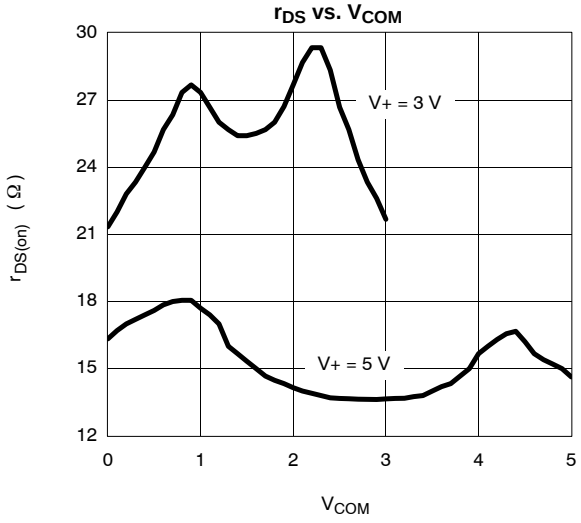
Off-Isolation vs. Frequency



Off-Leakage vs. Voltage @ 25°C



r_{DS} vs. V_{COM}



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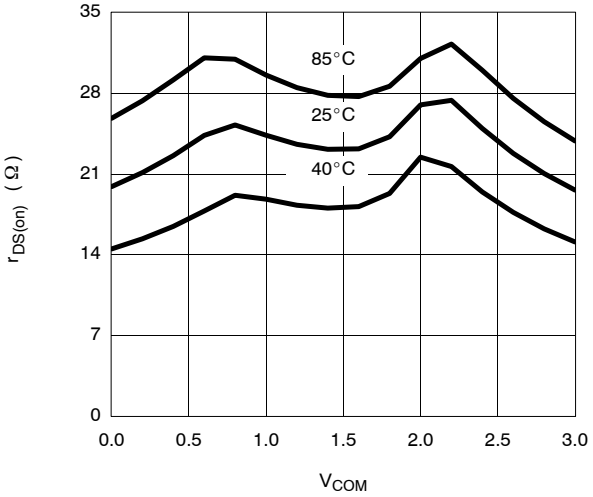
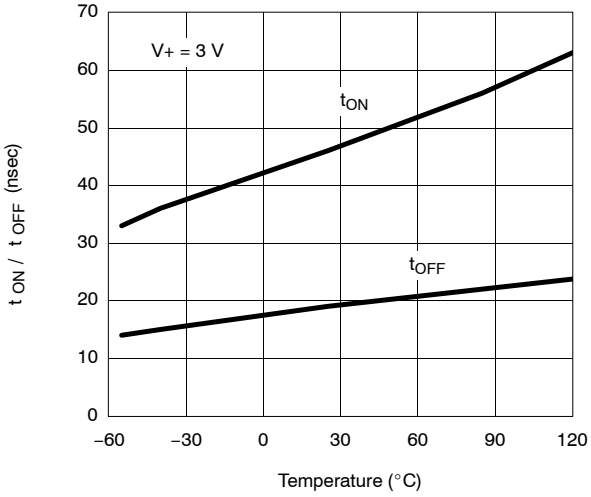
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

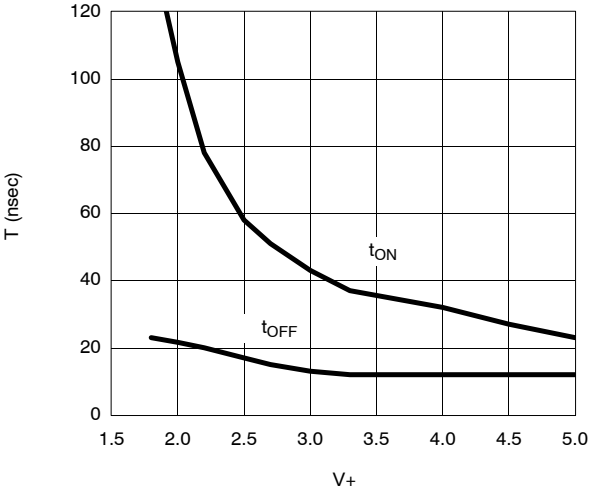
r_{DS} vs. V_{COM}



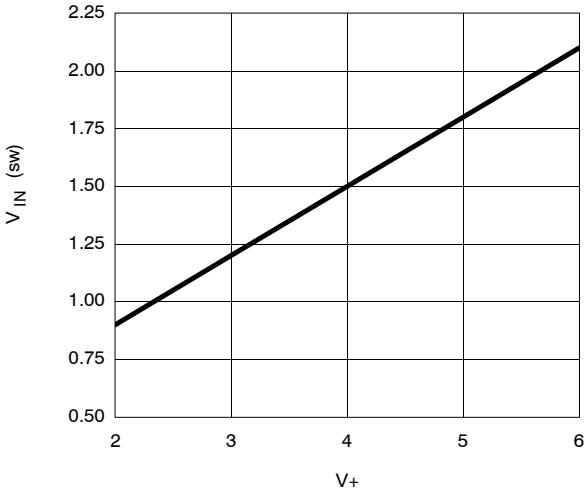
Switching Time vs. Temperature



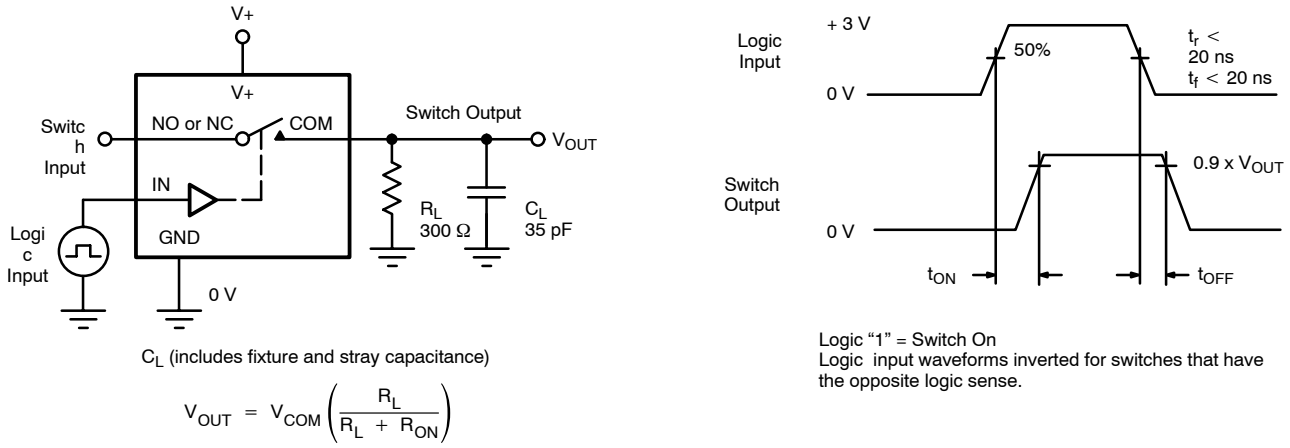
t_{ON}/t_{OFF} vs. Power Supply Voltage



Input Switching Point vs. Power Supply Voltage



TEST CIRCUITS

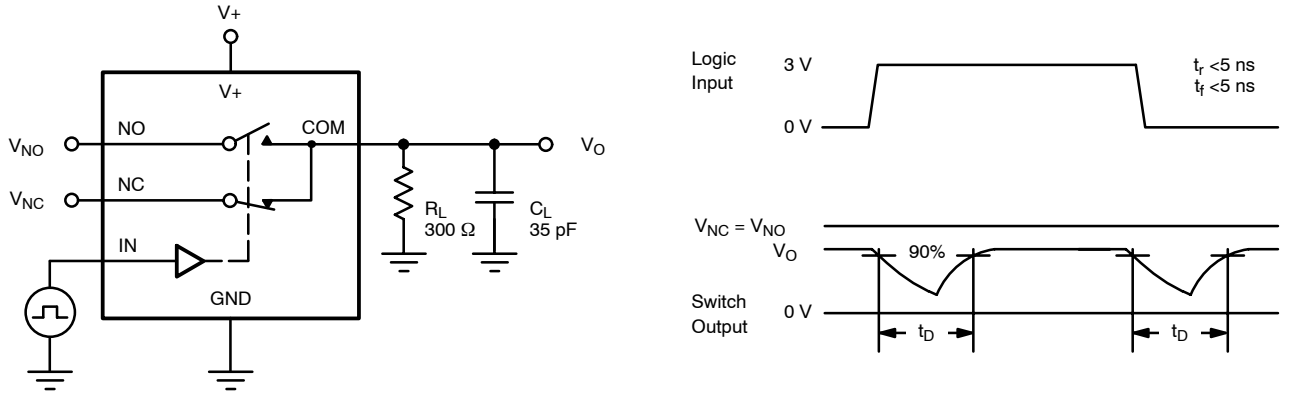


C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

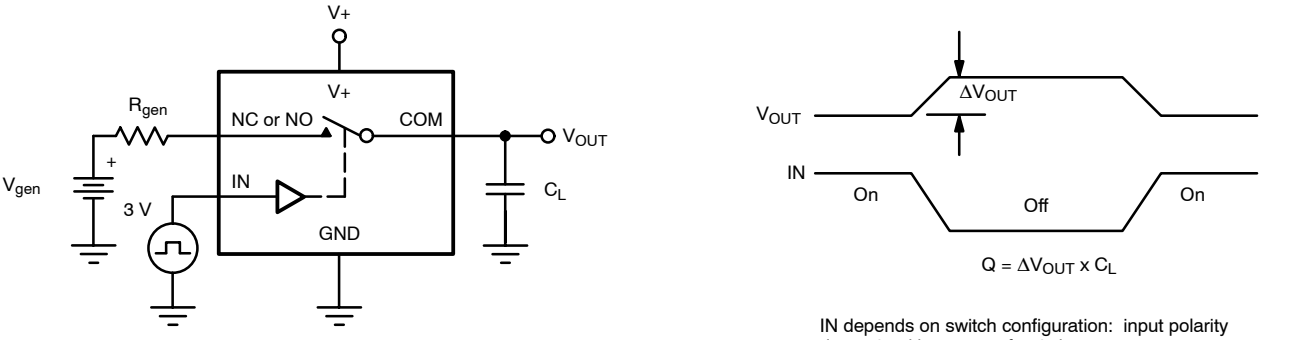
Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

FIGURE 1. Switching Time



C_L (includes fixture and stray capacitance)

FIGURE 2. Break-Before-Make Interval



IN depends on switch configuration: input polarity determined by sense of switch.

FIGURE 3. Charge Injection

TEST CIRCUITS

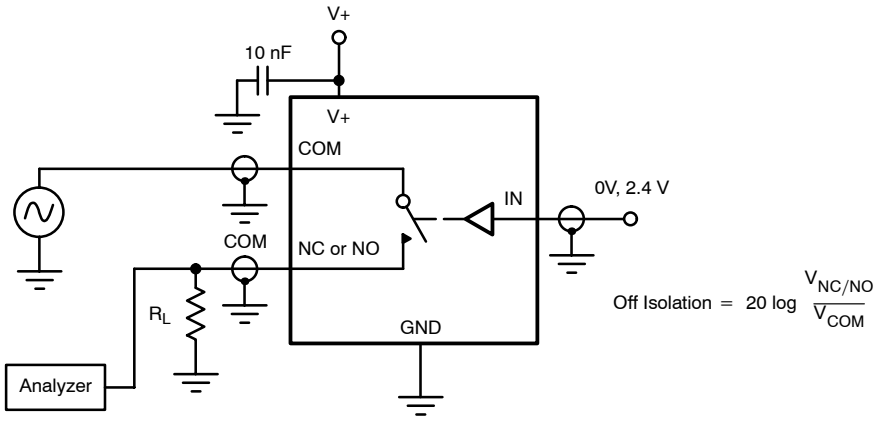


FIGURE 4. Off-Isolation

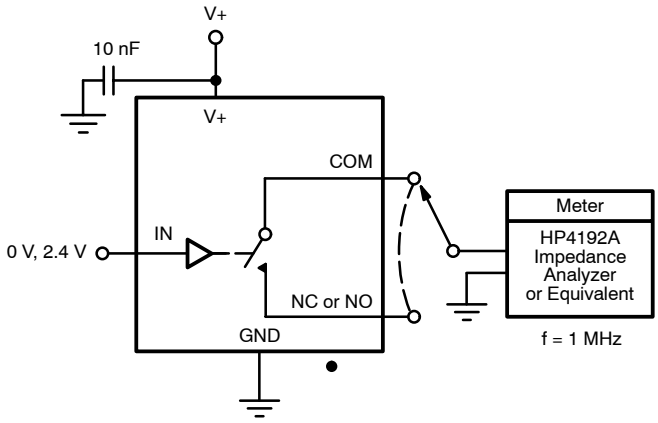


FIGURE 5. Channel Off/On Capacitance

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