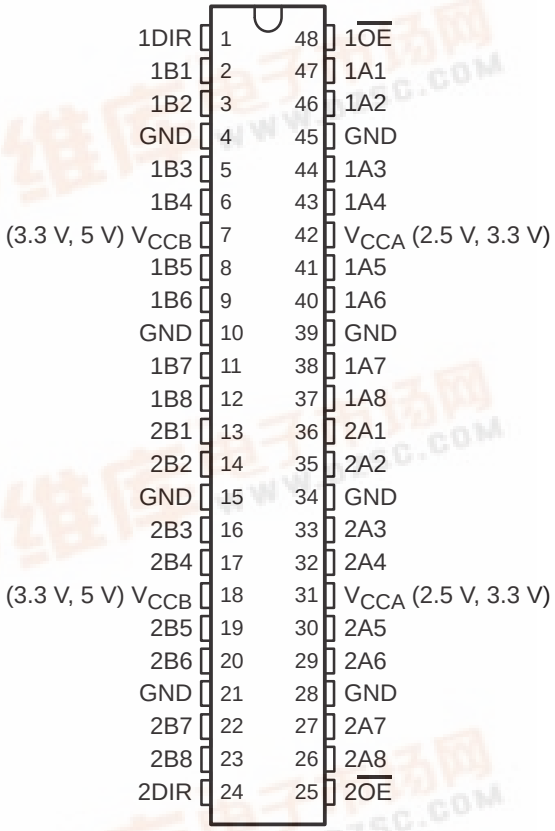
16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

SCAS416L – MARCH 1994 – REVISED FEBRUARY 2004

- **Member of the Texas Instruments Widebus™ Family**
- **Max t_{pd} of 5.8 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

DGG OR DL PACKAGE
(TOP VIEW)



description/ordering information

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has V_{CCB}, which is set to operate at 3.3 V and 5 V. A port has V_{CCA}, which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

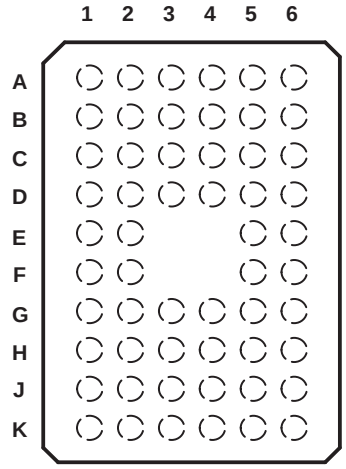
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SSOP – DL	Tube of 25	SN74ALVC164245DL	ALVC164245
		Reel of 1000	SN74ALVC164245DLR	
	TSSOP – DGG	Reel of 2000	SN74ALVC164245DGGR	ALVC164245
		Reel of 250	SN74ALVC164245DGGT	
	VFBGA – GQL	Reel of 1000	SN74ALVC164245KR	VC4245
	VFBGA – ZQL (Pb-free)		74ALVC164245ZQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

GQL OR ZQL PACKAGE
(TOP VIEW)

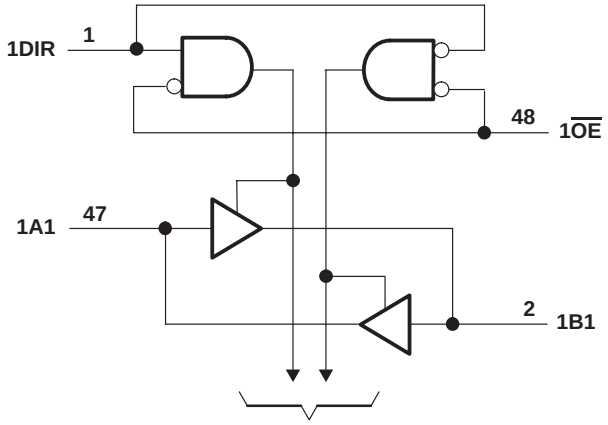


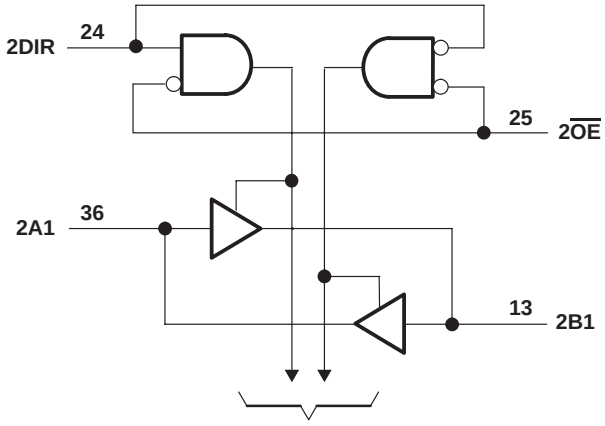
terminal assignments

	1	2	3	4	5	6
A	1DIR	NC	NC	NC	NC	$1\overline{OE}$
B	1B2	1B1	GND	GND	1A1	1A2
C	1B4	1B3	V_{CCB}	V_{CCA}	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	$2\overline{OE}$

NC − No internal connection

logic diagram (positive logic)





Pin numbers shown are for the DGG and DL packages.

absolute maximum ratings over operating free-air temperature range for V_{CCB} at 5 V and V_{CCA} at 3.3 V (unless otherwise noted)†

Supply voltage range: V_{CCA} . . . . . −0.5 V to 4.6 V
V_{CCB} . . . . . −0.5 V to 6 V
Input voltage range, V_I: Except I/O ports (see Note 1) . . . . . −0.5 V to 6 V
I/O port A (see Note 2) . . . . . −0.5 V to V_{CCA} + 0.5 V
I/O port B (see Note 1) . . . . . −0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) . . . . . −50 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . −50 mA
Continuous output current, I_O . . . . . ±50 mA
Continuous current through each V_{CC} or GND . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 70°C/W
DL package . . . . . 63°C/W
GQL/ZQL package . . . . . 42°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 6 V maximum.
2. This value is limited to 4.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions for V_{CCB} at 3.3 V and 5 V (see Note 4)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		3	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage	V_{CCB} = 3 V to 3.6 V		0.7	V
		V_{CCB} = 4.5 V to 5.5 V		0.8	
V_{IA}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current			−24	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

recommended operating conditions for V_{CCA} at 2.5 V and 3.3 V (see Note 4)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		2.3	3.6	V
V_{IH}	High-level input voltage	V_{CCA} = 2.3 V to 2.7 V	1.7		V
		V_{CCA} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CCA} = 2.3 V to 2.7 V		0.7	V
		V_{CCA} = 3 V to 3.6 V		0.8	
V_{IB}	Input voltage		0	V_{CCA}	V
V_{OA}	Output voltage		0	V_{CCA}	V
I_{OH}	High-level output current	V_{CCA} = 2.3 V		−18	mA
		V_{CCA} = 3 V		−24	
I_{OL}	Low-level output current	V_{CCA} = 2.3 V		18	mA
		V_{CCA} = 3 V		24	
$\Delta t/\Delta v$	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 2.7 V to 3.6 V and V_{CCB} = 4.5 V to 5.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP†	MAX	UNIT
V_{OH} (B to A)		I_{OH} = −100 μA	2.7 V to 3.6 V		V_{CC}−0.2			V
		I_{OH} = −12 mA	2.7 V		2.2			
			3 V		2.4			
		I_{OH} = −24 mA	3 V		2			
V_{OH} (A to B)		I_{OH} = −100 μA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = −24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL} (B to A)		I_{OL} = 100 μA	2.7 V to 3.6 V				0.2	V
		I_{OL} = 12 mA	2.7 V				0.4	
		I_{OL} = 24 mA	3 V				0.55	
V_{OL} (A to B)		I_{OL} = 100 μA		4.5 V to 5.5 V			0.2	V
		I_{OL} = 24 mA		4.5 V to 5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}/V_{CCB}$ or GND	3.6 V	5.5 V			±5	μA
I_{OZ}‡	A or B ports	$V_O = V_{CCA}/V_{CCB}$ or GND	3.6 V	5.5 V			±10	μA
I_{CC}		$V_I = V_{CCA}/V_{CCB}$ or GND, I_O = 0	5.5 V	5.5 V			40	μA
ΔI_{CC}§		One input at V_{CCA}/V_{CCB} − 0.6 V, Other inputs at V_{CCA}/V_{CCB} or GND	3 V to 3.6 V	4.5 V to 5.5 V			750	μA
C_i	Control inputs	$V_I = V_{CCA}/V_{CCB}$ or GND	3.3 V	5 V		6.5		pF
C_{io}	A or B ports	$V_O = V_{CCA}/V_{CCB}$ or GND	3.3 V	3.3 V		8.5		pF

† Typical values are measured at V_{CCA} = 3.3 V and V_{CCB} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.
§ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC}.

electrical characteristics over recommended operating free-air temperature range for V_{CCA} = 2.3 V to 2.7 V and V_{CCB} = 3 V to 3.6 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{OH} (B to A)		I_{OH} = −100 μA	2.3 V to 2.7 V	3 V to 3.6 V	V_{CCA}−0.2		V
		I_{OH} = −8 mA	2.3 V	3 V to 3.6 V	1.7		
		I_{OH} = −12 mA	2.7 V	3 V to 3.6 V	1.8		
V_{OH} (A to B)		I_{OH} = −100 μA	2.3 V to 2.7 V	3 V to 3.6 V	V_{CCB}−0.2		V
		I_{OH} = −18 mA	2.3 V to 2.7 V	3 V	2.2		
V_{OL} (B to A)		I_{OL} = 100 μA	2.3 V to 2.7 V	3 V to 3.6 V		0.2	V
		I_{OL} = 12 mA	2.3 V	3 V to 3.6 V		0.6	
V_{OL} (A to B)		I_{OL} = 100 μA	2.3 V to 2.7 V	3 V to 3.6 V		0.2	V
		I_{OL} = 18 mA	2.3 V	3 V		0.55	
I_I	Control inputs	$V_I = V_{CCA}/V_{CCB}$ or GND	2.3 V to 2.7 V	3 V to 3.6 V		±5	μA
I_{OZ}†	A or B ports	$V_O = V_{CCA}/V_{CCB}$ or GND	2.3 V to 2.7 V	3 V to 3.6 V		±10	μA
I_{CC}		$V_I = V_{CCA}/V_{CCB}$ or GND, I_O = 0	2.3 V to 2.7 V	3 V to 3.6 V		20	μA
ΔI_{CC}‡		One input at V_{CCA}/V_{CCB} − 0.6 V, Other inputs at V_{CCA}/V_{CCB} or GND	2.3 V to 2.7 V	3 V to 3.6 V		750	μA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.
‡ This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated V_{CC}.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1-4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 3.3 V ± 0.3 V	V_{CCB} = 5 V ± 0.5 V			UNIT
			V_{CCA} = 2.5 V ± 0.2 V	V_{CCA} = 2.7 V		V_{CCA} = 3.3 V ± 0.3 V	
			MIN MAX	MIN	MAX	MIN MAX	
t_{pd}	A	B	7.6	5.9		1 5.8	ns
	B	A	7.6	6.7		1.2 5.8	
t_{en}	$\overline{OE}$	B	11.5	9.3		1 8.9	ns
t_{dis}	$\overline{OE}$	B	10.5	9.2		2.1 9.5	ns
t_{en}	$\overline{OE}$	A	12.3	10.2		2 9.1	ns
t_{dis}	$\overline{OE}$	A	9.3	9		2.9 8.6	ns

operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCB} = 3.3 V	V_{CCB} = 5 V	UNIT
			V_{CCA} = 2.5 V	V_{CCA} = 3.3 V	
			TYP	TYP	
C_{pd} Power dissipation capacitance	Outputs enabled (B)	C_L = 50 pF, f = 10 MHz	55	56	pF
	Outputs disabled (B)		27	6	
	Outputs enabled (A)	C_L = 50 pF, f = 10 MHz	118	56	
	Outputs disabled (A)		58	6	

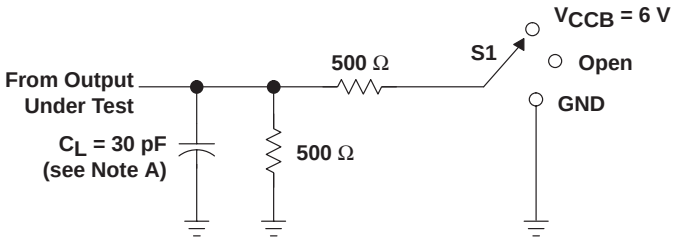
power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

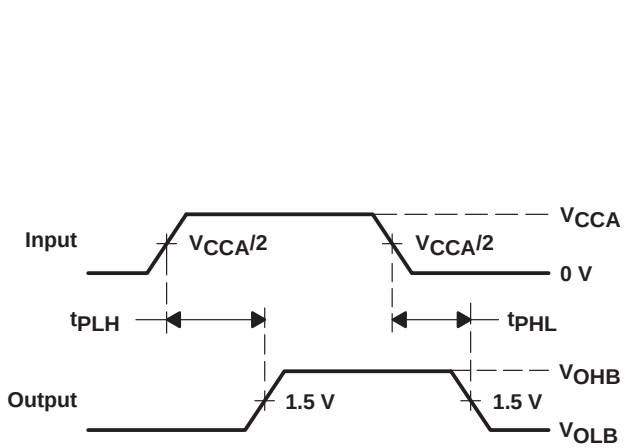
† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

PARAMETER MEASUREMENT INFORMATION
V_{CCA}= 2.5 V ± 0.2 V TO V_{CCB}= 3.3 V ± 0.3 V

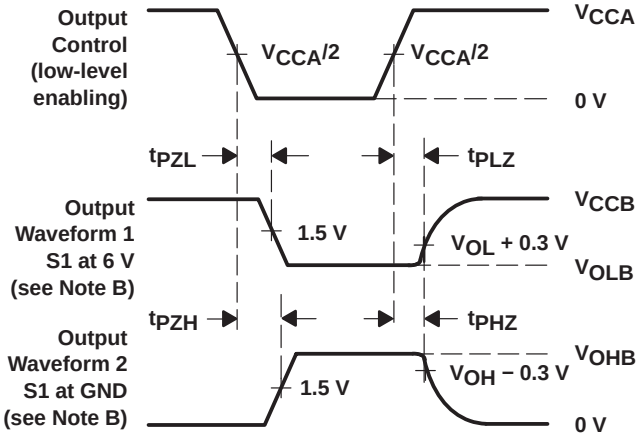


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open V_{CCB} = 6 V GND

LOAD CIRCUIT



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

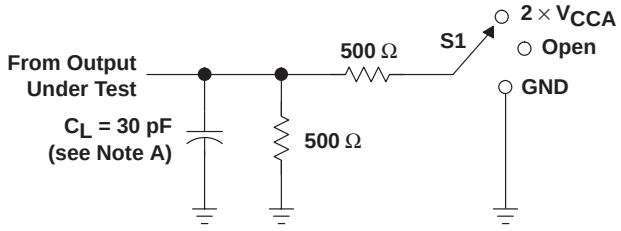


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f≤2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

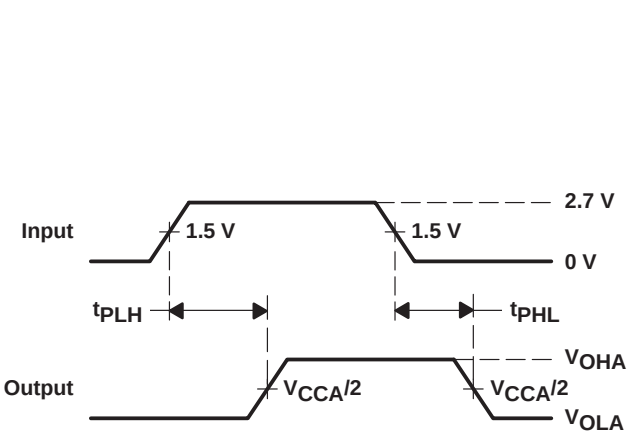
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CCB} = 3.3 V ± 0.3 V TO V_{CCA} = 2.5 V ± 0.2 V

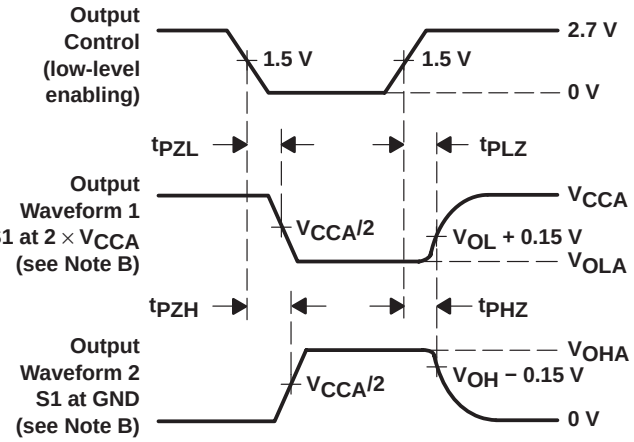


LOAD CIRCUIT

TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CCA} GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

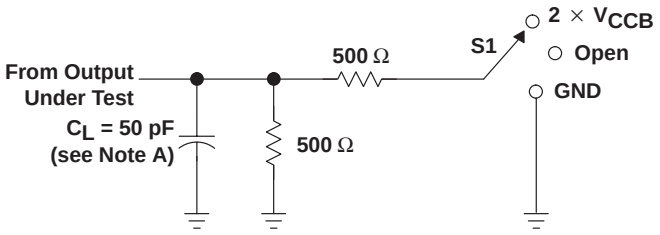


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50 Ω, t_r≤2 ns, t_f≤2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

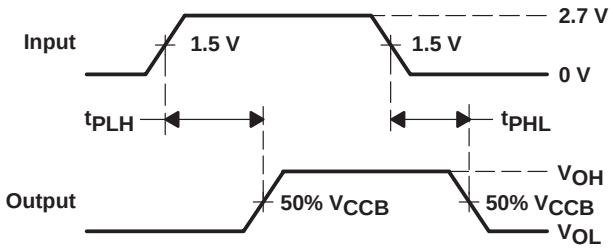
Figure 2. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CCA} = 3.3 V ± 0.3 V TO V_{CCB} = 5 V ± 0.5 V

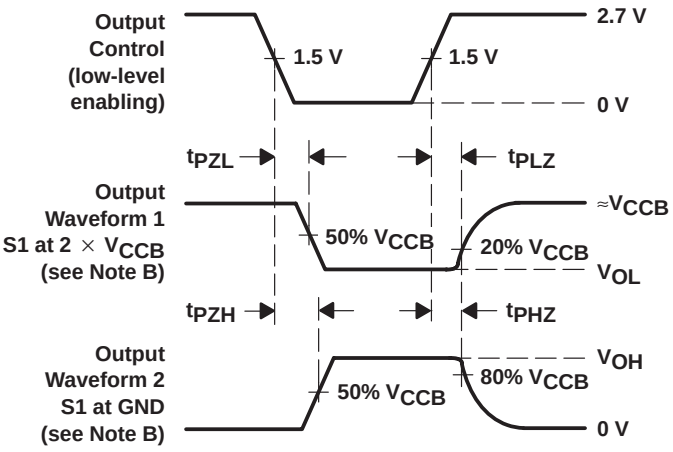


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCB}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

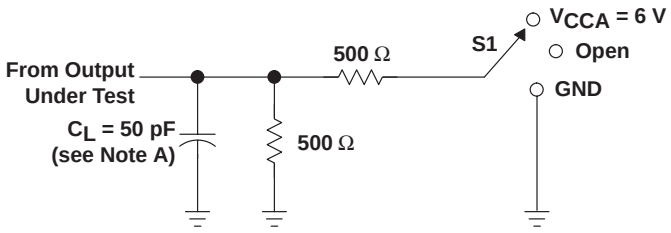


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

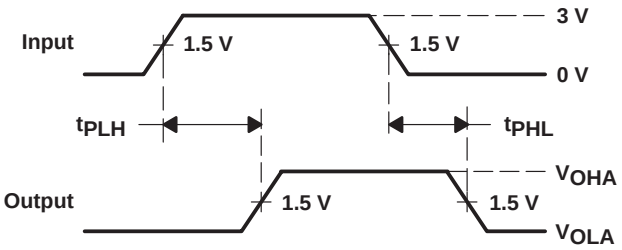
Figure 3. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION
V_{CCB} = 5 V ± 0.5 V TO V_{CCA} = 2.7 V AND 3.3 V ± 0.3 V

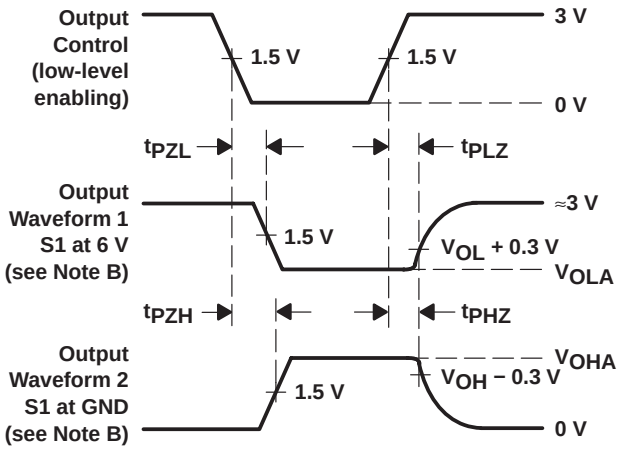


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	V_{CCA} = 6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

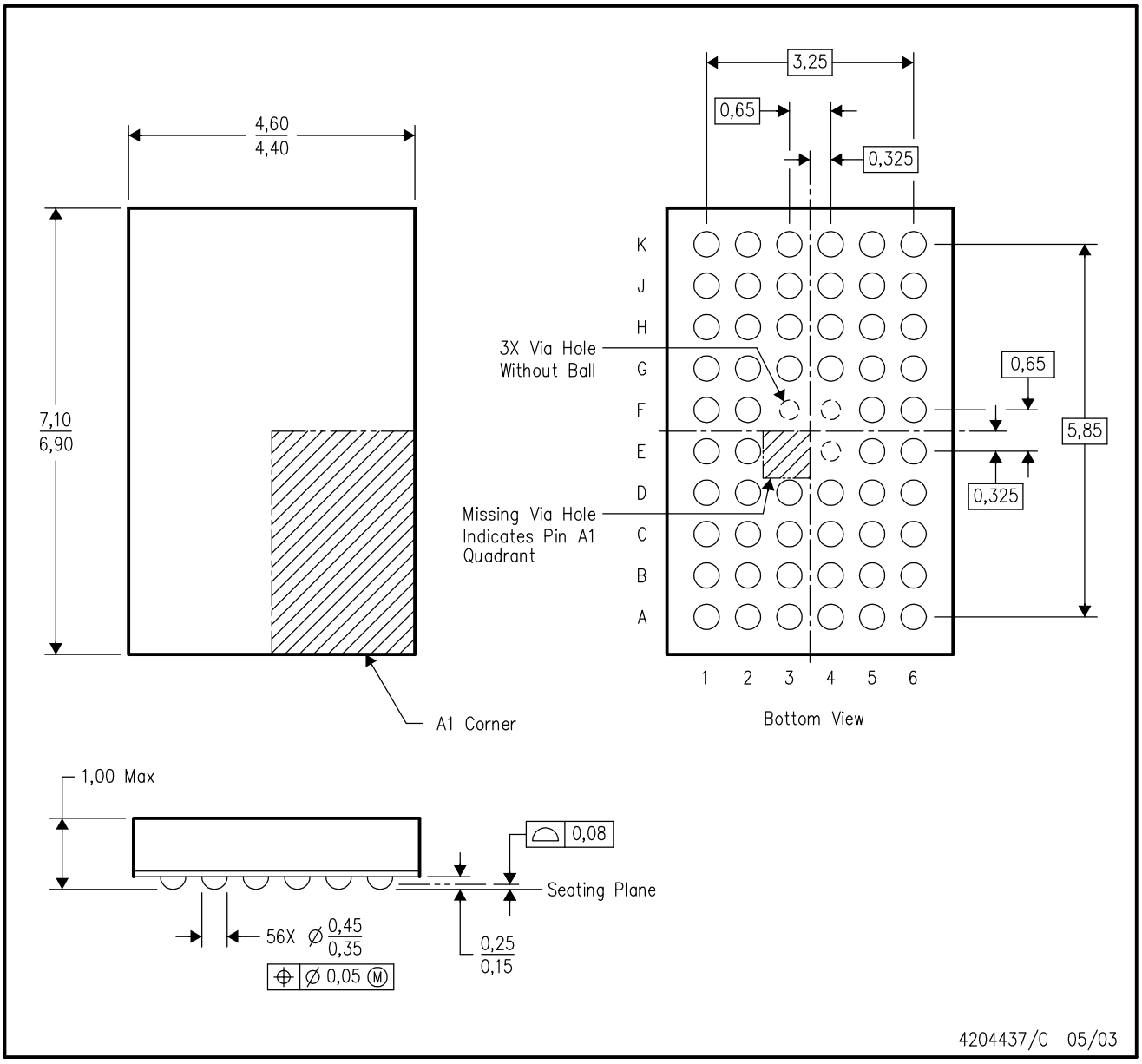


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 4. Load Circuit and Voltage Waveforms

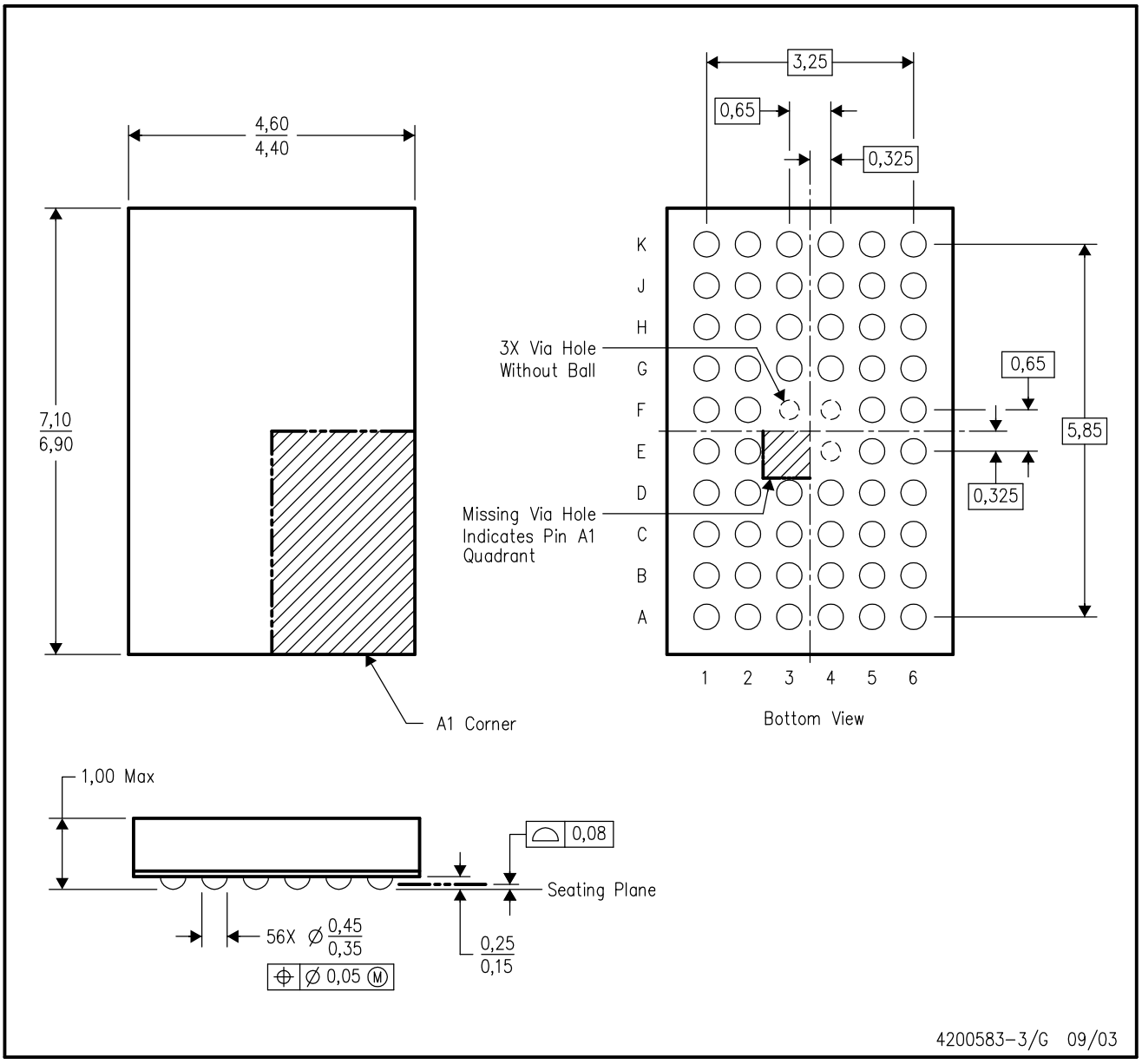
ZQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is lead–free. Refer to the 56 GQL package (drawing 4200583) for tin–lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments.

GQL (R–PBGA–N56) PLASTIC BALL GRID ARRAY



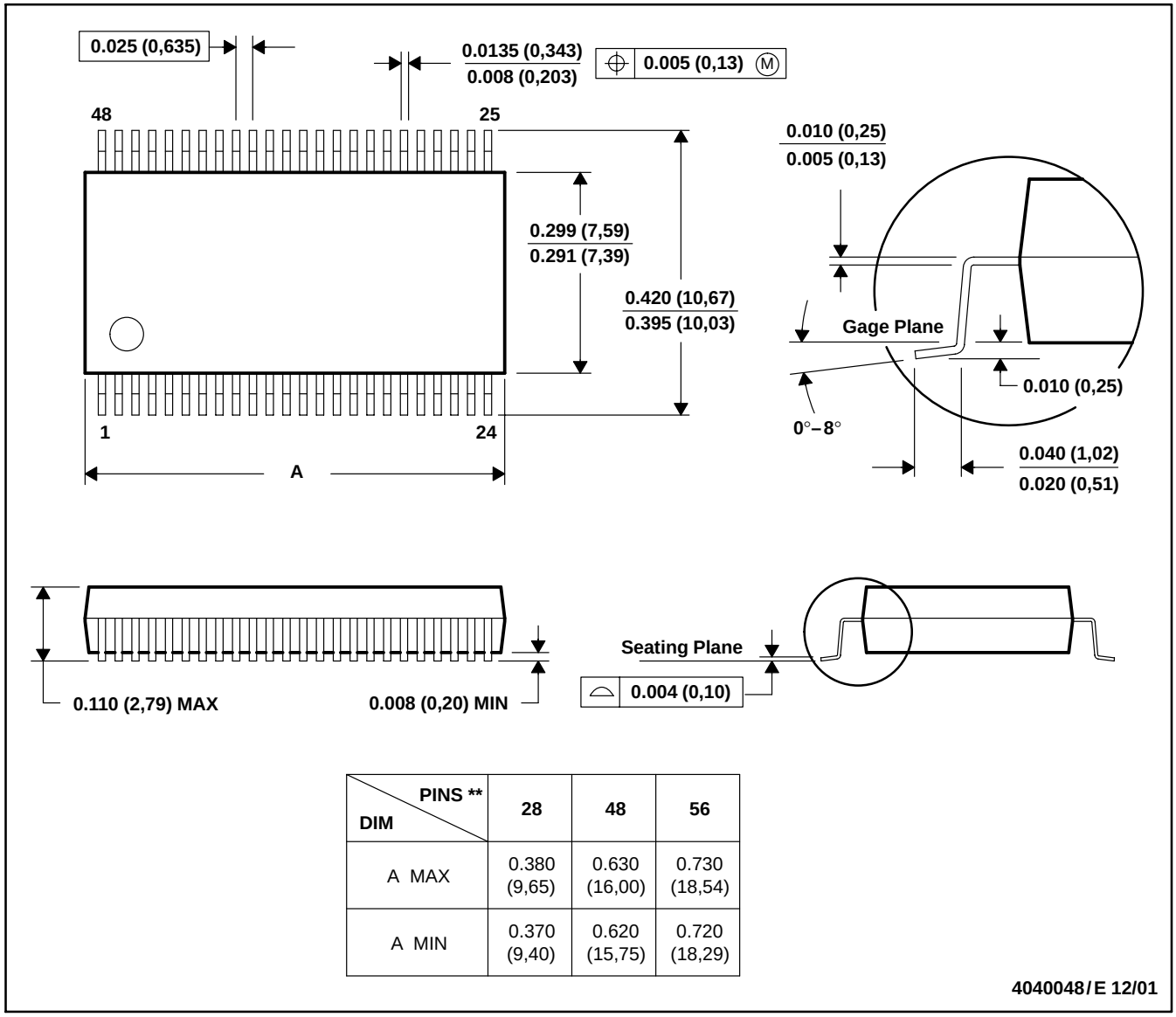
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ BGA configuration.
D. Falls within JEDEC MO–225 variation BA.
E. This package is tin–lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead–free.

MicroStar Junior is a trademark of Texas Instruments.

MSSO001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

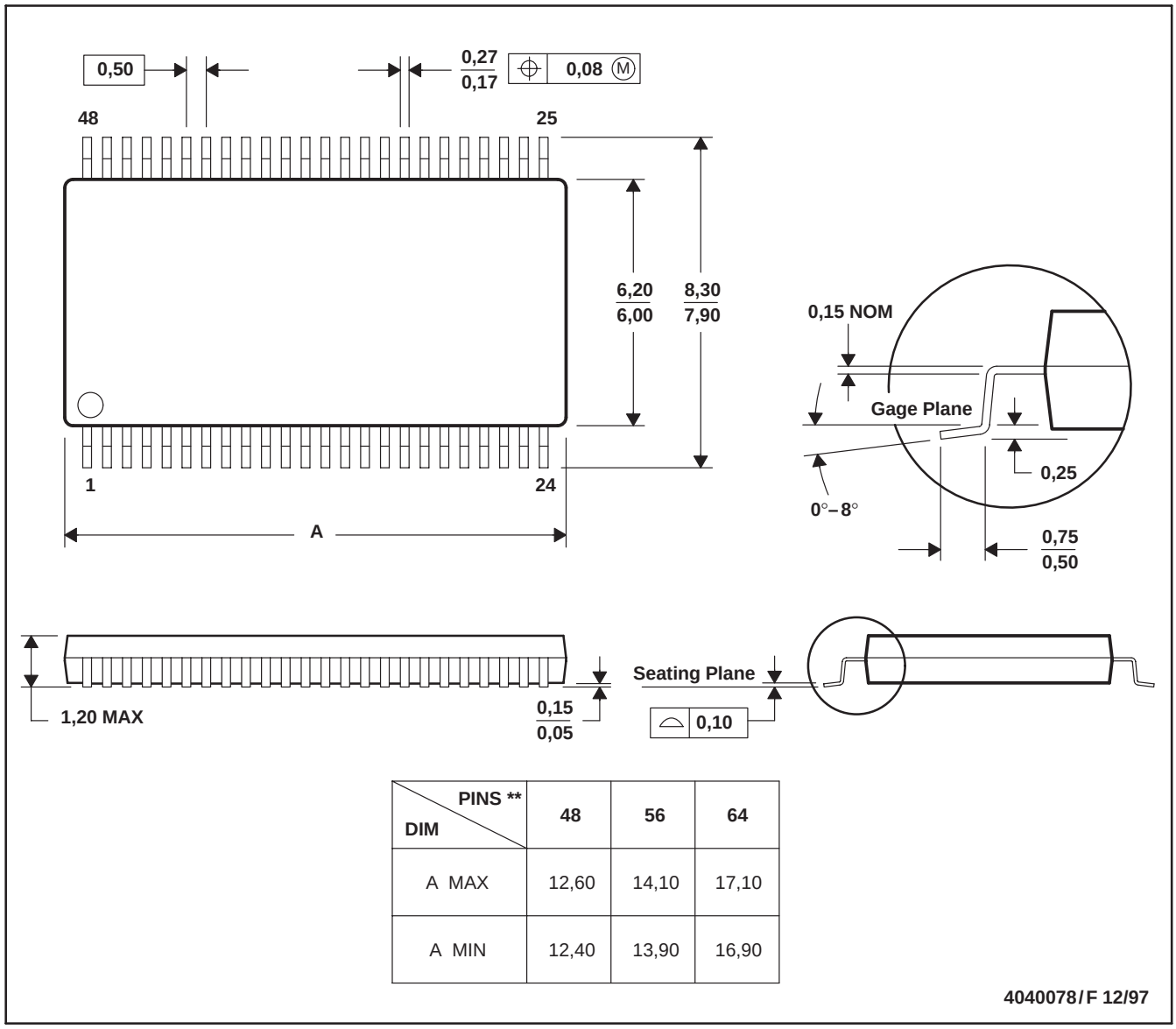
4040048/E 12/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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