

# SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS149D – JULY 1994 – REVISED MARCH 2004

- **Members of the Texas Instruments Widebus™ Family**
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )**
- **Support Unregulated Battery Operation Down to 2.7 V**
- **Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **$I_{off}$  and Power-Up 3-State Support Hot Insertion**
- **Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flowthrough Architecture Optimizes PCB Layout**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVT16646...WD PACKAGE  
SN74LVT16646...DGG OR DL PACKAGE  
(TOP VIEW)

1DIR	1	56	1OE
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A1	5	52	1B1
1A2	6	51	1B2
$V_{CC}$	7	50	$V_{CC}$
1A3	8	49	1B3
1A4	9	48	1B4
1A5	10	47	1B5
GND	11	46	GND
1A6	12	45	1B6
1A7	13	44	1B7
1A8	14	43	1B8
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
$V_{CC}$	22	35	$V_{CC}$
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	2OE

## description/ordering information

The 'LVT16646 devices are 16-bit bus transceivers and registers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVT16646 devices.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SSOP – DL	Tube	SN74LVT16646DL	LVT16646
		Tape and reel	SN74LVT16646DLR	
	TSSOP – DGG	Tape and reel	SN74LVT16646DGGR	LVT16646
–55°C to 125°C	CFP – WD	Tube	SNJ54LVT16646WD	SNJ54LVT16646WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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# SN54LVT16646, SN74LVT16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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### description/ordering information (continued)

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. The direction control (DIR) determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE

INPUTS						DATA I/Os		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at  $\overline{OE}$  and DIR. Data input functions always are enabled; i.e., data at the bus pins are stored on every low-to-high transition of the clock inputs.

# SN54LVT16646, SN74LVT16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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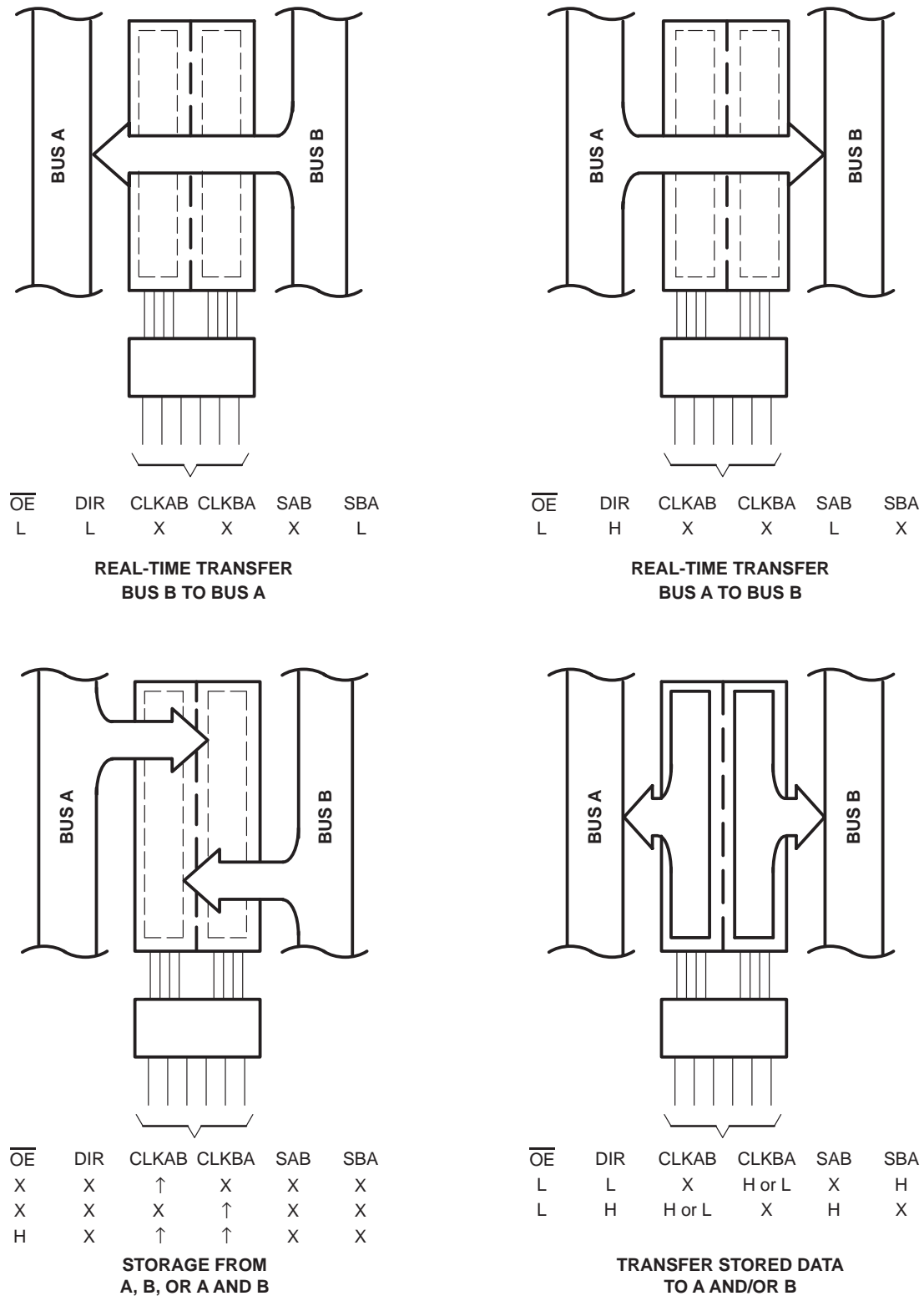


Figure 1. Bus-Management Functions

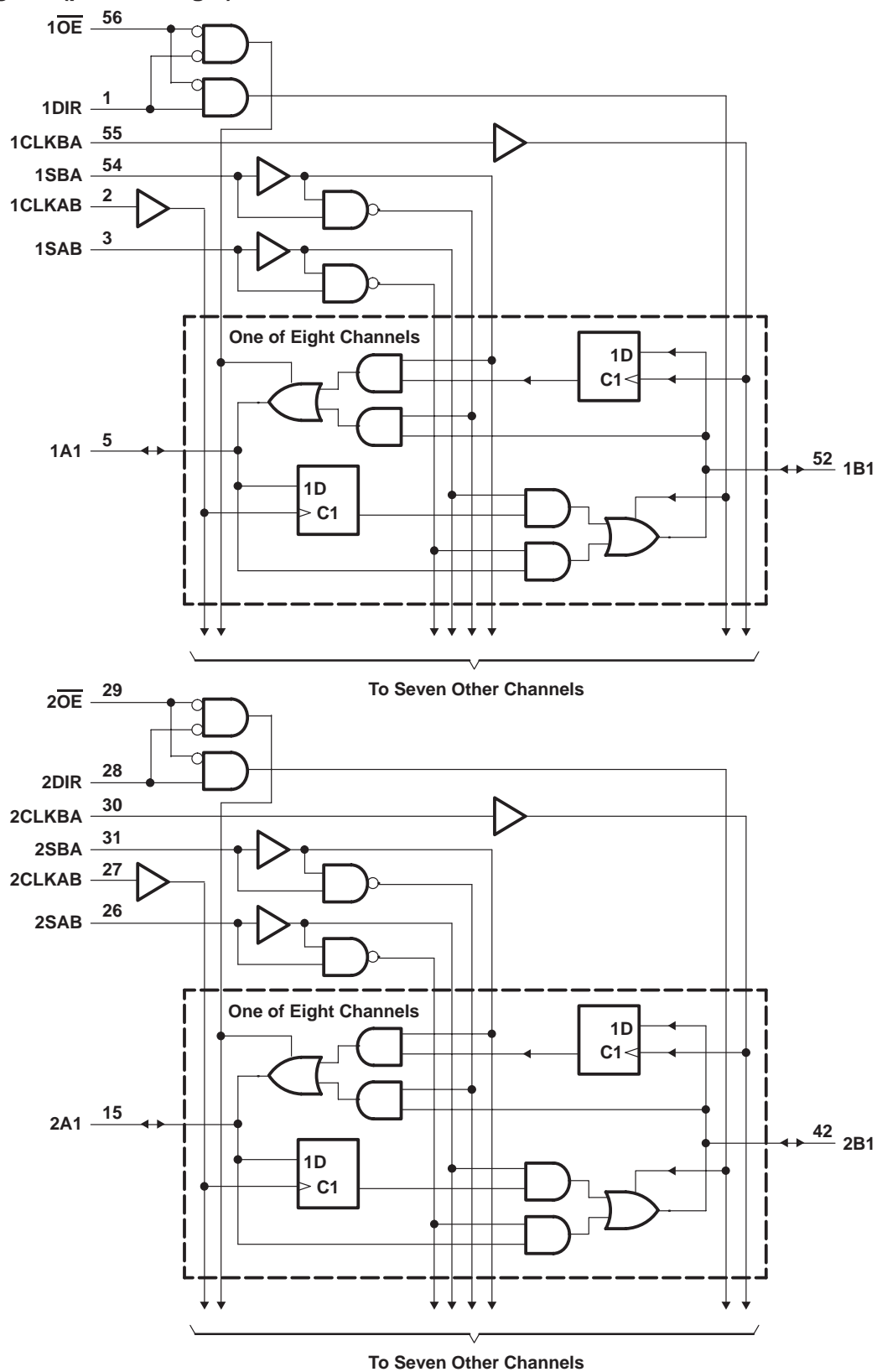
# SN54LVT16646, SN74LVT16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

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logic diagram (positive logic)



# SN54LVT16646, SN74LVT16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Current into any output in the low state, $I_O$ : SN54LVT16646	96 mA
SN74LVT16646	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVT16646	48 mA
SN74LVT16646	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package	64°C/W
DL package	56°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51–7.

### recommended operating conditions (see Note 4)

		SN54LVT16646		SN74LVT16646		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVT16646, SN74LVT16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVT16646			SN74LVT16646			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$				-1.2			-1.2	V
$V_{OH}$	$V_{CC} = \text{MIN to MAX}^\ddagger$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
		$I_{OH} = -32\text{ mA}$				2			
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$			0.2			0.2	V
		$I_{OL} = 24\text{ mA}$			0.5			0.5	
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$			0.4			0.4	
		$I_{OL} = 32\text{ mA}$			0.5			0.5	
		$I_{OL} = 48\text{ mA}$			0.55				
		$I_{OL} = 64\text{ mA}$						0.55	
$I_I$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND	Control inputs			$\pm 1$			$\pm 1$	$\mu\text{A}$
	$V_{CC} = 0$ or $\text{MAX}^\ddagger$ , $V_I = 5.5\text{ V}$				10			10	
	$V_{CC} = 3.6\text{ V}$	$V_I = 5.5\text{ V}$			20			20	
		$V_I = V_{CC}$			5			5	
		$V_I = 0$			-10			-10	
$I_{off}$	$V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $4.5\text{ V}$							$\pm 100$	$\mu\text{A}$
$I_{I(\text{hold})}$	$V_{CC} = 3\text{ V}$	$V_I = 0.8\text{ V}$	A or B ports		75			75	$\mu\text{A}$
		$V_I = 2\text{ V}$			-75			-75	
$I_{OZH}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$				1			1	$\mu\text{A}$
$I_{OZL}$	$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$				-1			-1	$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND $I_O = 0$ ,	Outputs high			0.12			0.12	mA
		Outputs low			5			5	
		Outputs disabled			0.12			0.12	
$\Delta I_{CC}^\P$	$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}$ or GND				0.2			0.2	mA
$C_i$	$V_I = 3\text{ V}$ or 0				3.5			3.5	pF
$C_{io}$	$V_O = 3\text{ V}$ or 0				12			12	pF

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ Unused pins at  $V_{CC}$  or GND

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

# SN54LVT16646, SN74LVT16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS

### WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

			SN54LVT16646				SN74LVT16646				UNIT
			$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency		150		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low		3.3		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.3		1.4		1.3		1.4		ns
		Data low	2.4		3		2.4		3		
t <sub>h</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5		0		0.5		0		ns
		Data low	0.6		0.5		0.5		0.5		

switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT16646				SN74LVT16646				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V			
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			150				150				MHz	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	1.8	6	6.9		1.8	3.8	5.7	6.7		ns
t <sub>PHL</sub>			2.1	5.9	6.6		2.1	3.9	5.7	6.5		
t <sub>PLH</sub>	A or B	B or A	1.3	4.9	5.6		1.3	3	4.7	5.4		ns
t <sub>PHL</sub>			1	4.8	5.8		1	3.1	4.7	5.6		
t <sub>PLH</sub>	SBA or SAB‡	A or B	1.4	6.4	7.4		1.4	4	6.2	7.2		ns
t <sub>PHL</sub>			1.4	6.4	7.4		1.4	4.3	6.2	7.2		
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	1	5.7	7.4		1	3	5.4	6.4		ns
t <sub>PZL</sub>			1	6.5	7.5		1	3.1	5.6	6.5		
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	2.3	6.7	7.1		2.3	4.6	6.5	6.9		ns
t <sub>PLZ</sub>			2.2	6	6.5		2.2	4.5	5.8	5.9		
t <sub>PZH</sub>	DIR	A or B	1	5.9	7.7		1	3.3	5.7	6.7		ns
t <sub>PZL</sub>			1.2	5.9	7.3		1.2	3.5	5.8	6.7		
t <sub>PHZ</sub>	DIR	A or B	1.7	7.3	8.5		1.7	4.7	7.2	8.3		ns
t <sub>PLZ</sub>			1.5	7.8	7.4		1.5	4.9	6.6	7.2		

$\dagger$  All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

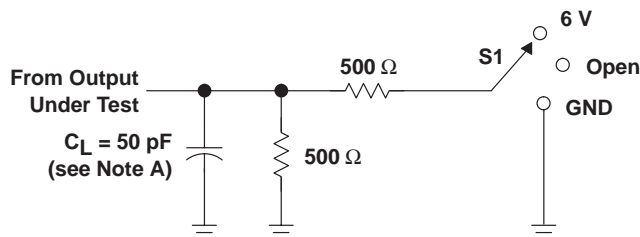
$\ddagger$  These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

# SN54LVT16646, SN74LVT16646

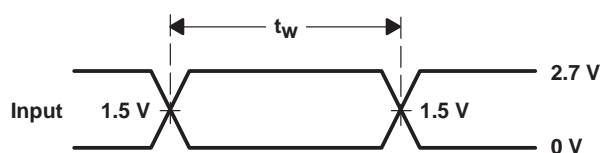
## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

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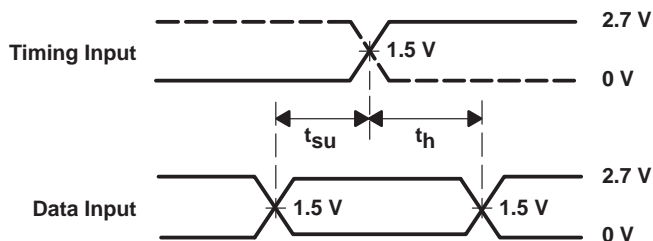
### PARAMETER MEASUREMENT INFORMATION



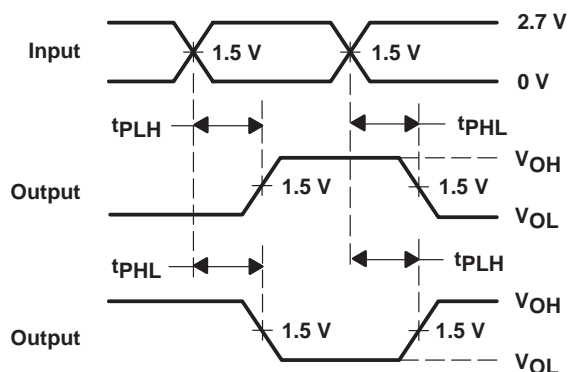
LOAD CIRCUIT FOR OUTPUTS



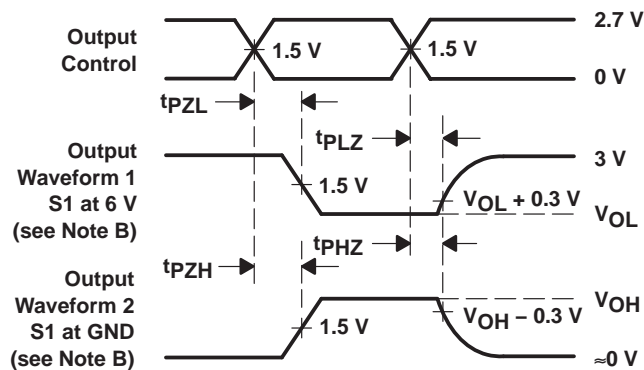
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
D. The outputs are measured one at a time, with one transition per measurement.  
E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74LVT16646DGGR	ACTIVE	TSSOP	DGG	56	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
SN74LVT16646DL	ACTIVE	SSOP	DL	56	20	TBD	CU NIPDAU	Level-1-235C-UNLIM
SN74LVT16646DLR	NRND	SSOP	DL	56	1000	TBD	CU NIPDAU	Level-1-235C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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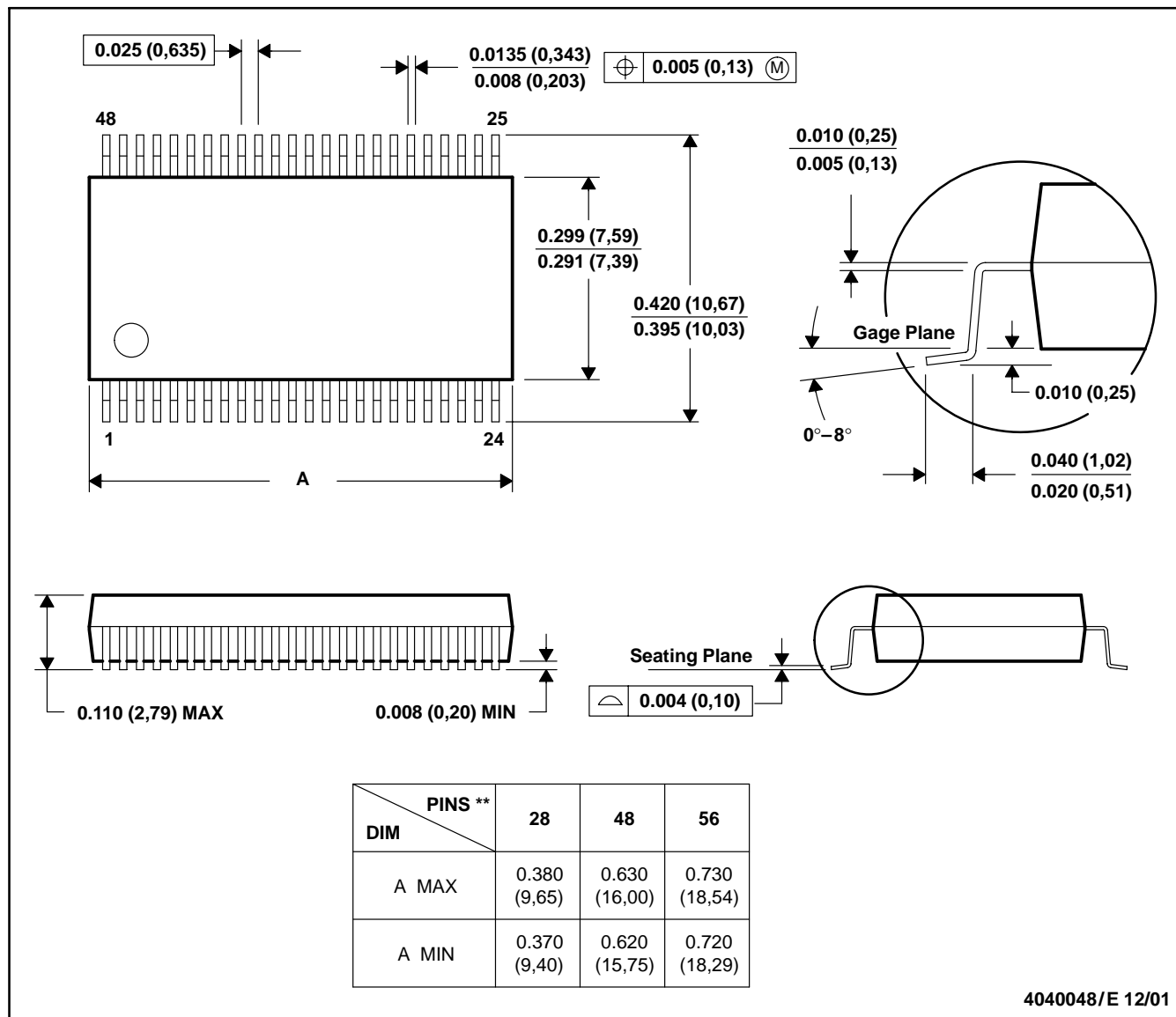
# MECHANICAL DATA

MSS0001C – JANUARY 1995 – REVISED DECEMBER 2001

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

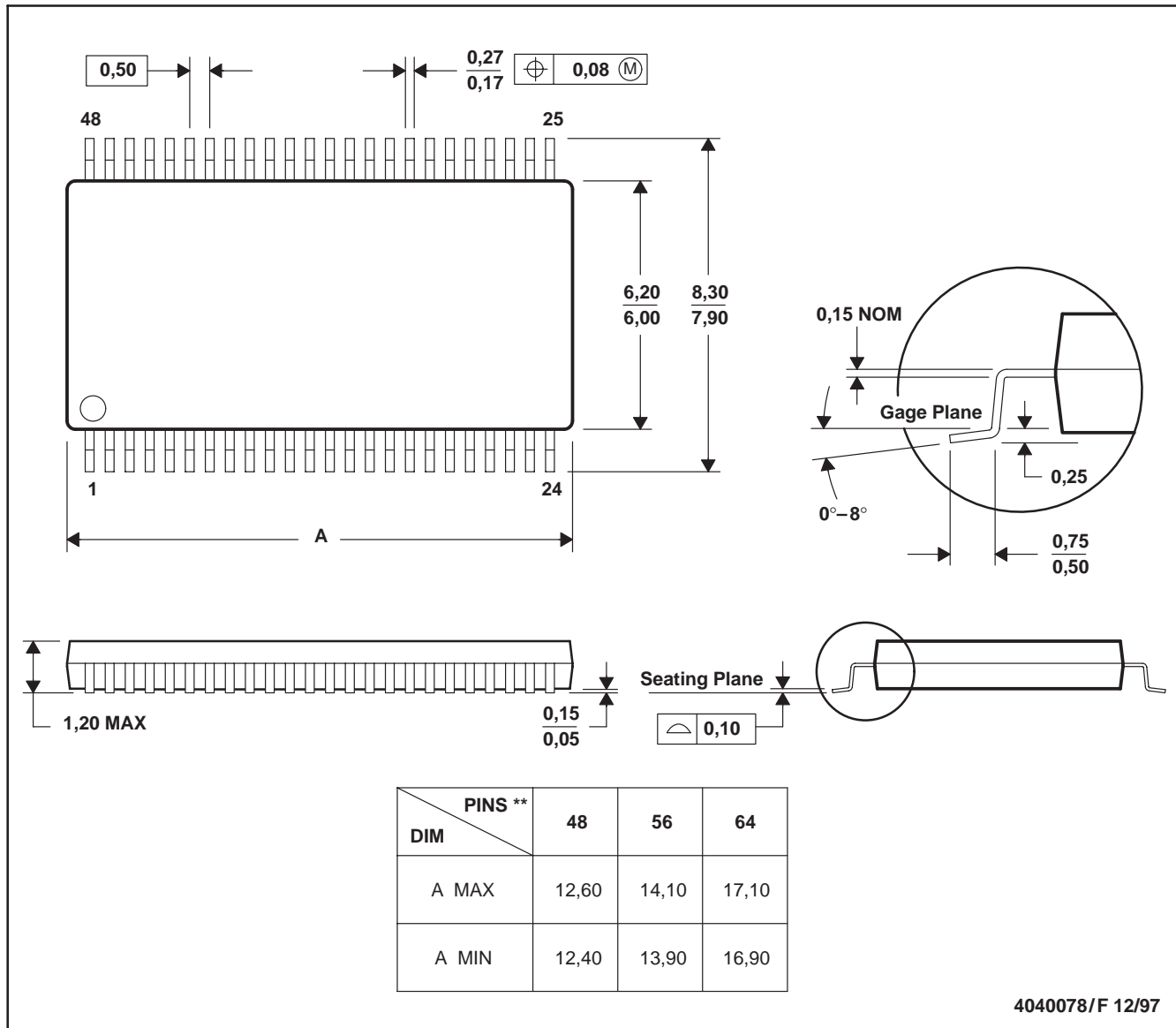
# MECHANICAL DATA

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265