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1.8-GHz, LOW DISTORTION, CURRENT FEEDBACK AMPLIFIER

FEATURES

- Unity Gain Bandwidth: 1.8 GHz
- High Slew Rate: 10500 V/μs
- Distortion at 100 MHz: (G = 10 V/V, R_L = 100 Ω, 2-V_{PP} envelope)
  - IMD_3: −80 dBc
  - OIP_3: 41 dBm
- Noise Figure : 11 dB (G = 10 V/V, R_G = 28 Ω, R_F = 255 Ω)
- Input Referred Noise (f > 10 MHz)
  - Voltage Noise: 1.65 nV/√Hz
  - Noninverting Current Noise: 13.4 pA/√Hz
  - Inverting Current Noise: 20 pA/√Hz
- Output Current: +115/−100 mA
- Power Supply Voltage Range: ±3.3 V to ±7.5 V

APPLICATIONS

- Arbitrary Waveform Driver
- High-Resolution, High-Sampling Rate ADC Drivers
- High-Resolution, High-Sampling Rate DAC Output Buffers
- If Amplification for Wireless Communications Applciations
- Broadcast Video and HDTV Line Drivers

DESCRIPTION

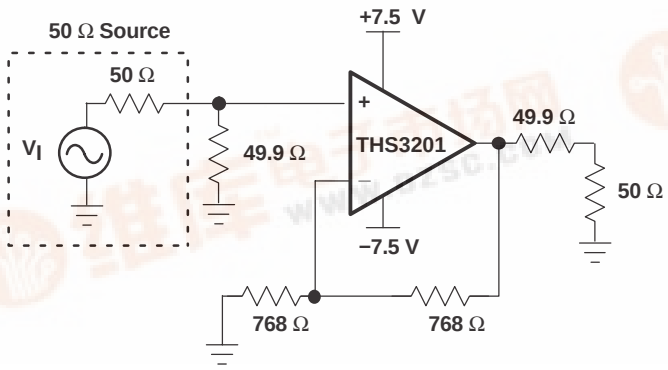
The THS3201 is a wide-band, high-speed current-feedback amplifier, designed to operate over a wide supply range of ±3.3 V to ±7.5 V for todays high performance applications.

The wide supply range combined with distortion as low as −74 dBc at 10 MHz, plus an extremely high slew rate of 10500 V/μs makes the THS3201 ideally suited for arbitrary waveform driver applications. The distortion performance also enables driving high-resolution and high-sampling rate ADCs. Moreover, the gain of +2 bandwidth of 850 MHz, combined with a 0.1 dB flatness of 380 MHz makes the THS3201 ideal for broadcast video and HDTV applications. The THS3201 also offers excellent performance for IF amplification in wireless communications systems by having IMD_3 performance of −80 dBc, OIP_3 of 41 dBm, and a noise figure of 11 dB, all at 100 MHz with a gain +10 V/V, while driving a 2-V_{PP} envelope into a 100-Ω load.

The THS3201 is offered in a 5-pin SOT−23, 8-pin SOIC, and an 8-pin MSOP with PowerPAD™ packages.

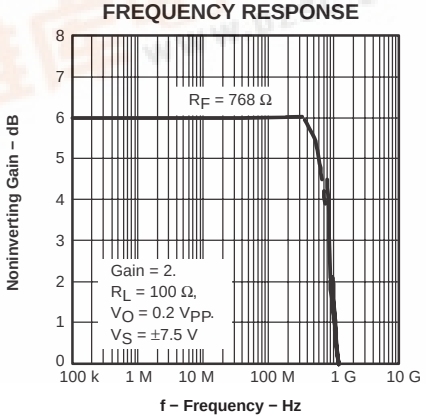
RELATED DEVICES AND DESCRIPTIONS	
THS3202	±7.5-V 2-GHz Dual Low Distortion CFB Amplifier
THS3001	±15-V 420-MHz Low Distortion CFB Amplifier
THS3061/2	±15-V 300-MHz Low Distortion CFB Amplifier
THS3122	±15-V Dual CFB Amplifier With 350 mA Drive
THS4271	±7.5-V 1.4-GHz Low Distortion VFB Amplifier

Low-Noise, Low-Distortion, Wideband Application Circuit



NOTE: Power supply decoupling capacitors not shown

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments Incorporated.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		UNIT
Supply voltage, V_S		16.5 V
Input voltage, V_I		±V_S
Output current, I_O (2)		175 mA
Differential input voltage, V_{ID}		±3 V
Continuous power dissipation		See Dissipation Rating Table
Maximum junction temperature, T_J (3)		150°C
Maximum junction temperature, continuous operation, long term reliability T_J (4)		125°C
Operating free-air temperature range, T_A		−40°C to 85°C
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300°C
ESD ratings:	HBM	3000 V
	CDM	1500 V
	MM	100 V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) The THS3201 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heat sink and must be connected to a thermally dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI technical briefs SLMA002 and SLMA004 for more information about utilizing the PowerPAD thermally enhanced package.

(3) The absolute maximum temperature under any condition is limited by the constraints of the silicon process.

(4) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC} (°C/W)	θ_{JA}(1) (°C/W)	POWER RATING(2) (T_J = 125°C)	
			$T_A \le 25°C$	T_A = 85°C
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
DGN (8)	4.7	58.4	1.71 W	685 mW
DGK (8 pin)	54.2	260	385 mW	154 mW

(1) This data was taken using the JEDEC standard High-K test PCB.

(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage	Dual supply	±3.3	±7.5	V
	Single supply	6.6	15	
Operating free-air temperature, T_A		−40	85	°C

PACKAGE/ORDERING INFORMATION

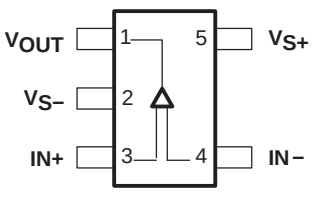
TEMPERATURE	PACKAGED DEVICES						
	PLASTIC SMALL OUTLINE (D)(1)	SOT-23(2)		PLASTIC MSOP(1) POWERPAD		PLASTIC MSOP(1)	
		(DBV)	SYM	(DGN)	SYM	(DGK)	SYM
−40°C to 85°C	THS3201D	THS3201DBVT	BEO	THS3201DGN	BEN	THS3201DGK	BGP
	THS3201DR	THS3201DBVR		THS3201DGNR		THS3201DGKR	

(1) Available in tape and reel. The R suffix standard quantity is 2500 (e.g. THS3201DGNR).

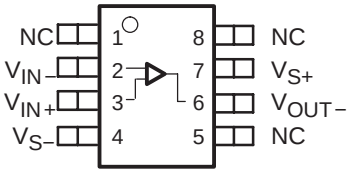
(2) Available in tape and reel. The R suffix standard quantity is 3000. The T suffix standard quantity is 250 (e.g. THS3201DBVT).

PIN ASSIGNMENTS

TOP VIEW — SOT−23



TOP VIEW — D, DGN, DGK



NC = No Internal Connection

NOTE: If a PowerPAD is used, it is electrically isolated from the active circuitry.

ELECTRICAL CHARACTERISTICS

V_S = ±7.5 V: R_f = 768 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS		THS3201					
			TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/TYP/MAX
AC PERFORMANCE								
Small-signal bandwidth, −3 dB (V_O = 200 mV_{PP})	G = +1, R_F= 1.2 kΩ		1.8				GHz	Typ
	G = +2, R_F = 768 Ω		850				MHz	Typ
	G = +5, R_F = 619 Ω		565					
	G = +10, R_F = 487 Ω		520					
Bandwidth for 0.1 dB flatness	G = +2, V_O = 200 mV_{pp}, R_F = 768 Ω		380				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 2 V_{pp}, R_F = 715 Ω		880				MHz	Typ
Slew rate (25% to 75% level)	G = +1, V_O = 5-V step		6200				V/µs	Typ
	G = +2, V_O = 10-V step		10500					
Rise and fall time	G = +2, V_O = 4-V step, R_F = 768 Ω		0.6				ns	Typ
Settling time to 0.1%	G = −2, V_O = 2-V step		20				ns	Typ
0.01%	G = −2, V_O = 2-V step		60					
Harmonic distortion	G = +5, f = 10 MHz, V_O = 2 V_{pp}							
2nd harmonic	R_L = 100 Ω		−75				dBc	Typ
	R_L = 500 Ω		−77					
3rd harmonic	R_L = 100 Ω		−91				dBc	Typ
	R_L = 500 Ω		−93					
Third-order intermodulation distortion (IMD_3)	G = +10, f_c = 100 MHz, Δf = 200 kHz, $V_{O(envelope)}$ = 2 V_{pp}		−80				dBc	Typ
Third-order output intercept point (OIP_3)			41				dBm	Typ
Noise figure	G = +10, f_c = 100 MHz, R_F = 255 Ω, R_G = 28		11				dB	Typ
Input voltage noise	f > 10 MHz		1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz		13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz		20				pA/√Hz	Typ
Differential gain	G = +2, R_L = 150 Ω, R_F = 768 Ω	NTSC	0.008%					Typ
		PAL	0.004%					Typ
Differential phase		NTSC	0.007°					Typ
		PAL	0.011°					Typ

DC PERFORMANCE							
Open-loop transimpedance gain	V_O = ±1 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} = 0 V	±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 0 V	±13	±60	±80	±85	µA	Max
Average bias current drift (−)	V_{CM} = 0 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 0 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 0 V			±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS

V_S = ±7.5 V: R_f = 768 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3201					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/TYP/MAX
INPUT							
Common-mode input range		±5.1	±5	±5	±5	V	Min
Common-mode rejection ratio	V_{CM} = ±3.75 V	71	60	58	58	dB	Min
Inverting input impedance, Z_{in}	Open loop	16				Ω	Typ
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±6	±5.9	±5.8	±5.8	V	Min
	R_L = 100 Ω	±5.8	±5.7	±5.5	±5.5		
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3.3	±3.3	±3.3	V	Min
Maximum operating voltage	Absolute maximum		±8.25	±8.25	±8.25	V	Max
Maximum quiescent current		14	18	21	21	mA	Max
Power supply rejection (+PSRR)	V_{S+} = 7 V to 8 V	69	63	60	60	dB	Min
Power supply rejection (−PSRR)	V_{S-} = −7 V to –8 V	65	58	55	55	dB	Min

ELECTRICAL CHARACTERISTICS

V_S = ±5 V: R_f = 715 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS		THS3201					
			TYP	OVER TEMPERATURE				
			25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/TYP/MAX
AC PERFORMANCE								
Small-signal bandwidth, −3dB (V_O = 200 mV_{PP})	G = +1, R_F= 1.2 kΩ		1.3				GHz	Typ
	G = +2, R_F = 715 Ω		725				MHz	Typ
	G = +5, R_F = 576 Ω		540					
	G = +10, R_F = 464 Ω		480					
Bandwidth for 0.1 dB flatness	G = +2, V_O = 200 mV_{pp}, R_F= 715 Ω		170				MHz	Typ
Large-signal bandwidth	G = +2, V_O = 2 V_{pp}, R_F= 715 Ω		900				MHz	Typ
Slew rate (25% to 75% level)	G = +1, V_O = 5-V step		5200				V/µs	Typ
	G = +2, V_O = 5-V step		5200					
Rise and fall time	G = +2, V_O = 4-V step, R_F= 715 Ω		0.7				ns	Typ
Settling time to 0.1%	G = −2, V_O = 2-V step		20				ns	Typ
0.01%	G = −2, V_O = 2-V step		60				ns	Typ
Harmonic distortion	G = +5, f = 10 MHz, V_O = 2 V_{pp}							
2nd harmonic	R_L = 100 Ω		−68				dBc	Typ
	R_L = 500 Ω		−70					
3rd harmonic	R_L = 100 Ω		−72				dBc	Typ
	R_L = 500 kΩ		−74					
Third-order intermodulation distortion (IMD_3)	G = +10, f_C = 100 MHz, Δf = 200 kHz, $V_{O(envelope)}$ = 2 V_{pp}		−65				dBc	Typ
Third-order output intercept point (OIP_3)			33.5				dBm	Typ
Noise figure	G = +10, f_C = 100 MHz, R_F = 255 Ω, R_G = 28		11				dB	Typ
Input voltage noise	f > 10 MHz		1.65				nV/√Hz	Typ
Input current noise (noninverting)	f > 10 MHz		13.4				pA/√Hz	Typ
Input current noise (inverting)	f > 10 MHz		20				pA/√Hz	Typ
Differential gain	G = +2, R_L = 150 Ω, R_F= 768 Ω	NTSC	0.006%					Typ
		PAL	0.004%					Typ
Differential phase		NTSC	0.03°					Typ
		PAL	0.04°					Typ

DC PERFORMANCE							
Open-loop transimpedance gain	V_O = +1 V, R_L = 1 kΩ	300	200	140	120	kΩ	Min
Input offset voltage	V_{CM} =0 V	±0.7	±3	±3.8	±4	mV	Max
Average offset voltage drift	V_{CM} = 0 V			±10	±13	µV/°C	Typ
Input bias current (inverting)	V_{CM} = 0 V	±13	±60	±80	±85	µA	Max
Average bias current drift (−)	V_{CM} = 0 V			±300	±400	nA/°C	Typ
Input bias current (noninverting)	V_{CM} = 0 V	±14	±35	±45	±50	µA	Max
Average bias current drift (+)	V_{CM} = 0 V			±300	±400	nA/°C	Typ

ELECTRICAL CHARACTERISTICS continued

V_S = ±5 V: R_f = 715 Ω, R_L = 100 Ω, and G = +2 unless otherwise noted

PARAMETER	TEST CONDITIONS	THS3201					
		TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	−40°C to 85°C	UNITS	MIN/TYP/MAX
INPUT							
Common-mode input range		±2.6	±2.5	±2.5	±2.5	V	Min
Common-mode rejection ratio	V_{CM} = ±2.5 V	71	60	58	58	dB	Min
Inverting input impedance, Z_{in}	Open loop	17.5				Ω	Typ
Input resistance	Noninverting	780				kΩ	Typ
	Inverting	11				Ω	Typ
Input capacitance	Noninverting	1				pF	Typ
OUTPUT							
Voltage output swing	R_L = 1 kΩ	±3.65	±3.5	±3.45	±3.4	V	Min
	R_L = 100 Ω	±3.45	±3.33	±3.25	±3.2		
Current output, sourcing	R_L = 20 Ω	115	105	100	100	mA	Min
Current output, sinking	R_L = 20 Ω	100	85	80	80	mA	Min
Closed-loop output impedance	G = +1, f = 1 MHz	0.01				Ω	Typ
POWER SUPPLY							
Minimum operating voltage	Absolute minimum		±3.3	±3.3	±3.3	V	Min
Maximum operating voltage	Absolute maximum		±8.25	±8.25	±8.25	V	Max
Maximum quiescent current		14	16.8	19	20	mA	Max
Power supply rejection (+PSRR)	V_{S+} = 4.5 V to 5.5 V	69	63	60	60	dB	Min
Power supply rejection (−PSRR)	V_{S-} = −4.5 V to –5.5 V	65	58	55	55	dB	Min

TYPICAL CHARACTERISTICS

Table of Graphs (V_S = ±7.5 V)

		FIGURE
Noninverting small signal frequency response		1, 2
Inverting small signal frequency response		3
Noninverting large signal frequency response		4
Inverting large signal frequency response		5
0.1 dB gain flatness frequency response		6
Capacitive load frequency response		7
Recommended switching resistance	vs Capacitive Load	8
2nd harmonic distortion	vs Frequency	9
3rd harmonic distortion	vs Frequency	10
Harmonic distortion	vs Output voltage swing	11, 12
Third-order intermodulation distortion (IMD_3)	vs Frequency	13
Third-order output intercept point (OIP_3)	vs Frequency	14
S − Parameter	vs Frequency	15, 16
Input voltage and current noise	vs Frequency	17
Noise figure	vs Frequency	18
Transimpedance	vs Frequency	19
Input offset voltage	vs Case Temperature	20
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Slew rate	vs Output voltage step	22, 23
Settling time		24, 25
Quiescent current	vs Supply voltage	26
Output voltage	vs Load resistance	27
Rejection ratio	vs Frequency	28
Noninverting small signal transient response		29
Inverting large signal transient response		30
Overdrive recovery time		31
Differential gain	vs Number of loads	32
Differential phase	vs Number of loads	33
Closed-loop output impedance	vs Frequency	34

Table of Graphs (V_S = ±5 V)

		FIGURE
Noninverting small signal frequency response		35
Inverting small signal frequency response		36
		37
2nd harmonic distortion	vs Frequency	38
3rd harmonic distortion	vs Frequency	39
Harmonic distortion	vs Output voltage swing	40, 41
Third-order intermodulation distortion (IMD_3)	vs Frequency	42
Third-order output intercept point (OIP_3)	vs Frequency	43
S − Parameter	vs Frequency	44, 45
Slew rate	vs Output voltage step	46
Noninverting small signal transient response		47
Inverting large signal transient response		48
Overdrive recovery time		49

V_S = ±7.5 V Graphs

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

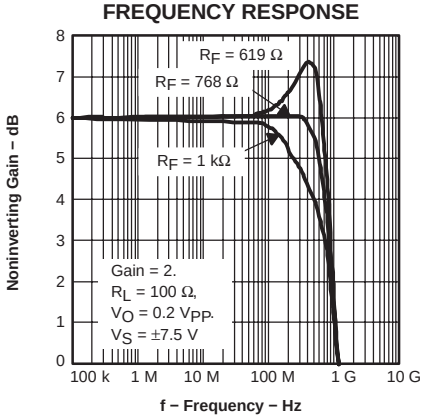


Figure 1

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

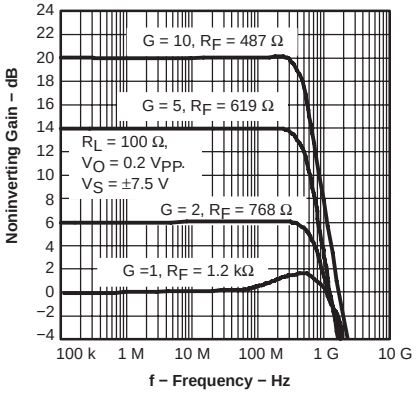


Figure 2

INVERTING SMALL SIGNAL FREQUENCY RESPONSE

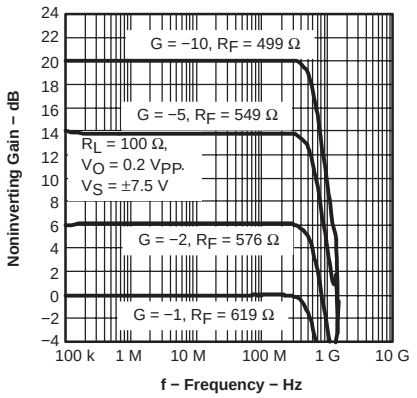


Figure 3

INVERTING LARGE SIGNAL FREQUENCY RESPONSE

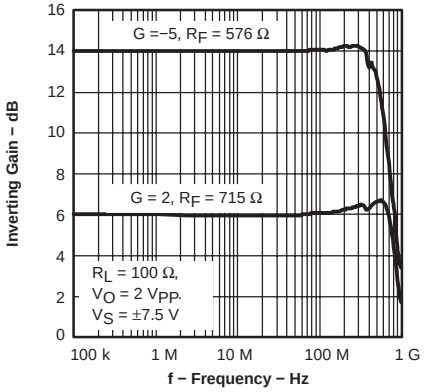


Figure 4

INVERTING LARGE SIGNAL FREQUENCY RESPONSE

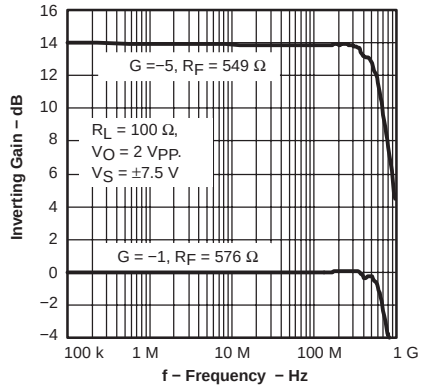


Figure 5

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

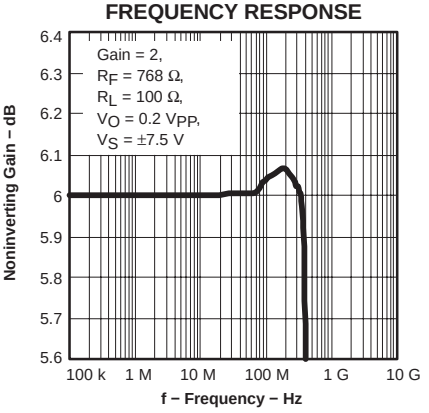


Figure 6

CAPACITIVE LOAD FREQUENCY RESPONSE

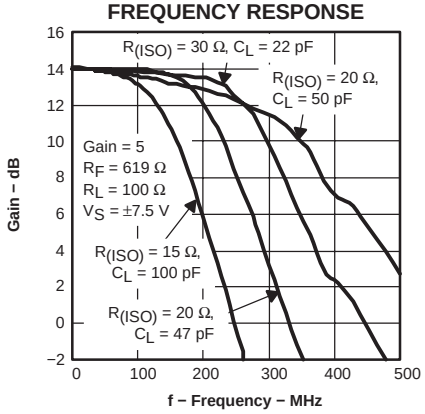


Figure 7

RECOMMENDED R_{ISO} VS CAPACTIVE LOAD

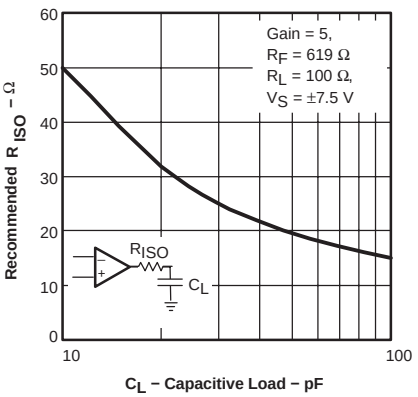


Figure 8

2nd HARMONIC DISTORTION VS FREQUENCY

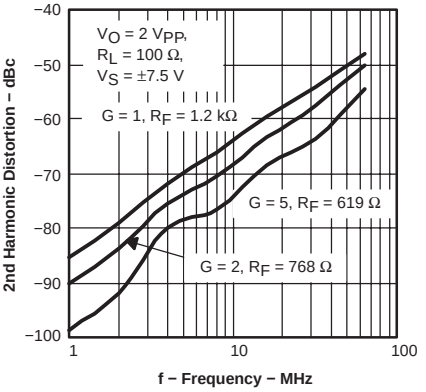


Figure 9

3rd HARMONIC DISTORTION vs FREQUENCY

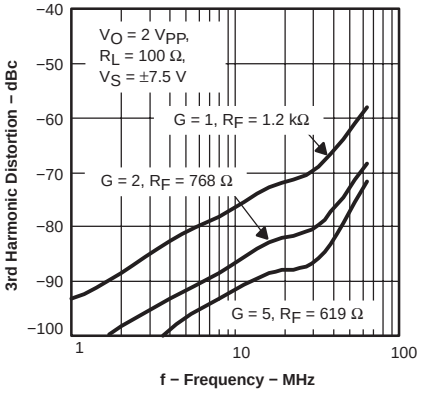


Figure 10

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

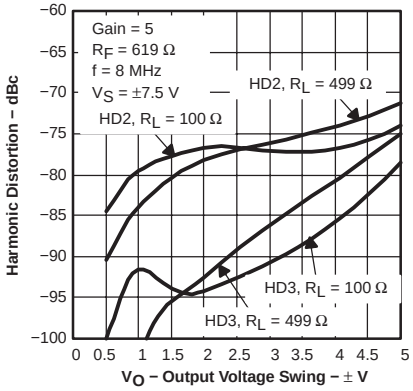


Figure 11

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

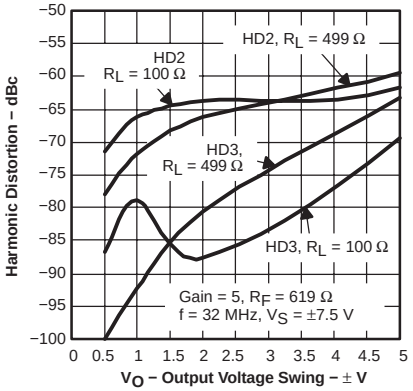


Figure 12

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

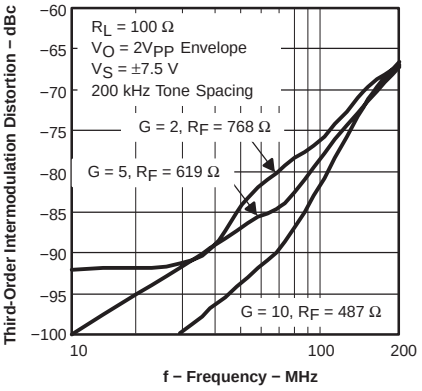


Figure 13

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

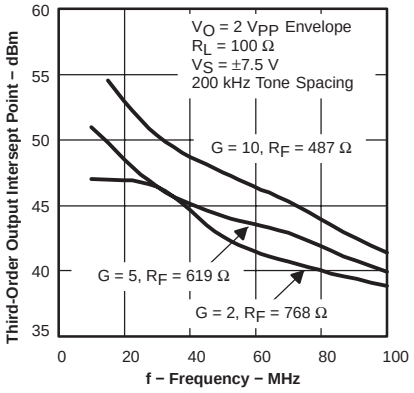


Figure 14

S − PARAMETER vs FREQUENCY

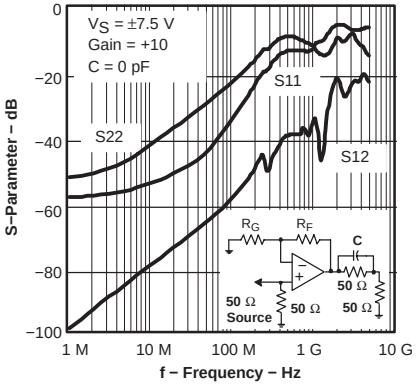


Figure 15

S − PARAMETER vs FREQUENCY

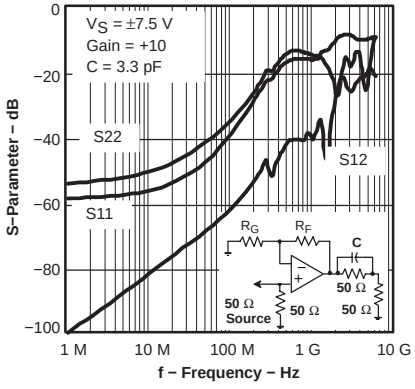


Figure 16

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

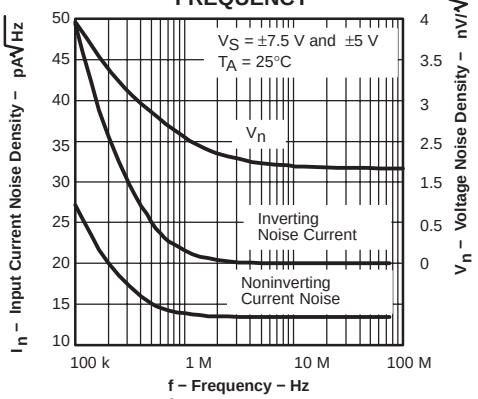


Figure 17

NOISE FIGURE vs FREQUENCY

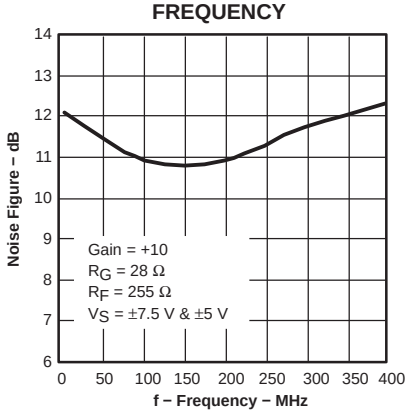


Figure 18

TRANSIMPEDANCE vs FREQUENCY

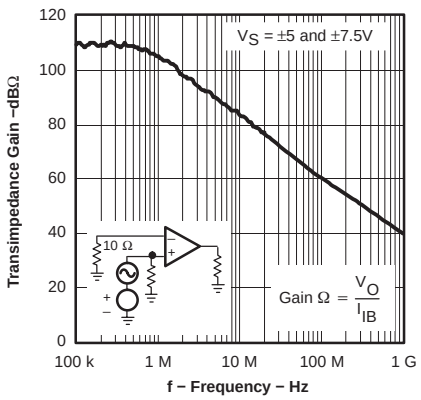


Figure 19

INPUT OFFSET VOLTAGE vs CASE TEMPERATURE

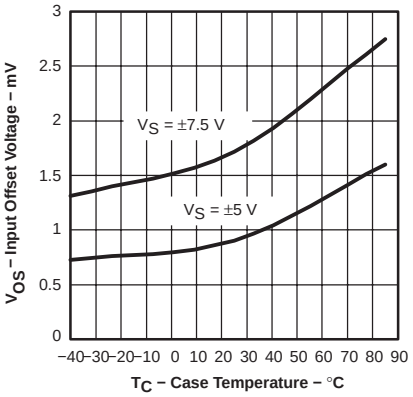


Figure 20

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

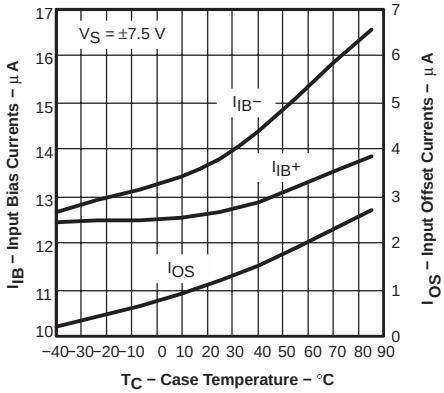


Figure 21

SLEW RATE vs OUTPUT VOLTAGE

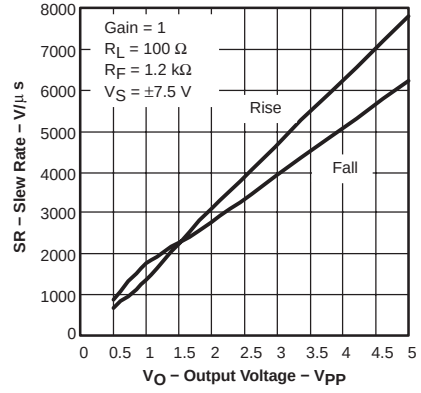


Figure 22

SLEW RATE vs OUTPUT VOLTAGE

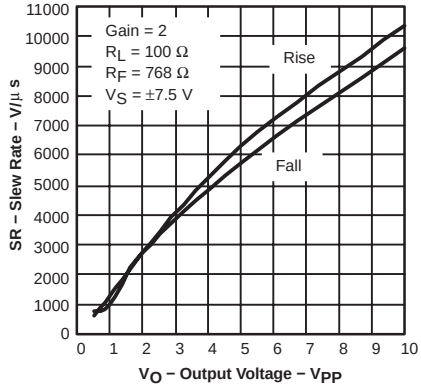


Figure 23

SETTLING TIME

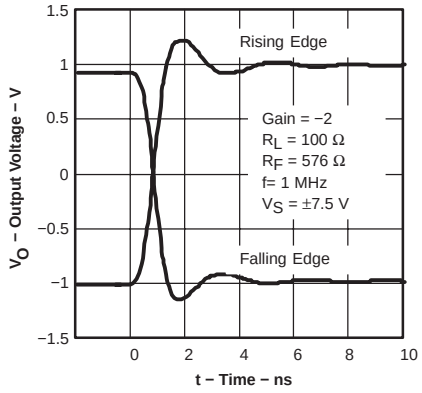


Figure 24

SETTLING TIME

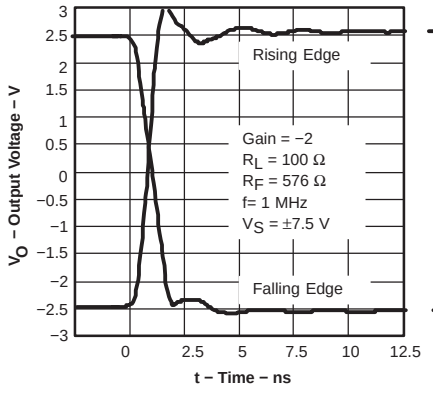


Figure 25

QUIESCENT CURRENT vs SUPPLY VOLTAGE

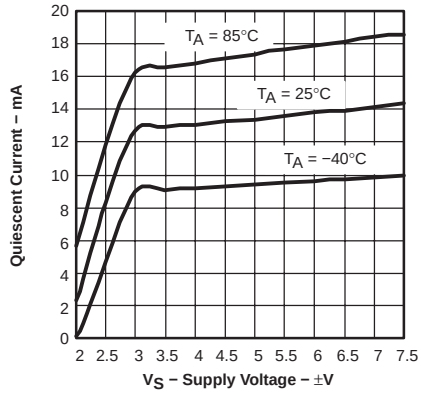


Figure 26

OUTPUT VOLTAGE vs LOAD RESISTANCE

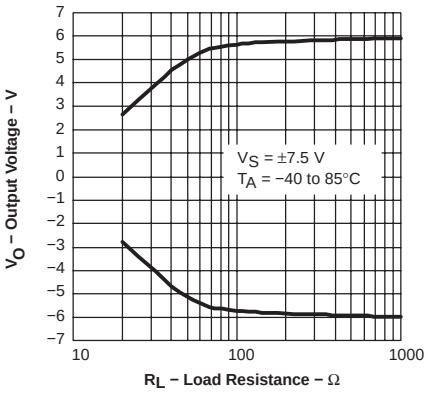


Figure 27

REJECTION RATIO vs FREQUENCY

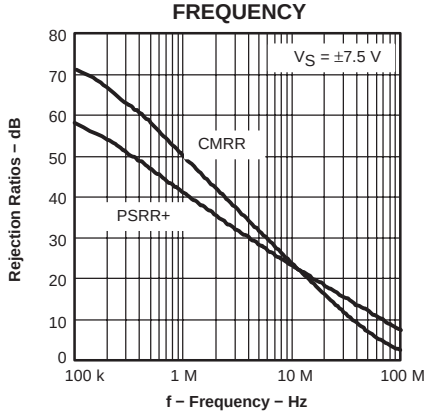


Figure 28

NONINVERTING SMALL-SIGNAL TRANSIENT RESPONSE

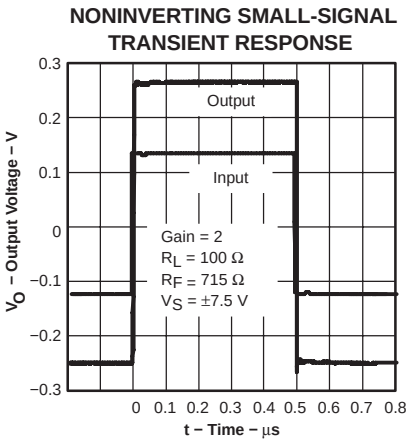


Figure 29

INVERTING LARGE-SIGNAL TRANSIENT RESPONSE

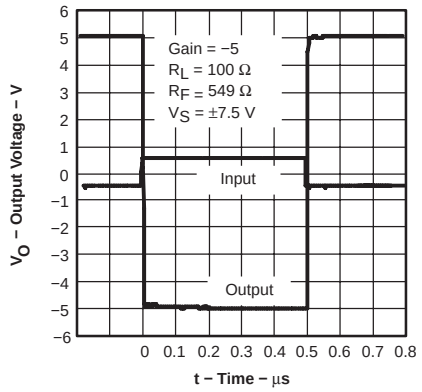


Figure 30

OVERDRIVE RECOVERY TIME

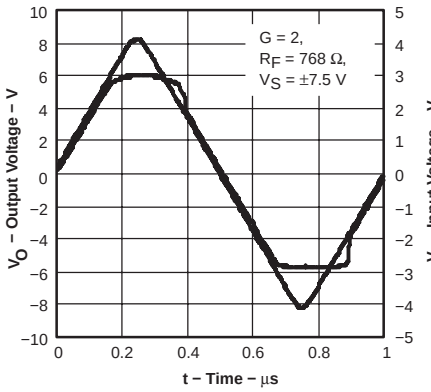


Figure 31

DIFFERENTIAL GAIN vs NUMBER OF LOADS

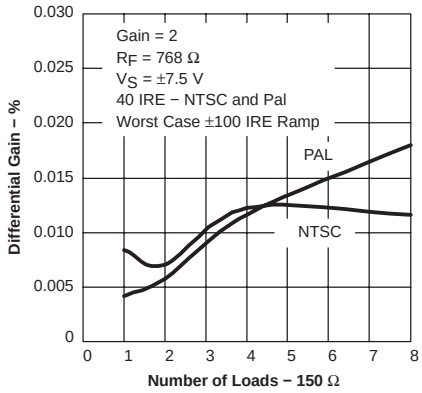


Figure 32

DIFFERENTIAL PHASE vs NUMBER OF LOADS

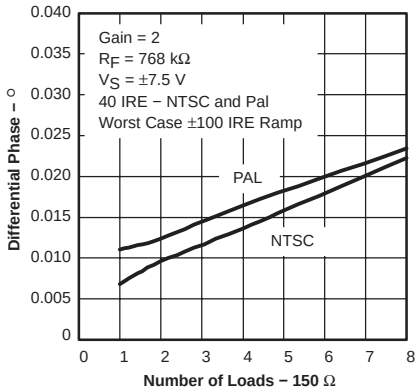


Figure 33

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

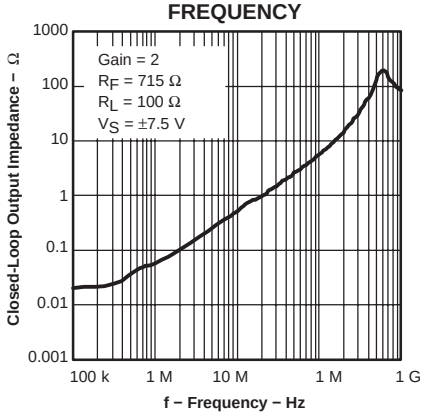


Figure 34

V_S = ±5 V Graphs

NONINVERTING SMALL SIGNAL FREQUENCY RESPONSE

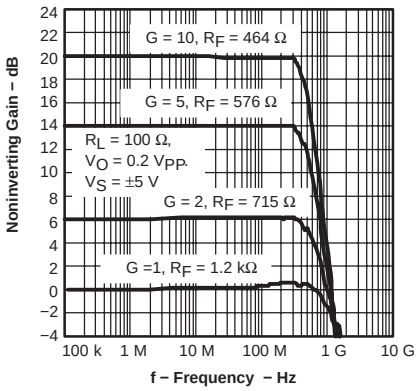


Figure 35

INVERTING SMALL SIGNAL FREQUENCY RESPONSE

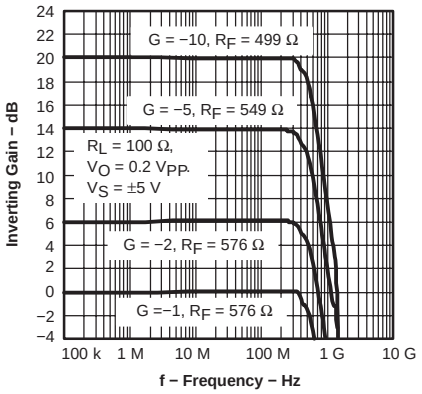


Figure 36

0.1 dB GAIN FLATNESS FREQUENCY RESPONSE

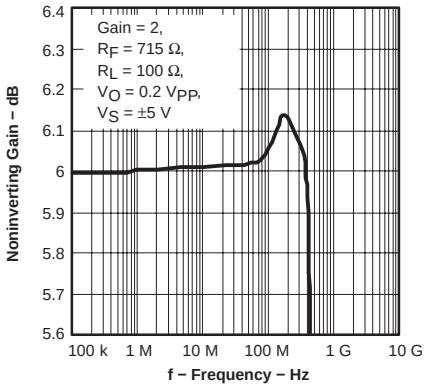


Figure 37

2nd HARMONIC DISTORTION vs FREQUENCY

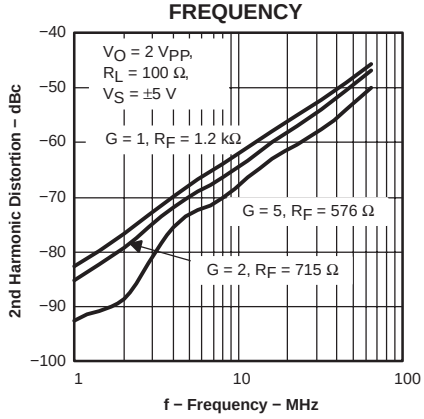


Figure 38

3rd HARMONIC DISTORTION vs FREQUENCY

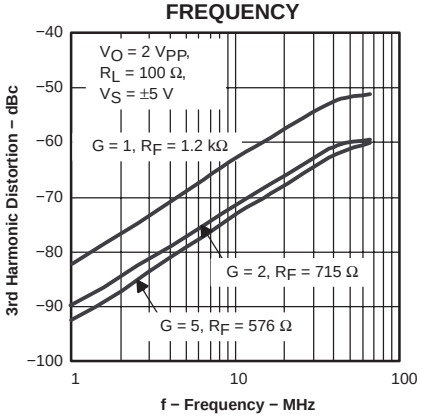


Figure 39

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

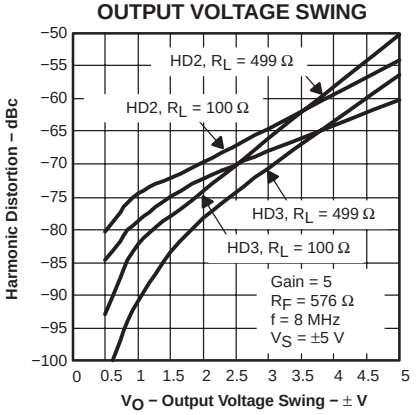


Figure 40

HARMONIC DISTORTION vs OUTPUT VOLTAGE SWING

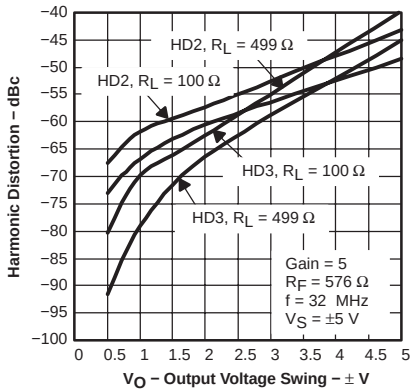


Figure 41

THIRD-ORDER INTERMODULATION DISTORTION vs FREQUENCY

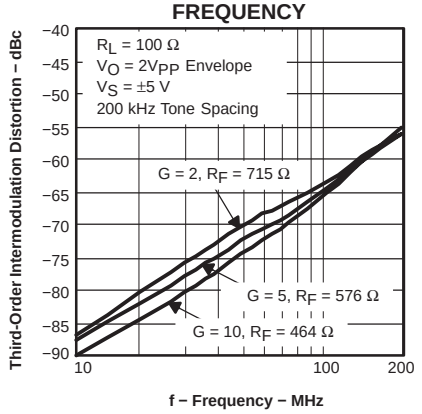


Figure 42

THIRD-ORDER OUTPUT INTERCEPT POINT vs FREQUENCY

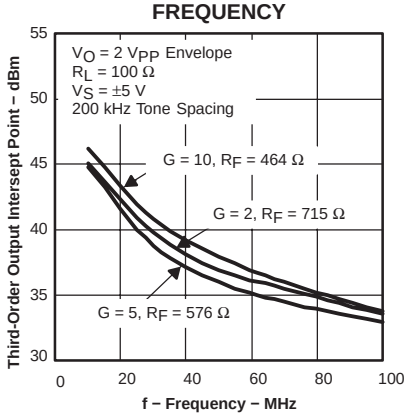


Figure 43

S − PARAMETER vs FREQUENCY

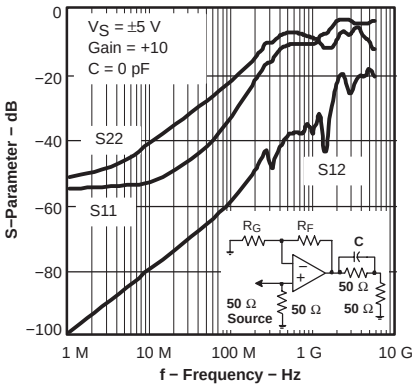


Figure 44

S − PARAMETER vs FREQUENCY

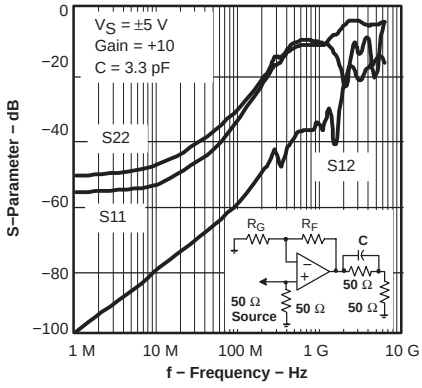


Figure 45

SLEW RATE vs OUTPUT VOLTAGE

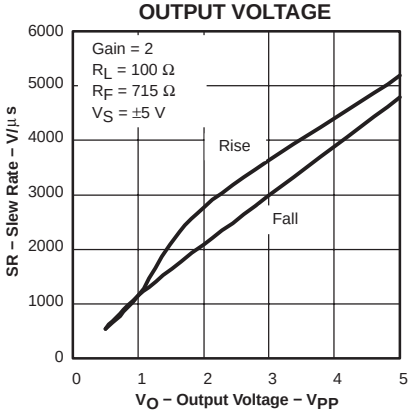


Figure 46

NONINVERTING SMALL-SIGNAL TRANSIENT RESPONSE

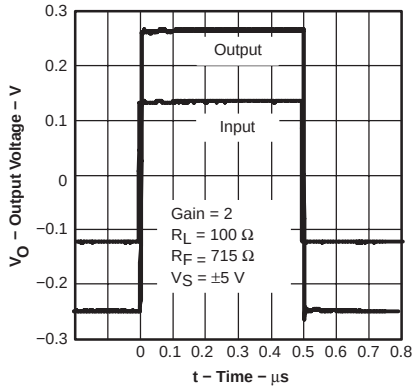


Figure 47

INVERTING LARGE-SIGNAL TRANSIENT RESPONSE

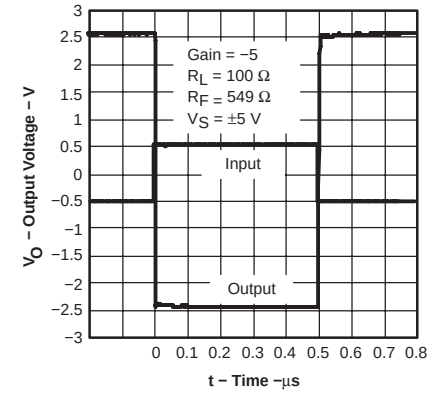


Figure 48

OVERDRIVE RECOVERY TIME

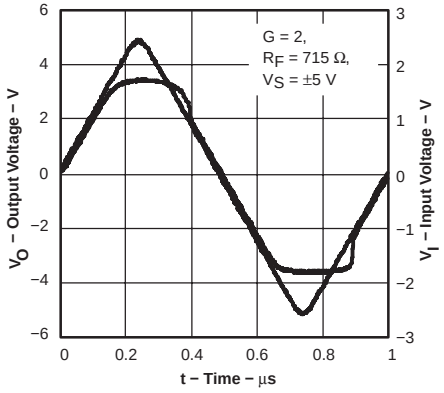


Figure 49

APPLICATION INFORMATION

WIDEBAND, NONINVERTING OPERATION

The THS3201 is a unity gain stable 1.8-GHz current-feedback operational amplifiers, designed to operate from a ±3.3-V to ±7.5-V power supply.

Figure 50 shows the THS3201 in a noninverting gain of 2V/V configuration typically used to generate the performance curves. Most of the curves were characterized using signal sources with 50-Ω source impedance, and with measurement equipment presenting a 50-Ω load impedance. The 49.9-Ω shunt resistor at the V_I terminal in Figure 50 matches the source impedance of the test generator.

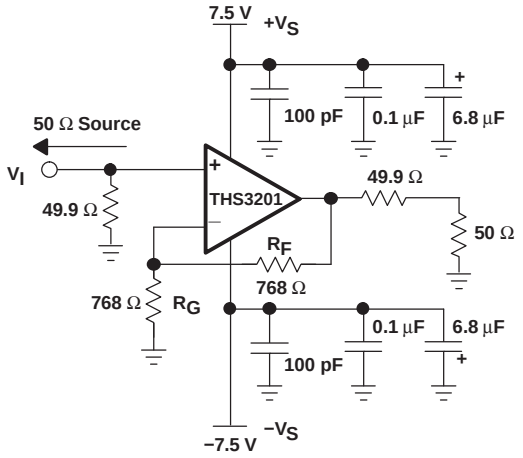


Figure 50. Wideband, Noninverting Gain Configuration

Unlike voltage-feedback amplifiers, current-feedback amplifiers are highly dependent on the feedback resistor R_F for maximum performance and stability. Table 1 shows the optimal gain setting resistors R_F and R_G at different gains to give maximum bandwidth with minimal peaking in the frequency response. Higher bandwidths can be achieved, at the expense of added peaking in the frequency response, by using even lower values for R_F. Conversely, increasing R_F decreases the bandwidth, but stability is improved.

Table 1. Recommended Resistor Values for Optimum Frequency Response

THS3201 R_F for AC When R_{load} = 100 Ω			
Gain (V/V)	Supply Voltage (V)	R_G (Ω)	R_F (Ω)
1	±7.5	—	1.2 k
	±5	—	1.2 k
2	±7.5	768	768
	±5	715	715
5	±7.5	154.9	619
	±5	143	576
10	±7.5	54.9	487
	±5	51.1	464
−1	±7.5	619	619
	±5	576	576
−2	±7.5 and ±5	287	576
−5	±7.5 and ±5	110	549
−10	±7.5 and ±5	49.9	499

WIDEBAND, INVERTING GAIN OPERATION

Figure 51 shows the THS3201 is a typical inverting gain configuration where the input and output impedances and signal gain from Figure 50 are retained in an inverting circuit configuration.

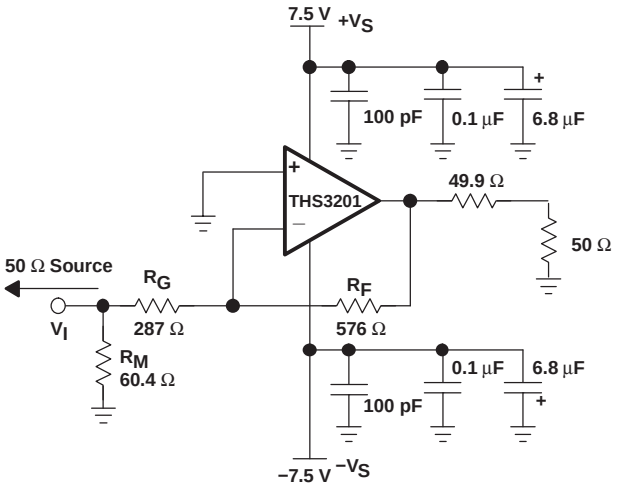


Figure 51. Wideband, Inverting Gain Configuration

SINGLE SUPPLY OPERATION

The THS3201 has the capability to operate from a single supply voltage ranging from 6.6V to 15V. When operating from a single power supply, care must be taken to ensure the input signal and amplifier is biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 52 demonstrate methods to configure an amplifier in a manner conducive for single supply operation

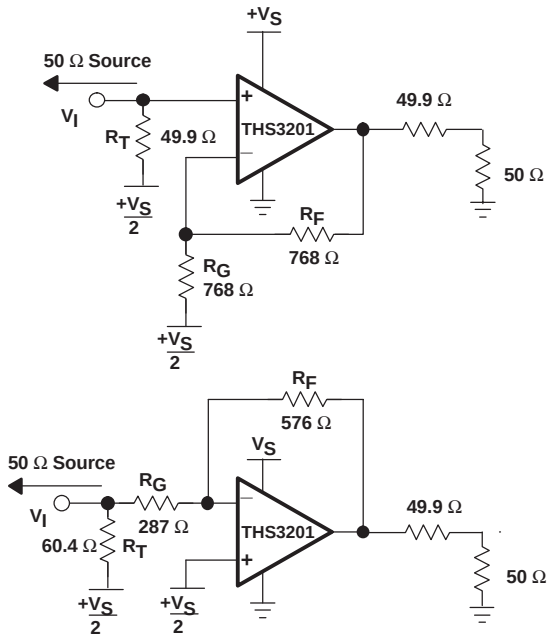


Figure 52. DC-Coupled Single Supply Operation

VIDEO AND HDTV DRIVERS

The exceptional bandwidth and slew rate of the THS3201 matches the demands for professional video and HDTV. Most commercial HDTV standards requires a video passband of 30-MHz. To ensure high signal quality with minimal degradation of performance, a 0.1-dB gain flatness should be at least 7x the passband frequency to minimize group delay variations—requiring 210-MHz 0.1-dB frequency flatness from the amplifier. High slew rates ensures there is minimal distortion of the video signal. Component video and RGB video signals require fast transition times and fast settling times to keep a high signal quality. The THS8135, for example, is a 240 MSPS video DAC and has a transition time approaching 4-ns. The THS3201 is a perfect candidate for interfacing the output of such high-performance video components.

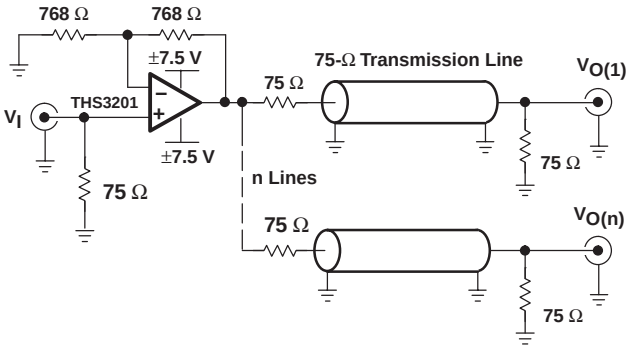


Figure 53. Video Distribution Amplifier Application

ADC DRIVER APPLICATION

The THS3201 can be used as a high-performance ADC driver in applications like radio receiver IF stages, and test and measurement devices. All high-performance ADCs have differential inputs. The THS3201 can be used in conjunction with a transformer as a drive amplifier in these applications. Figure 54 and Figure 55 show two different approaches.

In Figure 54, a transformer is used after the amplifier to convert the signal to differential. The advantage of this approach is fewer components are required. R_{OUT} and R_T are required for impedance matching the transformer.

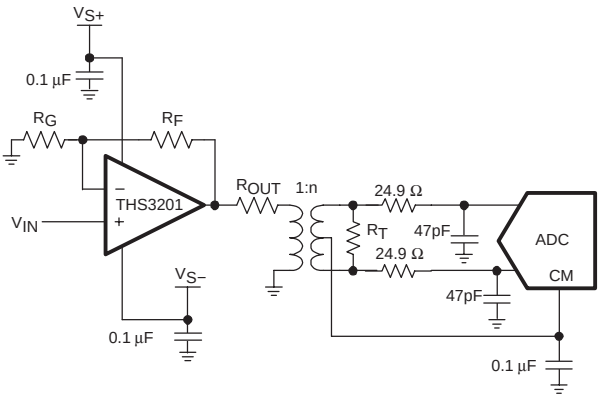


Figure 54. Differential ADC Driver Circuit 1

In Figure 55, a transformer is used before two amplifiers to convert the signal to differential. The two amplifiers then amplify the differential signal. The advantage to this approach is each amplifier is required to drive half the voltage as before. R_T is used to impedance match the transformer.

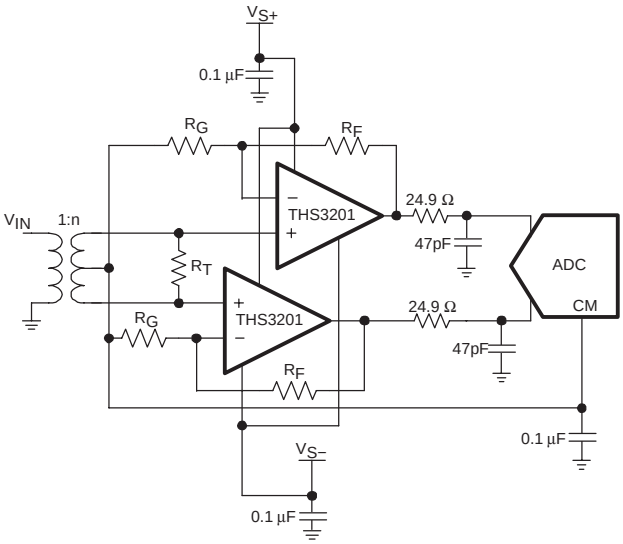


Figure 55. Differential ADC Driver Circuit 2

It is almost universally recommended to use a resistor and capacitor between the op amp's output and the ADC's input as shown in both Figures.

This resistor-capacitor (RC) combination has multiple functions:

- The capacitor is a local charge reservoir for ADC
- The resistor isolates the amplifier from the ADC
- In conjunction, they form a low-pass noise filter

During the sampling phase, current is required to charge the ADC's input sampling capacitors. By placing external capacitors directly at the input pins, most of the current is drawn from them. They are seen as a very low impedance source. They can be thought of as serving much the same purpose as a power supply bypass capacitor; to supply transient current, with the amplifier then providing the bulk charge.

Typically, a low-value capacitor in the range of 10 pF to 100 pF provides the required transient charge reservoir.

The capacitance and the switching action of the ADC is one of the worst loading scenarios that a high-speed amplifier encounters. The resistor provides a simple means of isolating the associated phase shift from the feedback network and maintaining the phase margin of the amplifier.

Typically, a low value resistor in the range of 10 Ω to 100 Ω provides the required isolation. Together, the R and C form a real pole in the s-plane located at the frequency:

$$f_P = \frac{1}{2\pi RC}$$

Placing this pole at about 10x the highest frequency of interest insures it has no impact on the signal. Since the resistor is typically a small value, it is very bad practice to place the pole at (or very near) frequencies of interest. At the pole frequency, the amplifiers sees a load with a magnitude of:

$$\sqrt{2}\,xR$$

If R is only 10 Ω, the amplifier is very heavily loaded above the pole frequency, and generates excessive distortion.

DAC DRIVER APPLICATION

The THS3201 can be used as a high-performance DAC output driver in applications like radio transmitter stages, and arbitrary waveform generators. All high-performance DACs have differential current outputs. Two THS3201s can be used as a differential drive amplifier in these applications as shown in Figure 56.

R_{PU} on the DAC output is used to convert the output current to voltage. The 24.9-Ω resistor and 47-pF capacitor between each DAC output and the op amp input is used to reduce the images generated at multiples of the sampling rate. The values shown form a pole a 136 MHz. R_{OUT} sets the output impedance of each amplifier.

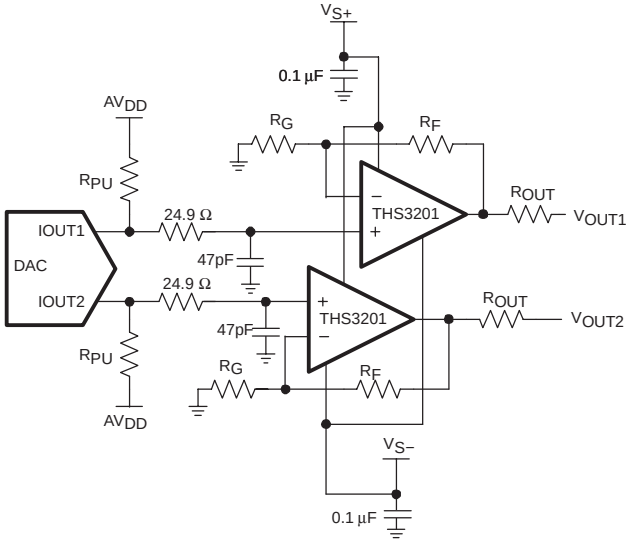


Figure 56. Differential DAC Driver Circuit

POWER SUPPLY

The performance of the THS3201 is dependent upon the power supply. Slew rate, bandwidth, and distortion are graphed against the power supply to highlight this dependence. As the power supply is increased from ±5 V to ±7.5 V, the slew rate increases, the bandwidth increases, and the distortion improves.

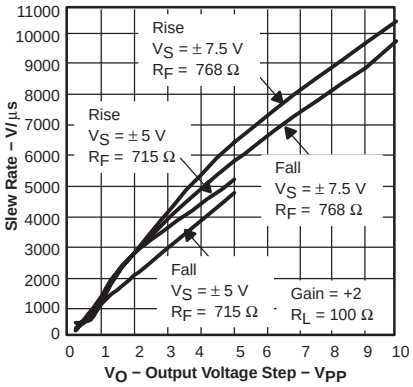


Figure 57. Slew Rate vs Output Voltage Step

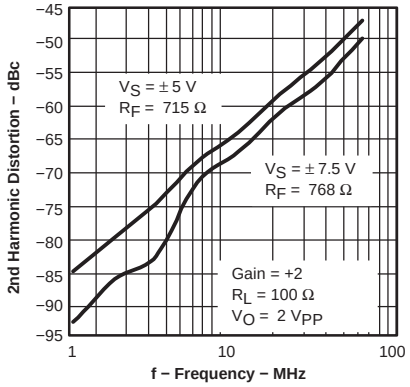


Figure 58. 2nd Harmonic Distortion vs Frequency

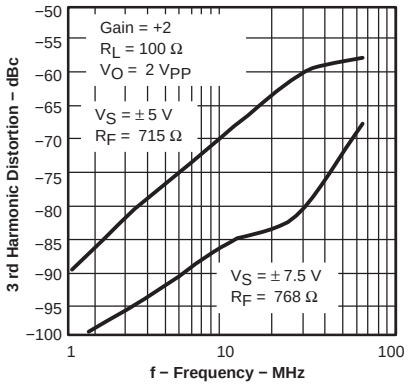


Figure 59. 3rd Harmonic Distortion vs Frequency

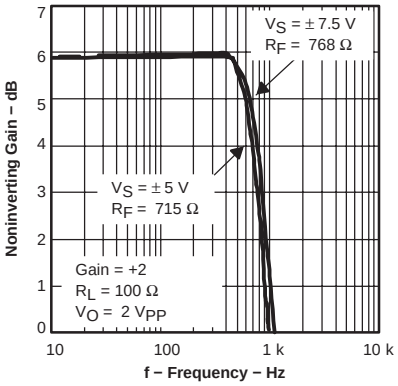


Figure 60. Noninverting Small Signal Frequency Response

PRINTED-CIRCUIT BOARD LAYOUT TECHNIQUES FOR OPTIMAL PERFORMANCE

Achieving optimum performance with high frequency amplifier-like devices in the THS3201 requires careful attention to board layout parasitic and external component types.

Recommendations that optimize performance include:

- Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and input pins can cause instability. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.
- Minimize the distance (< 0.25") from the power supply pins to high frequency 0.1-μF and 100 pF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (6.8 μF or more) tantalum decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board. The primary goal is to minimize the impedance seen in the differential-current return paths. For driving differential loads with the THS3201, adding a capacitor between the power supply pins improves 2nd order harmonic distortion performance. This also minimizes the current loop formed by the differential drive.
- Careful selection and placement of external components preserve the high frequency performance of the THS3201. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Again, keep their leads and PC board trace length as short as possible. Never use wirebound type resistors in a high frequency application. Since the output pin and inverting input pins are the most sensitive to parasitic capacitance, always position the feedback and series output resistors, if any, as close as possible to the inverting input pins and output pins. Other network components, such as input termination resistors, should be placed close to the gain-setting resistors. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero that can effect circuit operation. Keep resistor values as low as possible, consistent with load driving considerations.
- Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and determine if isolation resistors on the outputs are necessary. Low parasitic capacitive loads (< 4 pF) may not need an R_S since the THS3201 is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques).

  A 50-Ω environment is not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in the distortion versus load plots. With a characteristic board trace impedance based on board material and trace dimensions, a matching series resistor into the trace from the output of the THS3201 is used as well as a terminating shunt resistor at the input of the destination device.

  Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case. This does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.
- Socketing a high speed part like the THS3201 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the THS3201 parts directly onto the board.

PowerPAD DESIGN CONSIDERATIONS

The THS3201 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted [see Figure 61(a) and Figure 61(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 61(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the, heretofore, awkward mechanical methods of heatsinking.

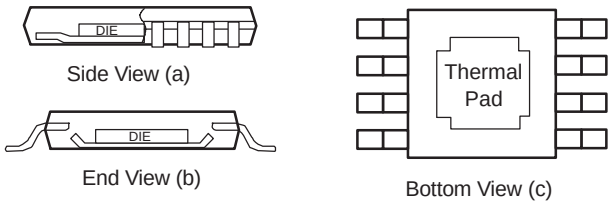


Figure 61. Views of Thermally Enhanced Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

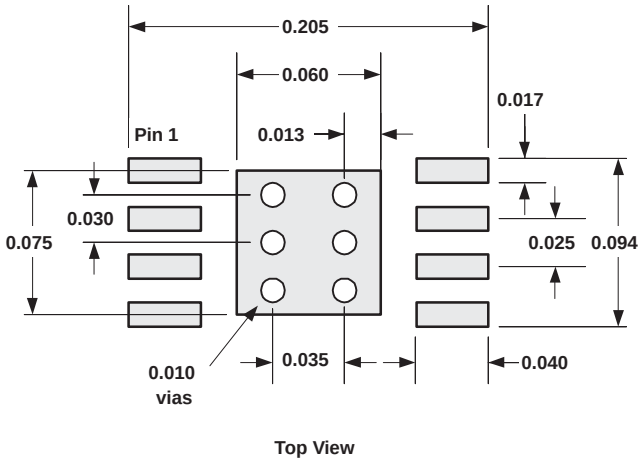


Figure 62. DGN PowerPAD PCB Etch and Via Pattern

PowerPAD PCB LAYOUT CONSIDERATIONS

1. Prepare the PCB with a top side etch pattern as shown in Figure 62. There should be etch for the leads as well as etch for the thermal pad.

2. Place five holes in the area of the thermal pad. These holes should be 10 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the THS3201 IC. These additional vias may be larger than the 10-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.

4. Connect all holes to the internal ground plane.

5. When connecting these holes to the ground plane, **do not** use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS3201 PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.

6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.

7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

8. With these preparatory steps in place, the IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

POWER DISSIPATION AND THERMAL CONSIDERATIONS

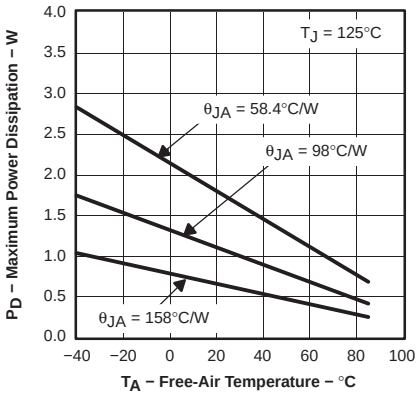
To maintain maximum output capabilities, the THS3201 does not incorporate automatic thermal shutoff protection. The designer must take care to ensure that the design does not violate the absolute maximum junction temperature of the device. Failure may result if the absolute maximum junction temperature of 150°C is exceeded. For best performance, design for a maximum junction temperature of 125°C. Between 125°C and 150°C, damage does not occur, but the performance of the amplifier begins to degrade.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:
P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

For systems where heat dissipation is more critical, the THS3201 is offered in an 8-pin MSOP with PowerPAD and the THS3201 is available in the SOIC−8 PowerPAD package offering even better thermal performance. The thermal coefficient for the PowerPAD packages are substantially improved over the traditional SOIC. Maximum power dissipation levels are depicted in the graph for the available packages. The data for the PowerPAD packages assume a board layout that follows the PowerPAD layout guidelines referenced above and detailed in the PowerPAD application note number SLMA002. The following graph also illustrates the effect of not soldering the PowerPAD to a PCB. The thermal impedance increases substantially which may cause serious heat and performance issues. Be sure to always solder the PowerPAD to the PCB for optimum performance.



Results are With No Air Flow and PCB Size = 3”x3”
θ_{JA} = 58.4°C/W for 8-Pin MSOP w/PowerPad (DGN)
θ_{JA} = 98°C/W for 8-Pin SOIC High Test PCB (D)
θ_{JA} = 158°C/W for 8-Pin MSOP w/PowerPad w/o Solder

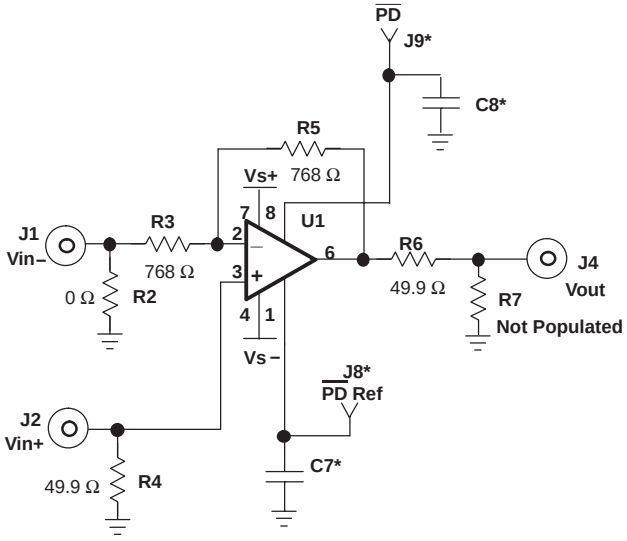
Figure 63. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to not only consider quiescent power dissipation, but also dynamic power dissipation. Often times, this is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

DESIGN TOOLS

Evaluation Fixture, Spice Models, and Applications Support

Texas Instruments is committed to providing its customers with the highest quality of applications support. To support this goal an evaluation board has been developed for the THS3201 operational amplifier. The board is easy to use, allowing for straightforward evaluation of the device. The evaluation board can be ordered through the Texas Instruments web site, www.ti.com, or through your local Texas Instruments sales representative. The schematic diagram, board layers, and bill of materials of the evaluation boards are provided below.



***Does Not Apply to the THS3201**

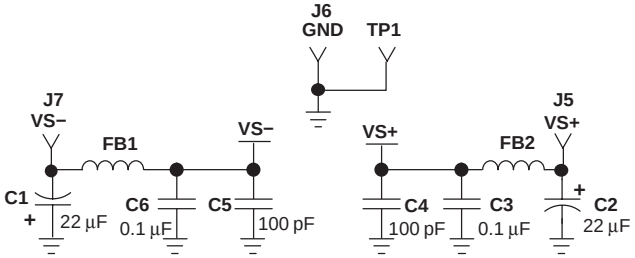


Figure 64. THS3201 EVM Circuit Configuration

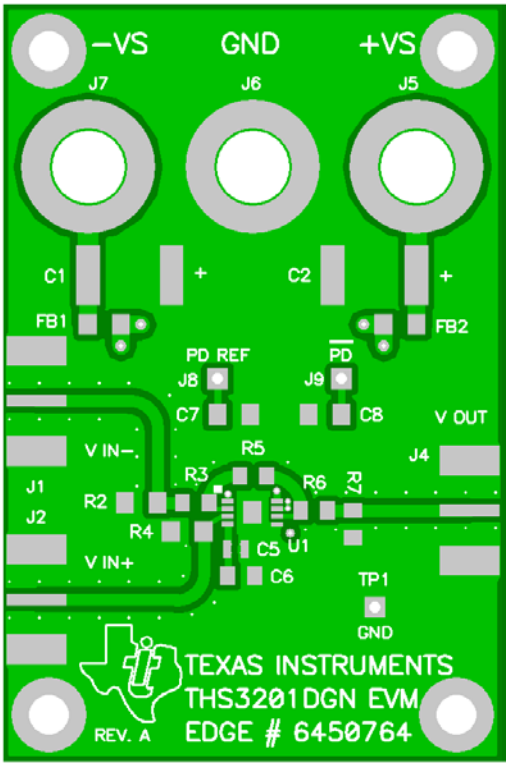


Figure 65. THS3201 EVM Board Layout (Top Layer)

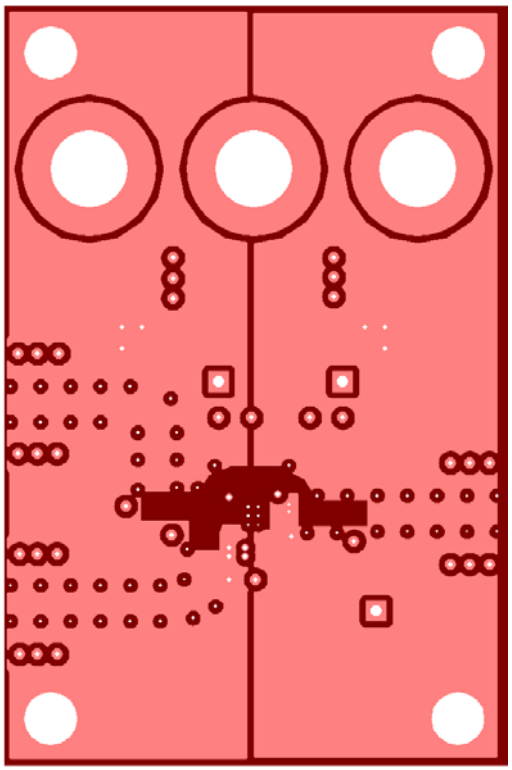


Figure 67. THS3201 EVM Board Layout (Third Layer, Power)

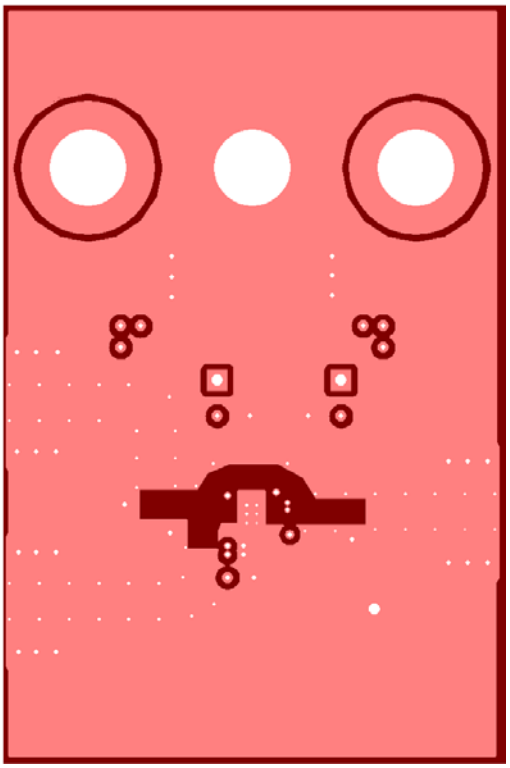


Figure 66. THS3201 EVM Board Layout (Second Layer, Ground)

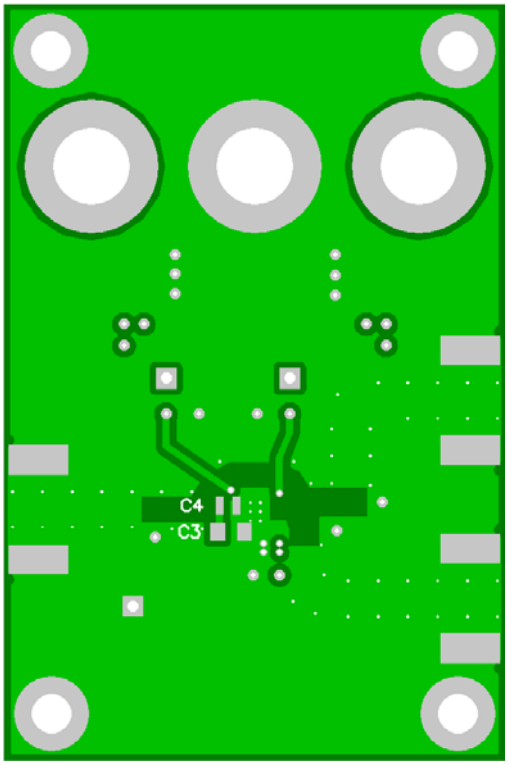


Figure 68. THS3201 EVM Board Layout (Bottom Layer)

Table 2. Bill of Materials

THS3201DGN EVM					
Item	**Description**	**SMD Size**	**Ref Des**	**PCB Quantity**	**Manufacturer's Part Number**
1	Bead, ferrite, 3 A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R−00
2	Cap, 22 µF, tanatalum, 25V, 10%	D	C1, C2	2	(AVX) TAJD226K025R
3	Cap, 100 pF, ceramic, 5%, 150V	AQ12	C4, C5	2	(AVX) AQ12EM101JAJME
4	Cap, 0.1 µF, ceramic, X7R, 50V	0805	C3, C6	2	(AVX) 08055C104KAT2A
6	Open	0805	R7	1	
7	Resistor, 49.9 Ω, 1/8W, 1%	0805	R6	1	(Phycomp) 9C08052A49R9FKHFT
9	Resistor, 768 Ω, 1/8W, 1%	0805	R3, R5	2	(Phycomp) 9C08052A7680FKHFT
10	Open	1206	C7, C8	2	
11	Resistor, 0 Ω, 1/4W, 1%	1206	R2	1	(KOA) RK73Z2BLTD
12	Resistor, 49.9 Ω, 1/4W, 1%	1206	R4	1	(Phycomp) 9C12063A49R9FKRFT
13	Test point, black		TP1	1	(Keystone) 5001
14	Open		J8, J9	2	
15	Jack, Banana Recptance, 0.25” dia. hole		J5, J6, J7	3	(HH Smith) 101
16	Connector, edge, SMA PCB jack		J1, J2, J4	3	(Johnson) 142−0701−801
17	Standoff, 4−40 hex, 0.625” length			4	(Keystone) 1804
18	Screw, Phillips, 4−40, .250”			4	SHR−0440−016−SN
19	IC, THS3201		U1	1	(TI) THS3201DGN
20	Board, printed circuit			1	(TI) Edge # 6447972 Rev.A

NOTE: The components shown in the BOM were used in test by TI.

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This is particularly true for video and R_F-amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the THS3201 is available through either the Texas Instruments web site (www.ti.com) or as one model on a disk from the Texas Instruments Product Information Center (1–800–548–6132). The PIC is also available for design assistance and detailed product information at this number. These models do a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. They are not intended to model the distortion characteristics of the amplifier, nor do they attempt to distinguish between the package types in their small-signal ac performance. Detailed information about what is and is not modeled is contained in the model file itself.

ADDITIONAL REFERENCE MATERIAL

PowerPAD Made Easy, application brief (SLMA004)

PowerPAD Thermally Enhanced Package, technical brief (SLMA002)

Voltage Feedback vs. Current Feedback amplifiers, (SLVA051)

Current Feedback Analysis and Compensation (SLOA021)

Current Feedback Amplifiers: Review, Stability, and Application (SBOA081)

Effect of parasitic capacitance in op amp circuits (SLOA013)

PACKAGING INFORMATION

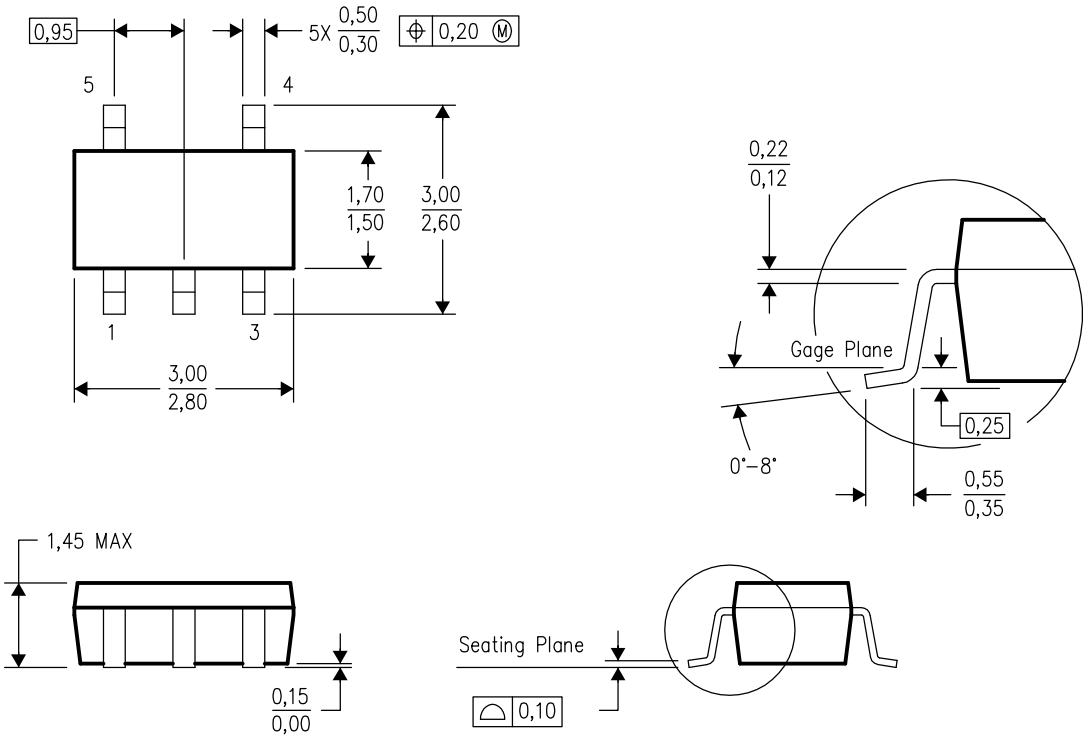
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
THS3201D	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
THS3201DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DGK	ACTIVE	MSOP	DGK	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
THS3201DR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

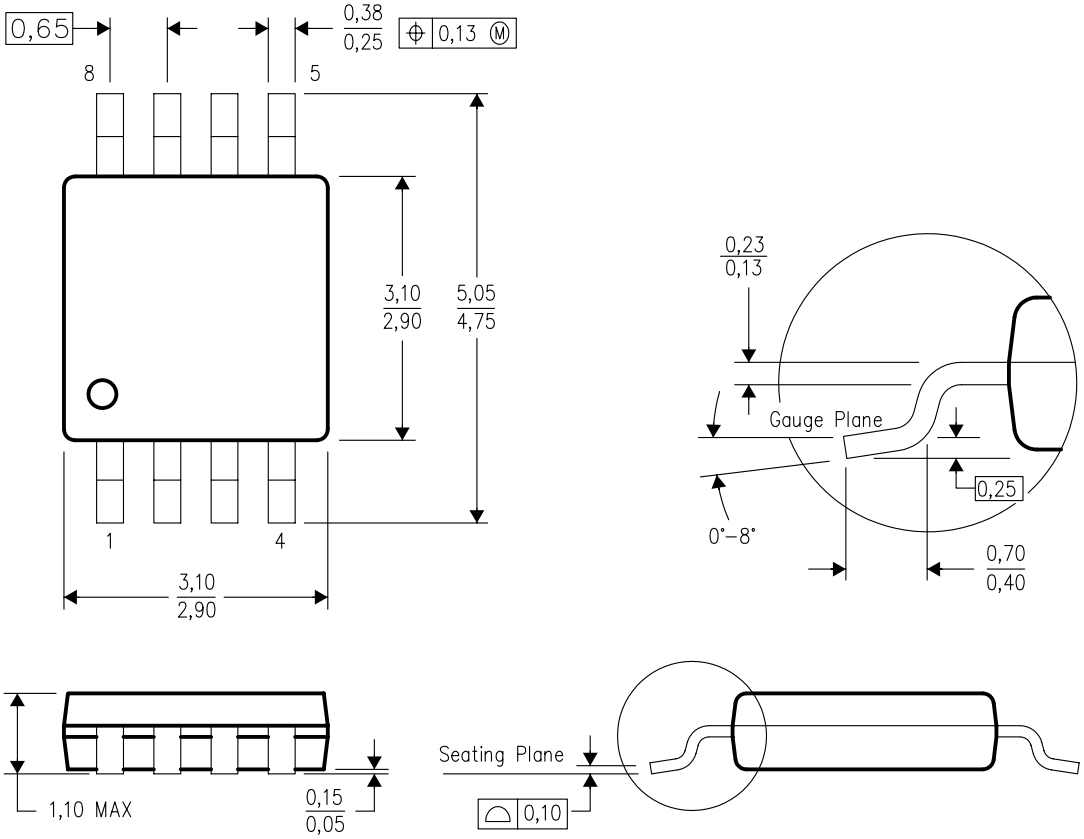
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/H 10/2003

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–178 Variation AA.

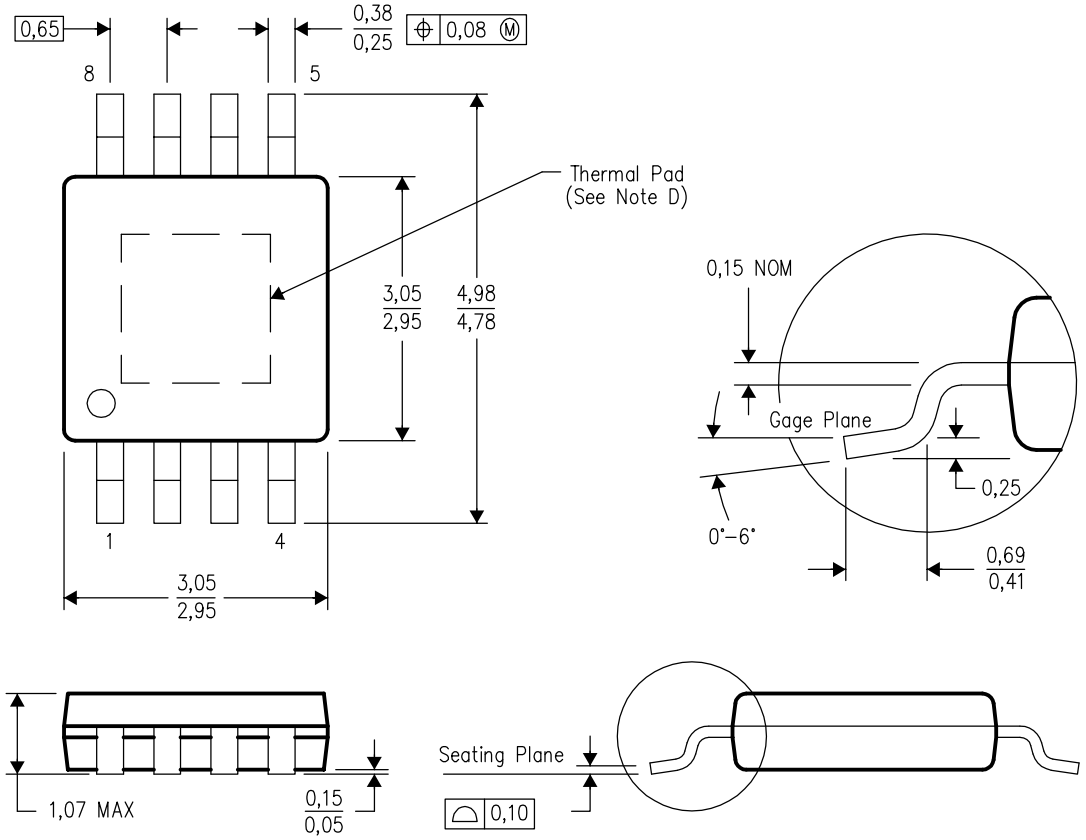
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/D 12/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation AA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

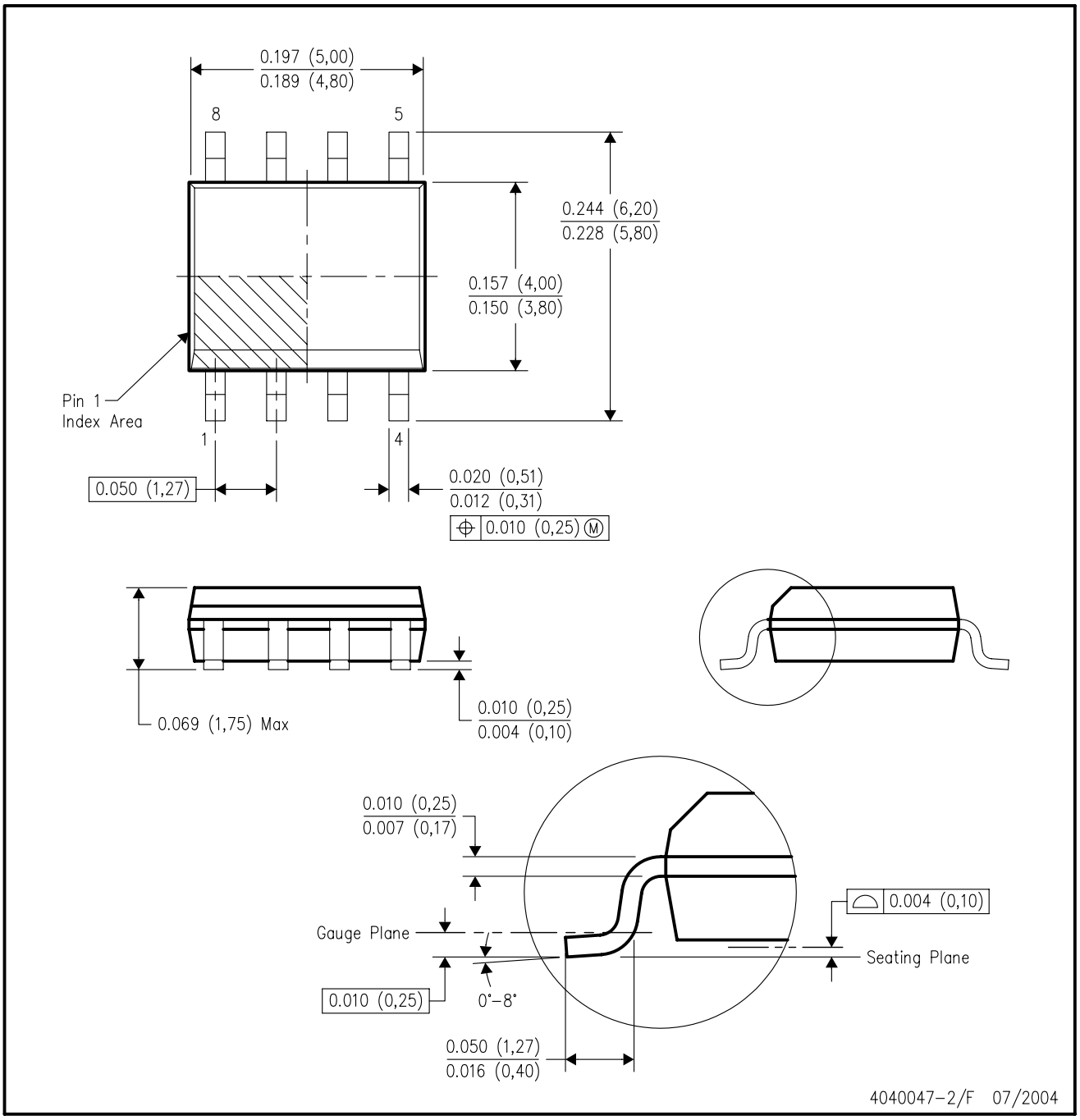


4073271/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

PowerPAD is a trademark of Texas Instruments.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265