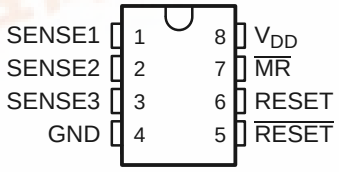
TRIPLE PROCESSOR SUPERVISORS

FEATURES

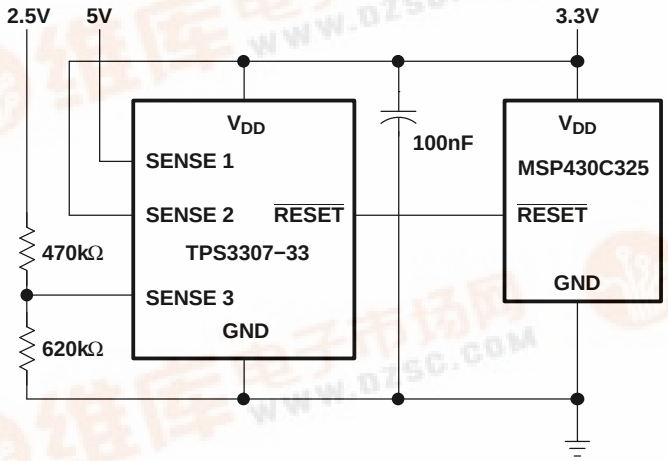
- Triple Supervisory Circuits for DSP and Processor-Based Systems
- Power-On Reset Generator With Fixed Delay Time of 200ms, No External Capacitor Needed
- Temperature-Compensated Voltage Reference
- Maximum Supply Current of 40µA
- Supply Voltage Range: 2V to 6V
- Defined $\overline{\text{RESET}}$ Output From $V_{DD} \geq 1.1V$
- MSOP-8 and SO-8 Packages
- Temperature Range : – 40°C to 85°C

D OR DGN PACKAGE
(TOP VIEW)



Typical Applications

Figure 1 lists some of the typical applications for the TPS3307 family, and a schematic diagram for a processor-based system application. This application uses TI part numbers TPS3307-33 and MSP430C325.



- Applications using DSPs, Microcontrollers or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Portable/Battery Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Notebook/Desktop Computers

Figure 1. Applications Using the TPS3307 Family

DESCRIPTION

The TPS3307 family is a series of micropower supply voltage supervisors designed for circuit initialization primarily in DSP and processor-based systems, which require more than one supply voltage.

The product spectrum of the TPS3307-xx is designed for monitoring three independent supply voltages: 3.3V/1.8V/adj, 3.3V/2.5V/adj or 3.3V/5V/adj. The adjustable SENSE input allows the monitoring of any supply voltage >1.25V.

The various supply voltage supervisors are designed to monitor the nominal supply voltage as shown in the following supply voltage monitoring table.

During power-on, $\overline{\text{RESET}}$ is asserted when the supply voltage V_{DD} becomes higher than 1.1V. Thereafter, the supply voltage supervisor monitors the SENSE*n* inputs and keeps $\overline{\text{RESET}}$ active as long as SENSE*n* remain below the threshold voltage V_{IT+}.

An internal timer delays the return of the $\overline{\text{RESET}}$ output to the inactive state (high) to ensure proper system reset. The delay time, $t_{d\ (typ)}$ = 200ms, starts after all SENSE*n* inputs have risen above the threshold voltage V_{IT+}. When the voltage at any SENSE input drops below the threshold voltage V_{IT-}, the $\overline{\text{RESET}}$ output becomes active (low) again.

The TPS3307-xx family of devices incorporates a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. In addition to the active-low $\overline{\text{RESET}}$ output, the TPS3307-xx family includes an active-high RESET output.

The devices are available in either 8-pin MSOP or standard 8-pin SO packages.

The TPS3307-xx devices are characterized for operation over a temperature range of –40°C to 85°C.

SUPPLY VOLTAGE MONITORING

DEVICE	NOMINAL SUPERVISED VOLTAGE			THRESHOLD VOLTAGE (TYP)		
	SENSE1	SENSE2	SENSE3	SENSE1	SENSE2	SENSE3
TPS3307-18	3.3V	1.8V	User defined	2.93V	1.68V	1.25V(1)
TPS3307-25	3.3V	2.5V	User defined	2.93V	2.25V	1.25V(1)
TPS3307-33	5V	3.3V	User defined	4.55V	2.93V	1.25V(1)

(1) The actual sense voltage has to be adjusted by an external resistor divider according to the application requirements.

AVAILABLE OPTIONS

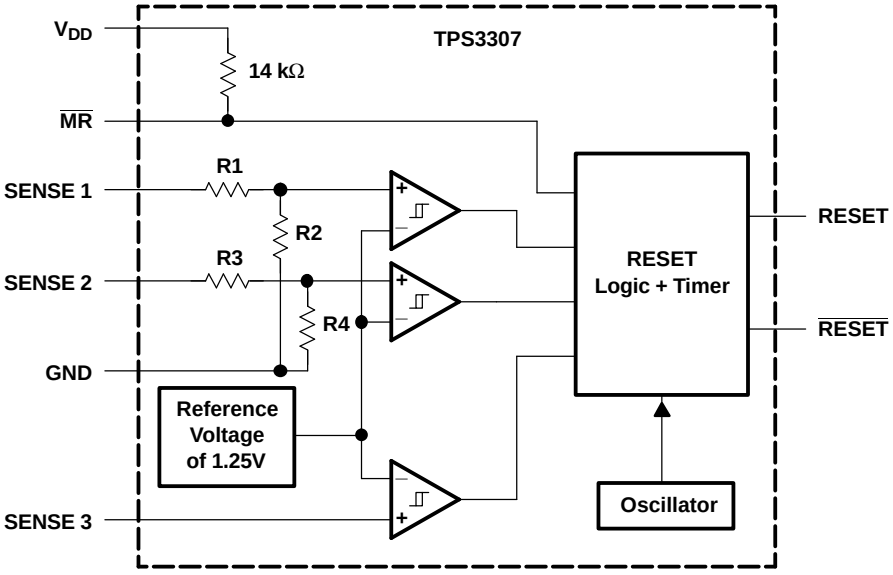
T_A	PACKAGED DEVICES		MARKING DGN PACKAGE	CHIP FORM (Y)
	SMALL OUTLINE (D)	PowerPAD™ µ-SMALL OUTLINE (DGN)		
-40°C to 85°C	TPS3307-18D	TPS3307-18DGN	TIAAP	TPS3307-18Y
	TPS3307-25D	TPS3307-25DGN	TIAAQ	TPS3307-25Y
	TPS3307-33D	TPS3307-33DGN	TIAAR	TPS3307-33Y

FUNCTION/TRUTH TABLES

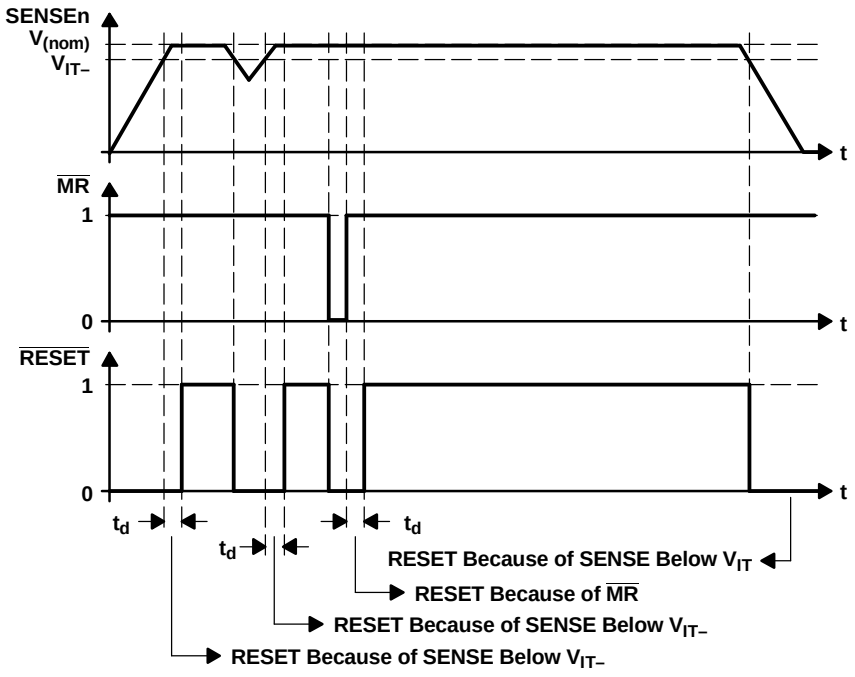
$\overline{\text{MR}}$	SENSE1 > V_{IT1}	SENSE2 > V_{IT2}	SENSE3 > V_{IT3}	$\overline{\text{RESET}}$	RESET
L	X(1)	X(1)	X	L	H
H	0	0	0	L	H
H	0	0	1	L	H
H	0	1	0	L	H
H	0	1	1	L	H
H	1	0	0	L	H
H	1	0	1	L	H
H	1	1	0	L	H
H	1	1	1	H	L

(1) X = Don't care

Functional Block Diagram

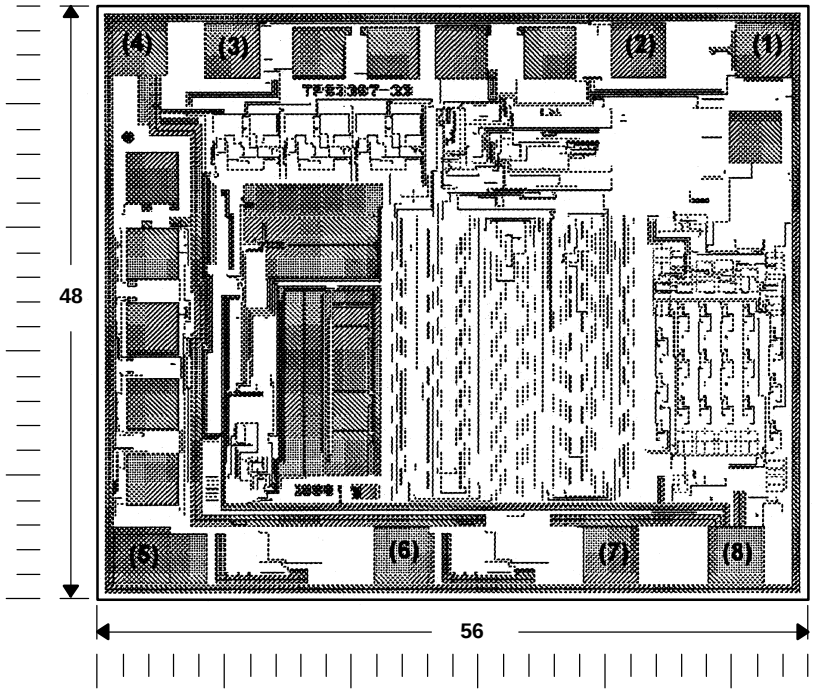


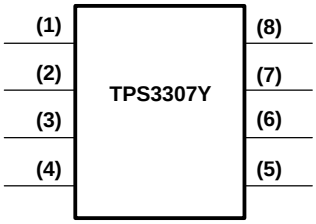
Timing Diagram



TPS3307Y Chip Information

These chips, when properly assembled, display characteristics similar to those of the TPS3307. Thermal compression or ultrasonic bonding may take place on the doped aluminium bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.





CHIP THICKNESS: 10 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_J max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	4		Ground
$\overline{MR}$	7	I	Manual reset
$\overline{RESET}$	5	O	Active-low reset output
RESET	6	O	Active-high reset output
SENSE1	1	I	Sense voltage input 1
SENSE2	2	I	Sense voltage input 2
SENSE3	3	I	Sense voltage input 3
V_{DD}	8		Supply voltage

Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted).

	UNIT
Supply voltage, V_{DD}(2)	7V
All other pins(2)	-0.3V to 7V
Maximum low output current, I_{OL}	5mA
Maximum high output current, I_{OH}	-5mA
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	±20mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	±20mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to 85°C
Storage temperature range, T_{stg}	-65°C to 150°C
Soldering temperature	260°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation the device must not be operated at 7V for more than t = 1000h continuously.

Dissipation Rating Table

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.14W	17.1mW/°C	1.37W	1.11W
D	725mW	5.8mW/°C	464mW	377mW

Recommended Operating Conditions

At specified temperature range.

	MIN	MAX	UNIT
Supply voltage, V_{DD}	2	6	V
Input voltage at $\overline{MR}$ and SENSE3, V_I	0	V_{DD} + 0.3	V
Input voltage at SENSE1 and SENSE2, V_I	0	$(V_{DD}+0.3)V_{IT}/1.25V$	V
High-level input voltage at $\overline{MR}$, V_{IH}	0.7 x V_{DD}		V
Low-level input voltage at $\overline{MR}$, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{MR}$, $\Delta t/\Delta V$		50	ns/V
Operating free-air temperature range, T_A	-40	85	°C

Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{DD} = 2V to 6V, I_{OH} = -20 µA	V_{DD} - 0.2V			V
			V_{DD} = 3.3V, I_{OH} = -2mA	V_{DD} - 0.4V			
			V_{DD} = 6V, I_{OH} = -3mA	V_{DD} - 0.4V			
V_{OL}	Low-level output voltage		V_{DD} = 2V to 6V, I_{OL} = 20µA			0.2	V
			V_{DD} = 3.3V, I_{OL} = 2mA			0.4	
			V_{DD} = 6V, I_{OL} = 3mA			0.4	
	Power-up reset voltage(1)		$V_{DD} \geq$ 1.1V, I_{OL} = 20µA			0.4	V
V_{IT-}	Negative-going input threshold voltage(2)	VSENSE3	V_{DD} = 2V to 6V, T_A = 0°C to 85°C	1.22	1.25	1.28	V
		VSENSE1, VSENSE2		1.64	1.68	1.72	
				2.20	2.25	2.30	
				2.86	2.93	3	
				4.46	4.55	4.64	
		VSENSE3	V_{DD} = 2V to 6V, T_A = -40°C to 85°C	1.22	1.25	1.29	V
		VSENSE1, VSENSE2		1.64	1.68	1.73	V
				2.20	2.25	2.32	
				2.86	2.93	3.02	
				4.46	4.55	4.67	
V_{hys}	Hysteresis at VSENSEn input		V_{IT-} = 1.25V		10		mV
			V_{IT-} = 1.68V		15		
			V_{IT-} = 2.25V		20		
			V_{IT-} = 2.93V		30		
			V_{IT-} = 4.55V		40		
I_H	High-level input current	$\overline{MR}$	$\overline{MR}$ = 0.7 × V_{DD}, V_{DD} = 6 V		-130	-180	µA
		SENSE1	VSENSE1 = V_{DD} = 6V		5	8	
		SENSE2	VSENSE2 = V_{DD} = 6V		6	9	
		SENSE3	VSENSE3 = V_{DD}	-25		25	nA
I_L	Low-level input current	$\overline{MR}$	$\overline{MR}$ = 0V, V_{DD} = 6V		-430	-600	µA
		SENSEn	VSENSE1,2,3 = 0V	-25		25	nA
I_{DD}	Supply current					40	µA
C_i	Input capacitance		V_I = 0V to V_{DD}		10		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geq$ 15µs/V

(2) To ensure best stability of the threshold voltage, a bypass capacitor (ceramic 0.1µF) should be placed close to the supply terminals.

Timing Requirements

At V_{DD} = 2V to 6V, R_L = 1MΩ, C_L = 50pF, T_A = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	SENSEn	$V_{SENSEnL} = V_{IT-} - 0.2V$, $V_{SENSEnH} = V_{IT+} + 0.2V$	6			µs
		$\overline{MR}$	$V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$	100			ns

Switching Characteristics

At V_{DD} = 2V to 6V, R_L = 1MΩ, C_L = 50pF, T_A = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$. See Timing Diagram.	140	200	280	ms
t_{PHL}	Propagation (delay) time, high-to-low level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET	$V_{I(SENSEn)} \geq V_{IT+} + 0.2V$, $V_{IH} = 0.7 \times V_{DD}$, $V_{IL} = 0.3 \times V_{DD}$		200	500	ns
t_{PLH}	Propagation (delay) time, low-to-high level output	$\overline{MR}$ to $\overline{RESETMR}$ to RESET					
t_{PHL}	Propagation (delay) time, high-to-low level output	SENSEn to $\overline{RESET}$ SENSEn to RESET	$V_{IH} = V_{IT+} + 0.2V$, $V_{IL} = V_{IT-} - 0.2V$, $\overline{MR} \geq 0.7 \times V_{DD}$		1	5	µs
t_{PLH}	Propagation (delay) time, low-to-high level output	SENSEn to $\overline{RESET}$ SENSEn to RESET					

Typical Characteristics

NORMALIZED SENSE THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

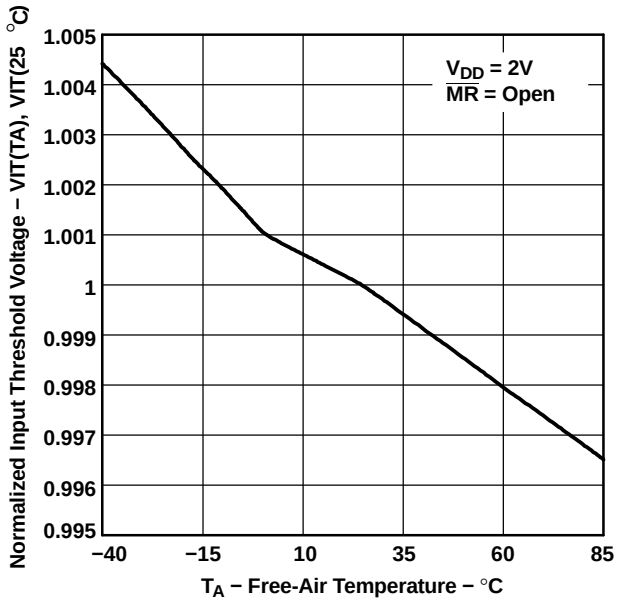


Figure 2.

SUPPLY CURRENT vs SUPPLY VOLTAGE

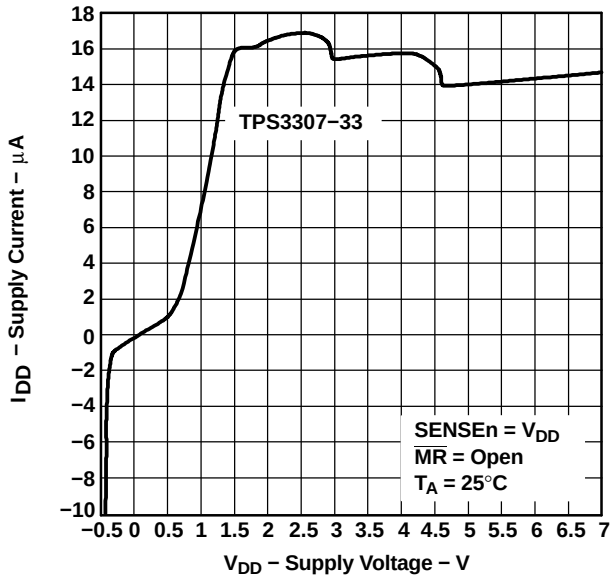


Figure 3.

INPUT CURRENT vs INPUT VOLTAGE AT $\overline{MR}$

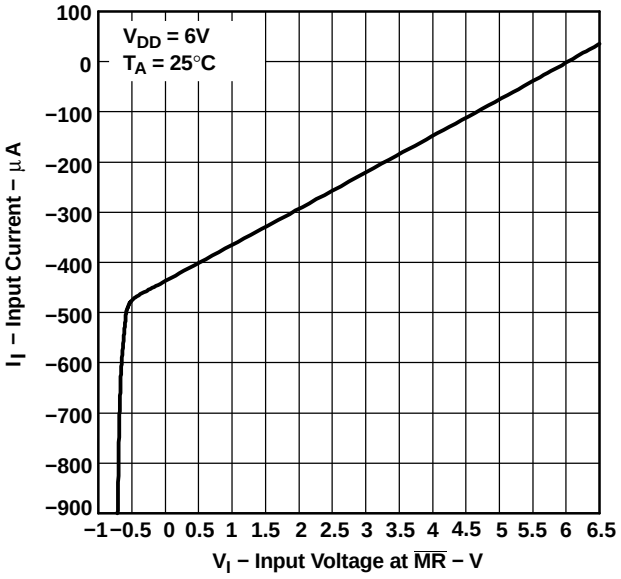


Figure 4.

MINIMUM PULSE DURATION AT SENSE vs THRESHOLD OVERDRIVE

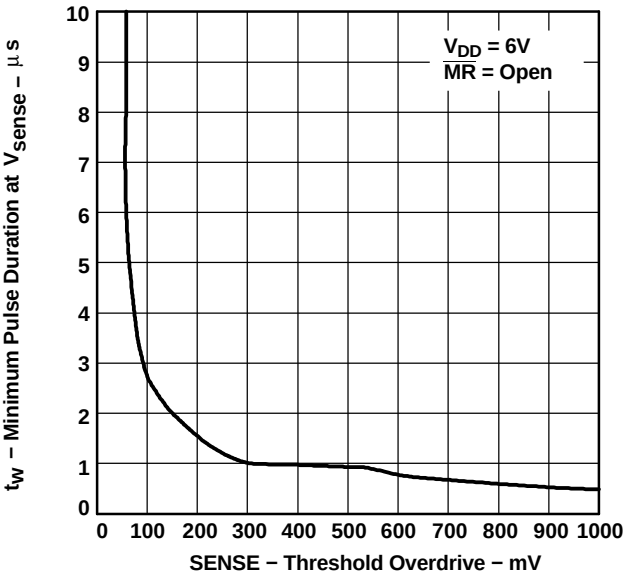


Figure 5.

Typical Characteristics (continued)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

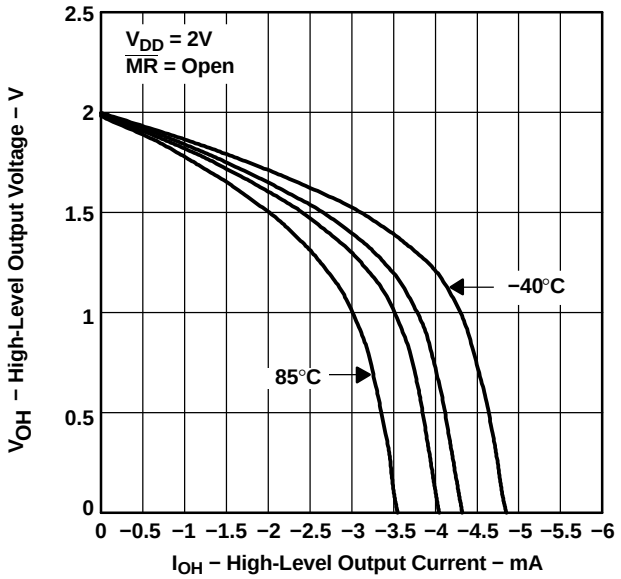


Figure 6.

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

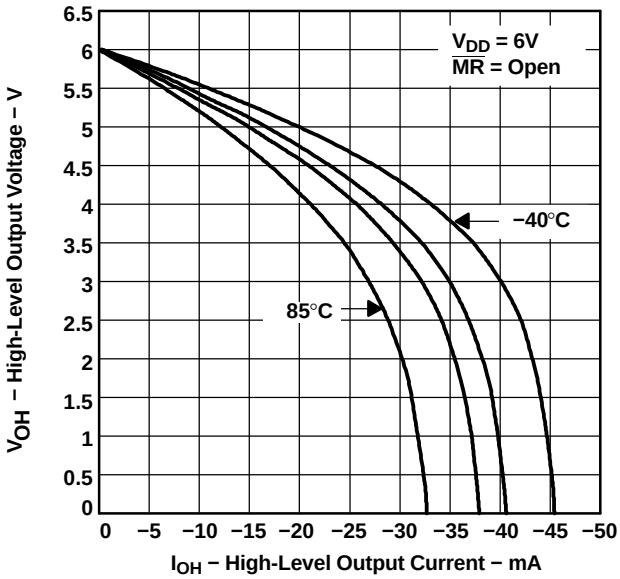


Figure 7.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

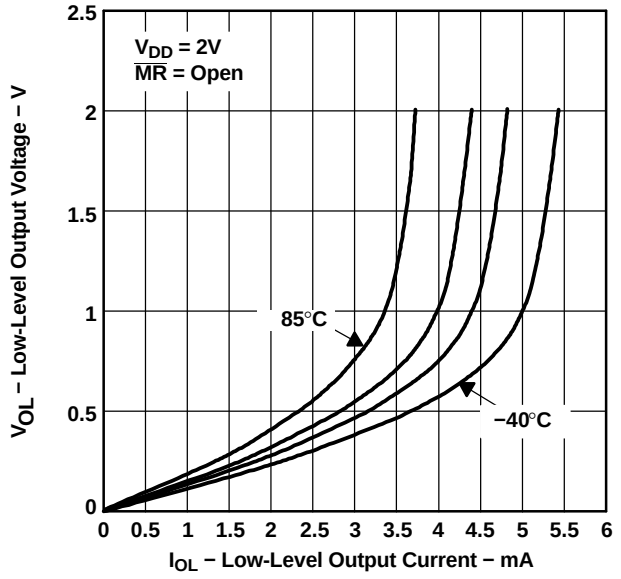


Figure 8.

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

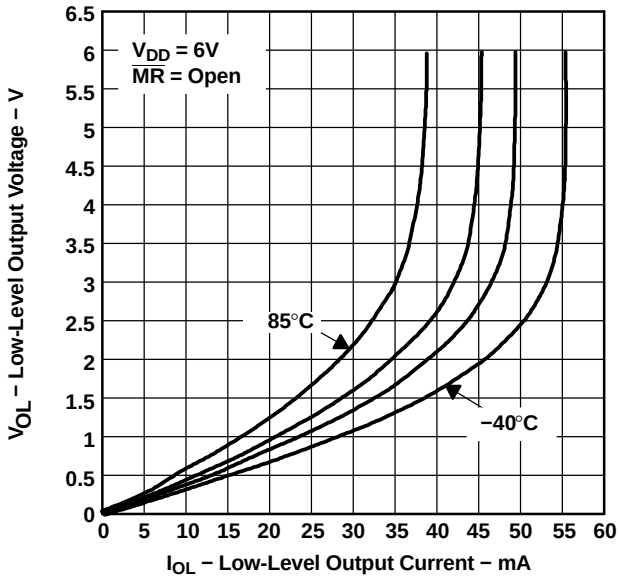


Figure 9.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3307-18D	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3307-18DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-18DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-18DR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3307-18DRG4	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3307-25D	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3307-25DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-25DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-25DGNRG4	ACTIVE	MSOP-Power PAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3307-25DR	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3307-25DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3307-33D	ACTIVE	SOIC	D	8	75	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-33DGN	ACTIVE	MSOP-Power PAD	DGN	8	80	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-33DGNR	ACTIVE	MSOP-Power PAD	DGN	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-33DR	ACTIVE	SOIC	D	8	2500	None	CU NIPDAU	Level-1-220C-UNLIM
TPS3307-33DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

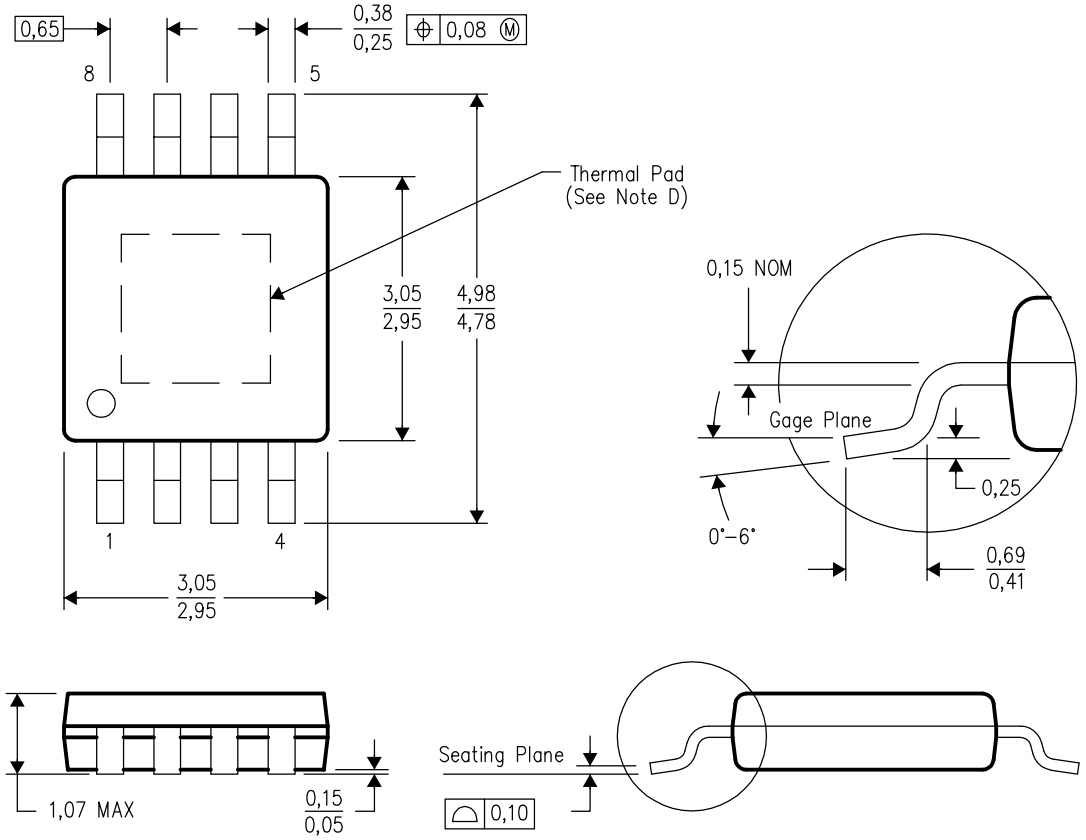
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens,

including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

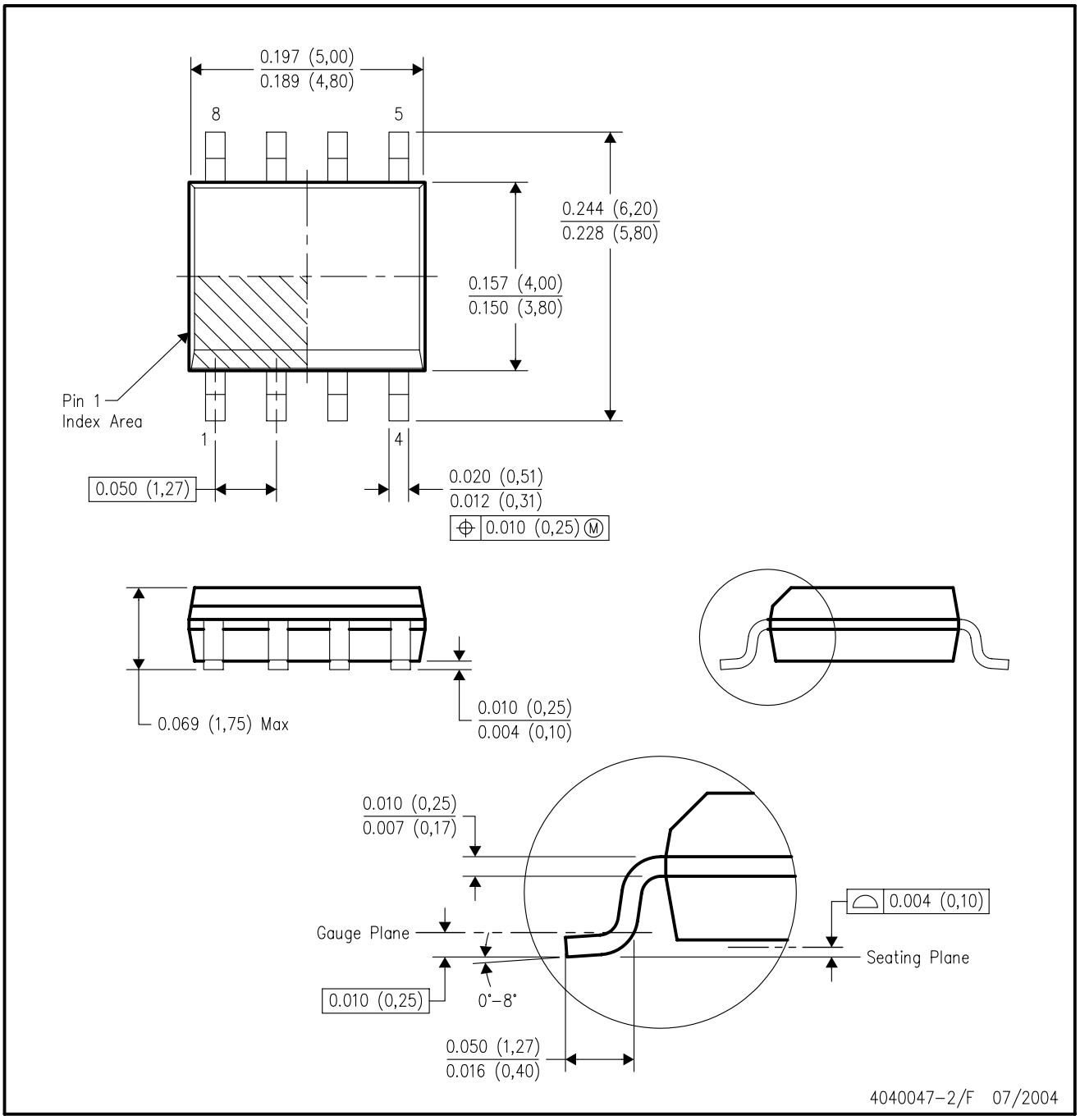


4073271/C 08/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–187

PowerPAD is a trademark of Texas Instruments.

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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