DYNEX SEMICONDUCTOR

DGT304RE

Reverse Blocking Gate Turn-off Thyristor

DS5518-2.1 February 2002

FEATURES

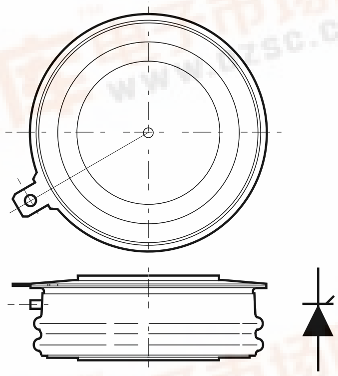
- Reverse Blocking Capability
- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

APPLICATIONS

- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters

KEY PARAMETERS

I_{TCM}	**700A**
V_{DRM}/V_{RRM}	**1300V**
$I_{T(AV)}$	**250A**
dV_D/dt	**500V/µs**
di_T/dt	**500A/µs**



Outline type code: E

(See Package Details for further information)

Fig. 1 Package outline

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V_{DRM} V	Repetitive Peak Reverse Voltage V_{RRM} V	Conditions
DGT304RE13	1300	1300	T_{vj} = 125°C, I_{DM} = 50mA, I_{RRM} = 50mA, V_{RG} = 2V

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TCM}	Repetitive peak controllable on-state current	$V_D = 60\% V_{DRM}$, $T_j = 125^oC$, $di_{GQ}/dt = 15A/\mu s$, $Cs = 2.0\mu F$	700	A
$I_{T(AV)}$	Mean on-state current	$T_{HS} = 80^oC$. Double side cooled. Half sine 50Hz.	250	A
$I_{T(RMS)}$	RMS on-state current	$T_{HS} = 80^oC$. Double side cooled. Half sine 50Hz.	390	A

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine. $T_j = 125^oC$	4.0	kA
I^2t	I^2t for fusing	10ms half sine. $T_j = 125^oC$	80000	A^2s
di_T/dt	Critical rate of rise of on-state current	$V_D = 60\% V_{DRM}$, $I_T = 700A$, $T_j = 125^oC$, $I_{FG} > 20A$, Rise time < 1.0µs	500	A/µs
dV_D/dt	Rate of rise of off-state voltage	To 80% V_{DRM}; $R_{GK} \leq 1.5\Omega$, $T_j = 125^oC$	500	V/µs

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I_{FGM}	Peak forward gate current		-	50	A
$P_{FG(AV)}$	Average forward gate power		-	10	W
P_{RGM}	Peak reverse gate power		-	6	kW
di_{GQ}/dt	Rate of rise of reverse gate current		10	50	A/µs
$t_{ON(min)}$	Minimum permissable on time		20	-	µs
$t_{OFF(min)}$	Minimum permissable off time		40	-	µs

THERMAL RATINGS

Symbol	Parameter	Conditions		Min.	Max.	Units
$R_{th(j-hs)}$	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.075	°C/W
		Anode side cooled		-	0.12	°C/W
		Cathode side cooled		-	0.20	°C/W
$R_{th(c-hs)}$	Contact thermal resistance	Clamping force 5.5kN With mounting compound	per contact	-	0.018	°C/W
T_{vj}	Virtual junction temperature			-	125	°C
T_{OP}/T_{stg}	Operating junction/storage temperature range			-40	125	°C
-	Clamping force			5.0	6.0	kN

CHARACTERISTICS

T_j = 125°C unless stated otherwise

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{TM}	On-state voltage	At 600A peak, $I_{G(ON)}$ = 2A d.c.	-	2.2	V
I_{DM}	Peak off-state current	At = V_{DRM}, V_{RG} = 2V	-	25	mA
I_{RRM}	Peak reverse current	At V_{RRM}	-	50	mA
V_{GT}	Gate trigger voltage	V_D = 24V, I_T = 100A, T_j = 25°C	-	0.9	V
I_{GT}	Gate trigger current	V_D = 24V, I_T = 100A, T_j = 25°C	-	1.0	A
I_{RGM}	Reverse gate cathode current	V_{RGM} = 16V, No gate/cathode resistor	-	50	mA
E_{ON}	Turn-on energy	V_D = 900V, I_T = 600A, dI_T/dt = 300A/µs	-	130	mJ
t_d	Delay time	I_{FG} = 20A, rise time < 1.0µs	-	1.5	µs
t_r	Rise time	R_L = (Residual inductance 3µH)	-	3.0	µs
E_{OFF}	Turn-off energy		-	350	mJ
t_{gs}	Storage time	I_T =600A, V_{DM} = 750V	-	10	µs
t_{gf}	Fall time	Snubber Cap Cs = 1.5µF,	-	11	µs
t_{gq}	Gate controlled turn-off time	di_{GQ}/dt = 15A/µs	-	0.9	µs
Q_{GQ}	Turn-off gate charge	R_L = (Residual inductance 3µH)	-	700	µC
Q_{GQT}	Total turn-off gate charge		-	1400	µC

CURVES

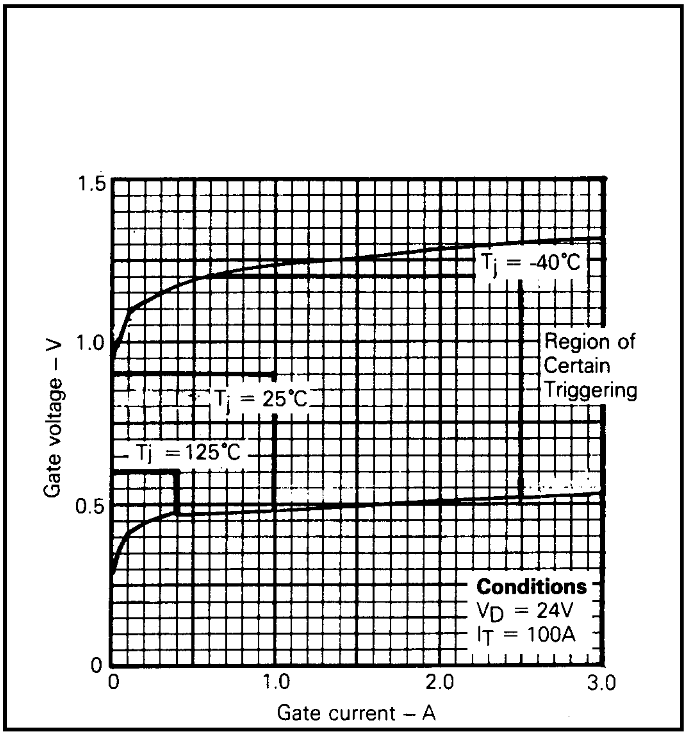


Fig.2 Gate characteristics

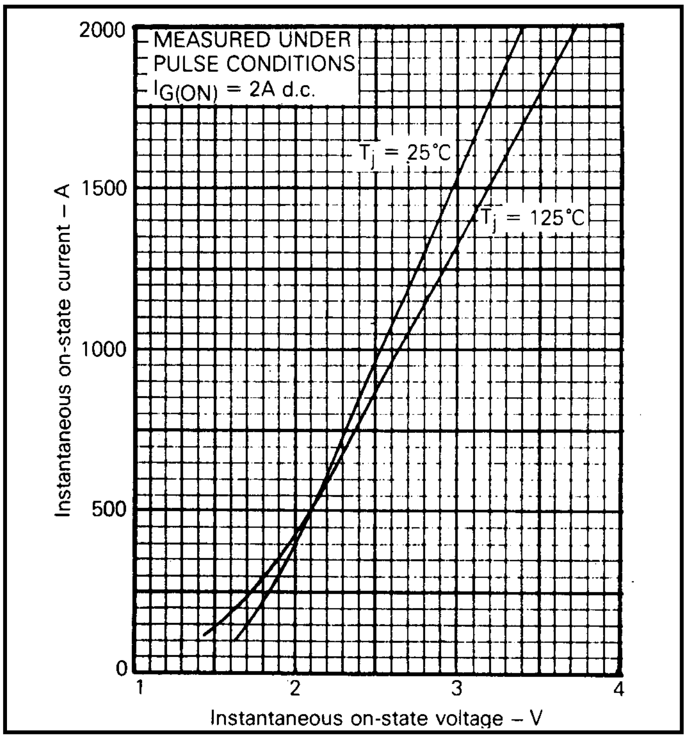


Fig.3 Maximum (limit) on-state characteristics

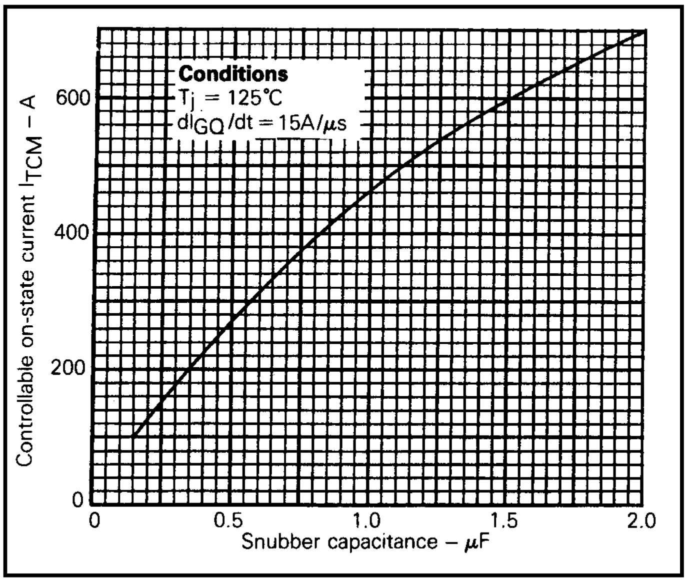


Fig.4 Dependence of I_{TCM} on C_S

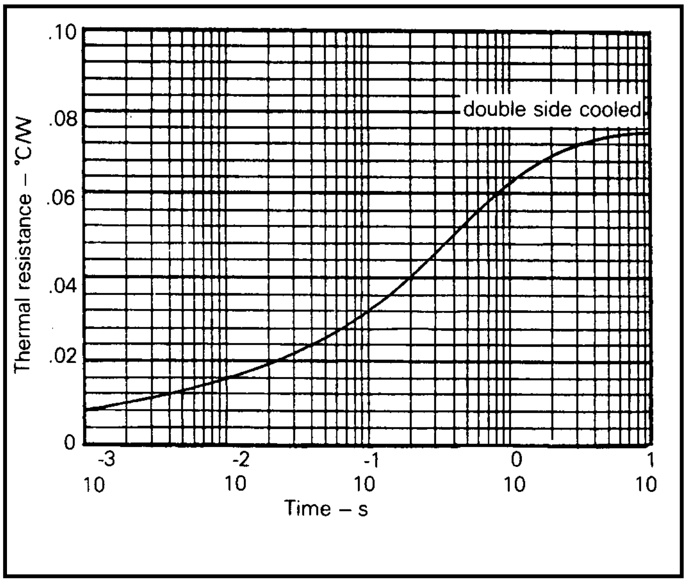


Fig.5 Maximum (limit) transient thermal resistance

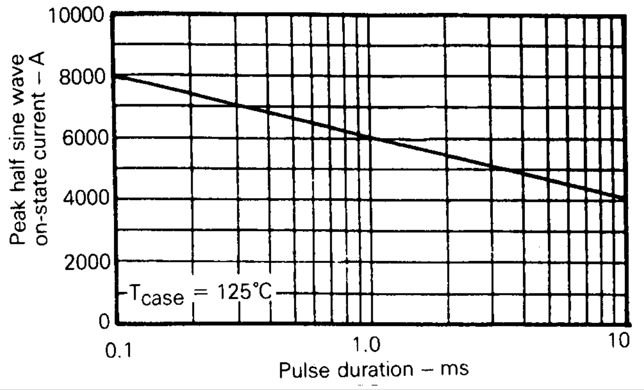


Fig.6 Surge (non-repetitive) on-state current vs time

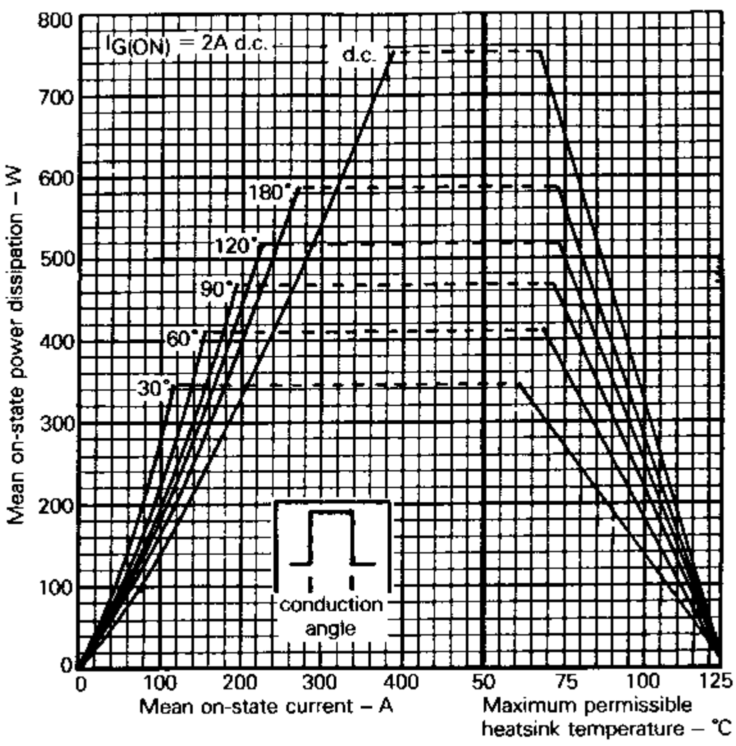


Fig.7 Steady state rectangulerwave conduction loss - double side cooled

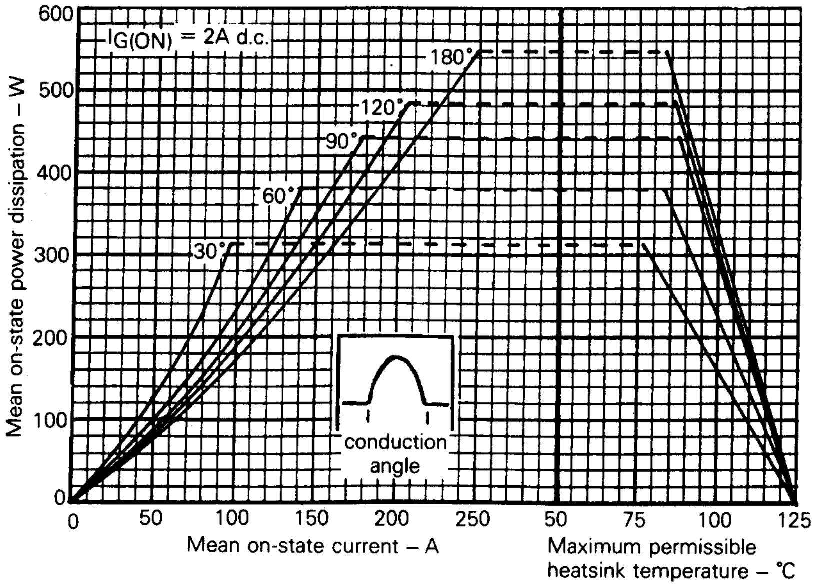


Fig.8 Steady state sinusoidal wave conduction loss - double side cooled

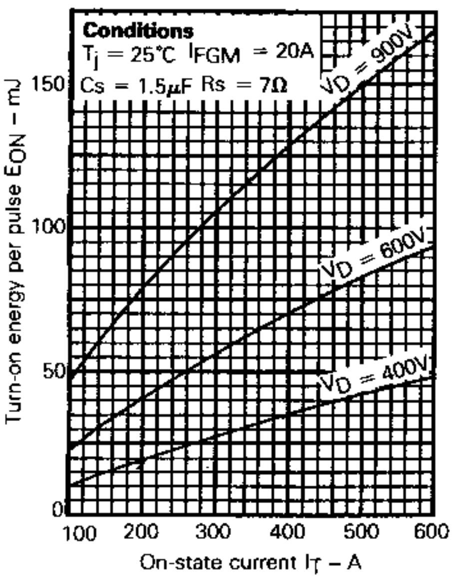


Fig.9 Turn-on energy vs on-state current

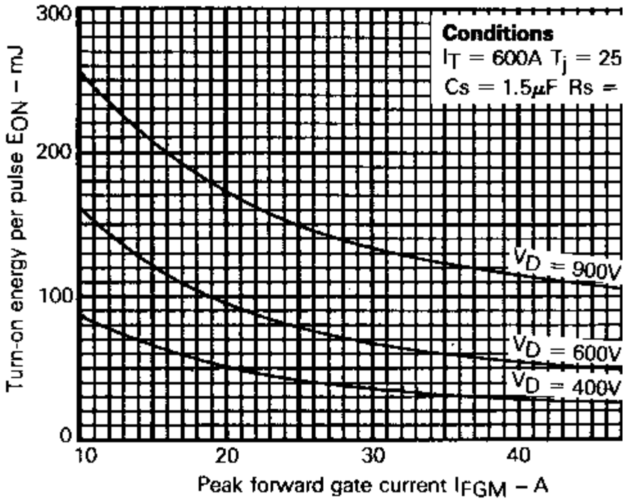


Fig.10 Turn-on energy vs peak forward gate current

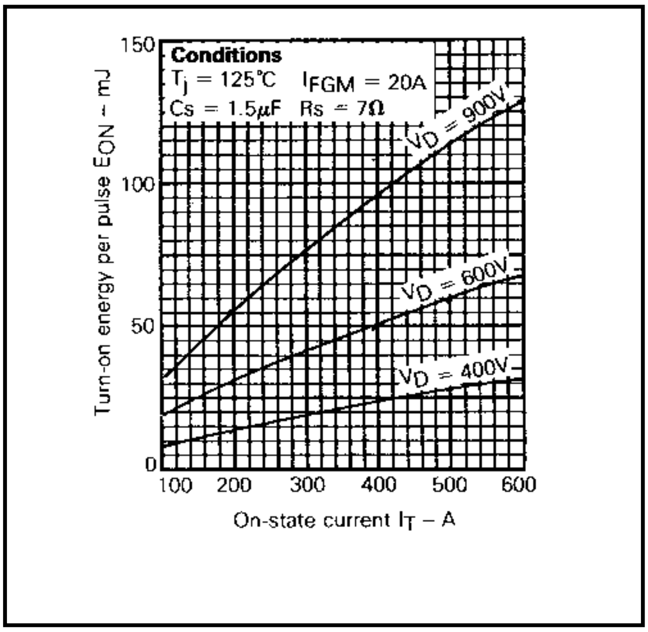


Fig.11 Turn-on energy vs on-state current

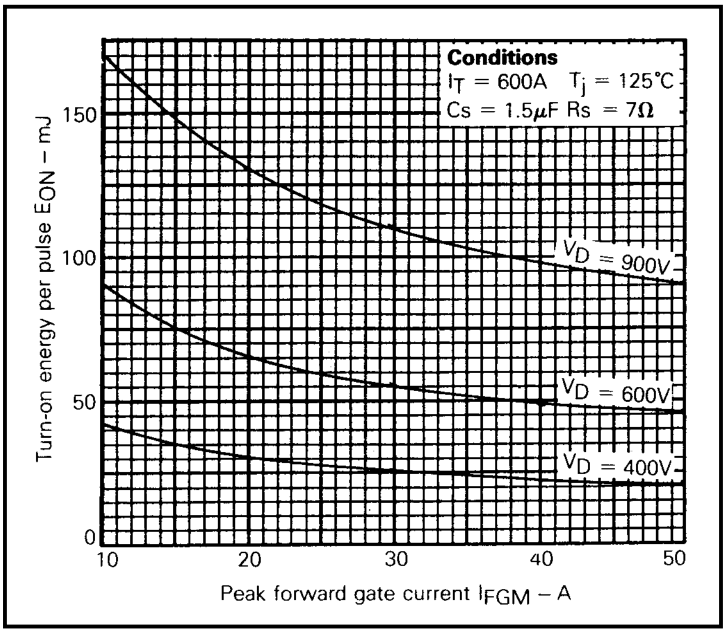


Fig.12 Turn-on energy vs peak forward gate current

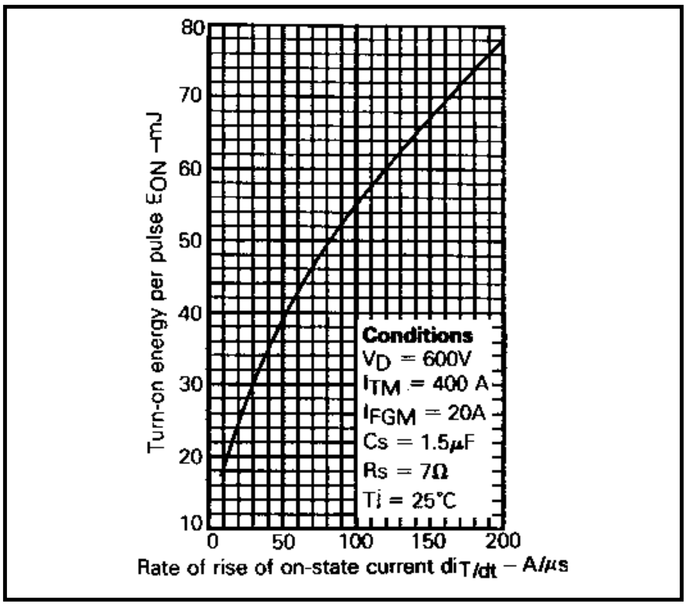


Fig.13 Turn-on energy vs rate of rise of on-state current

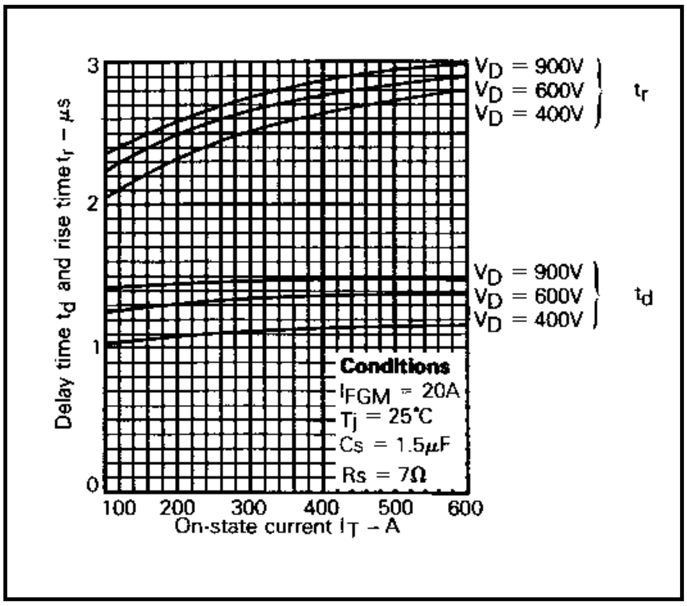


Fig.14 Delay time and rise time vs on-state current

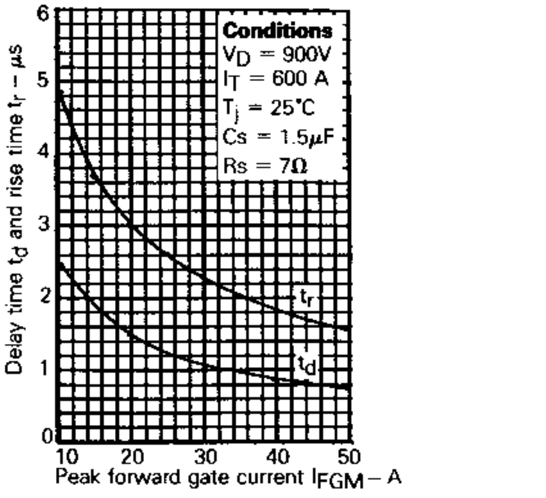


Fig.15 Delay time and rise time vs peak forward gate current

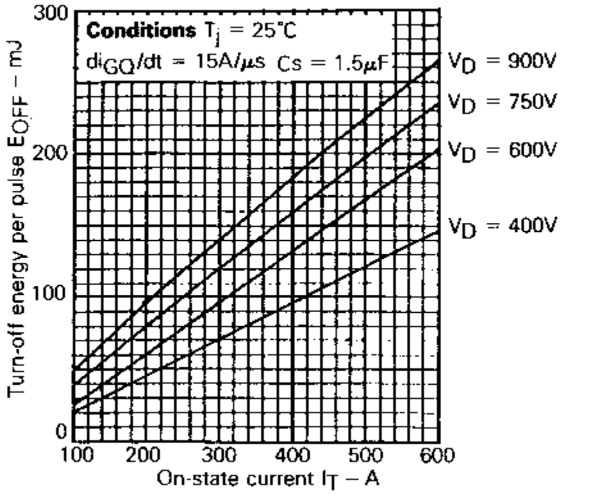


Fig.16 Turn-off energy vs on-state current

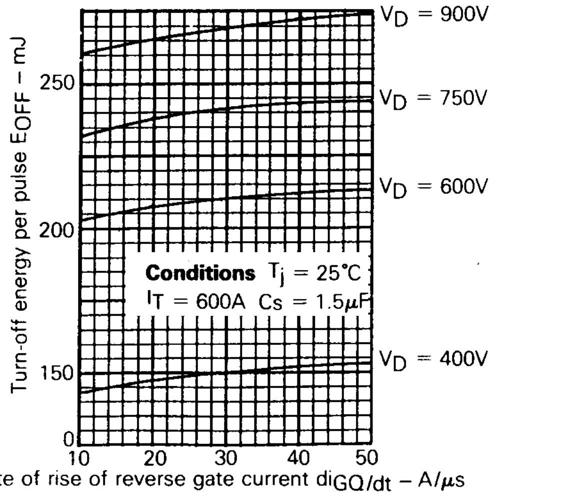


Fig.17 Turn-off energy vs rate of rise of reverse gate current

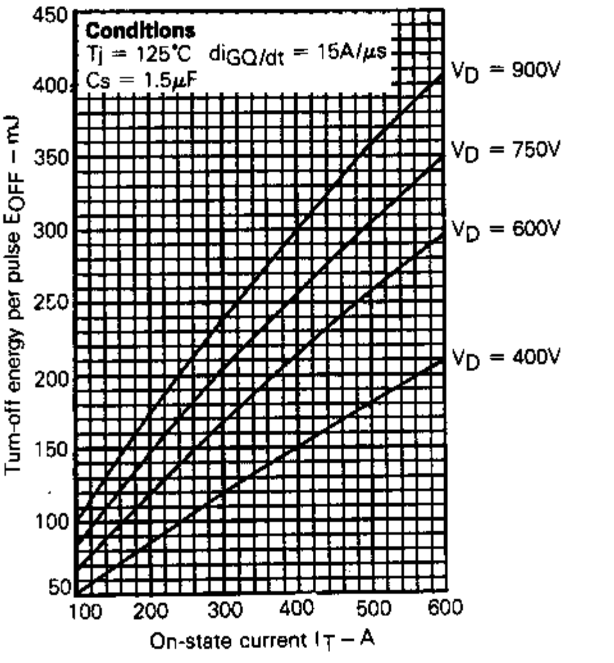


Fig.18 Turn-off energy vs on-state current

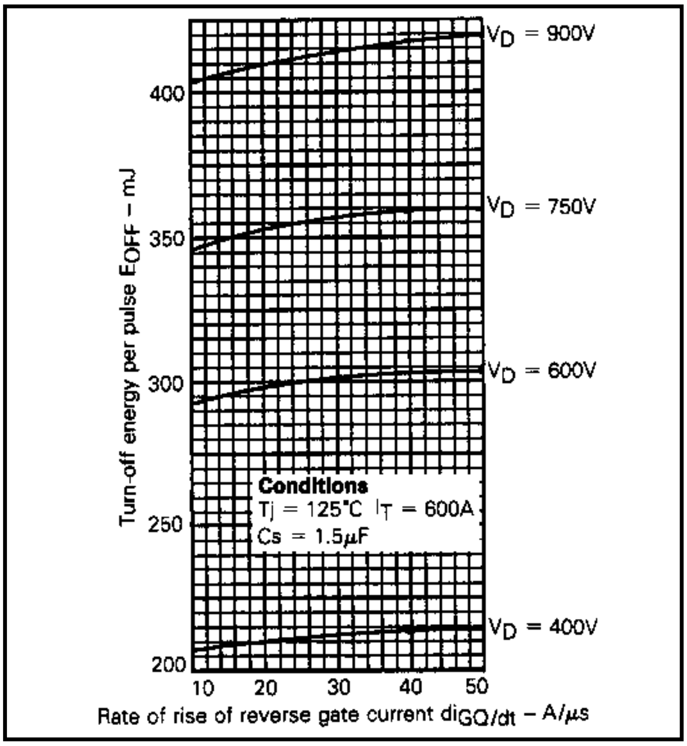


Fig.19 Turn-off energy vs rate of rise of reverse gate current

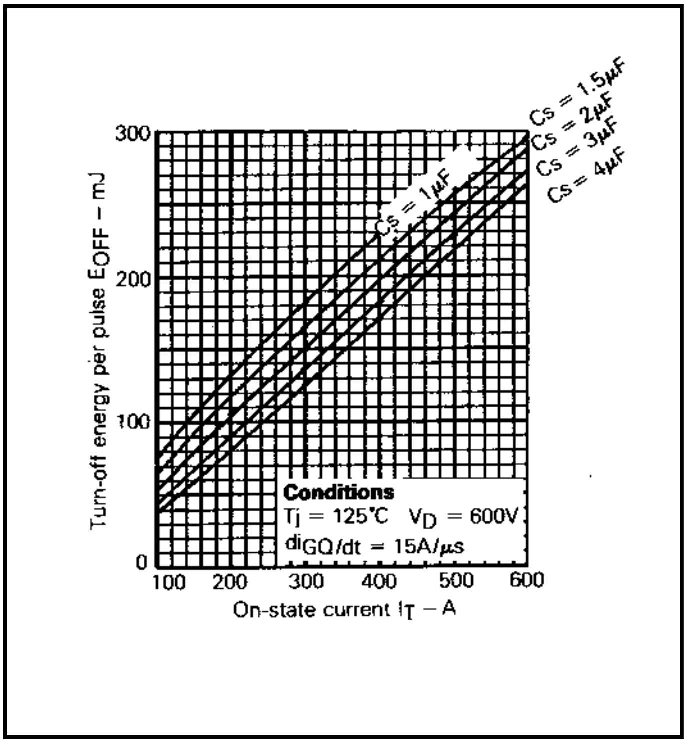


Fig.20 Turn-off energy vs on-state current with C_S as parameter

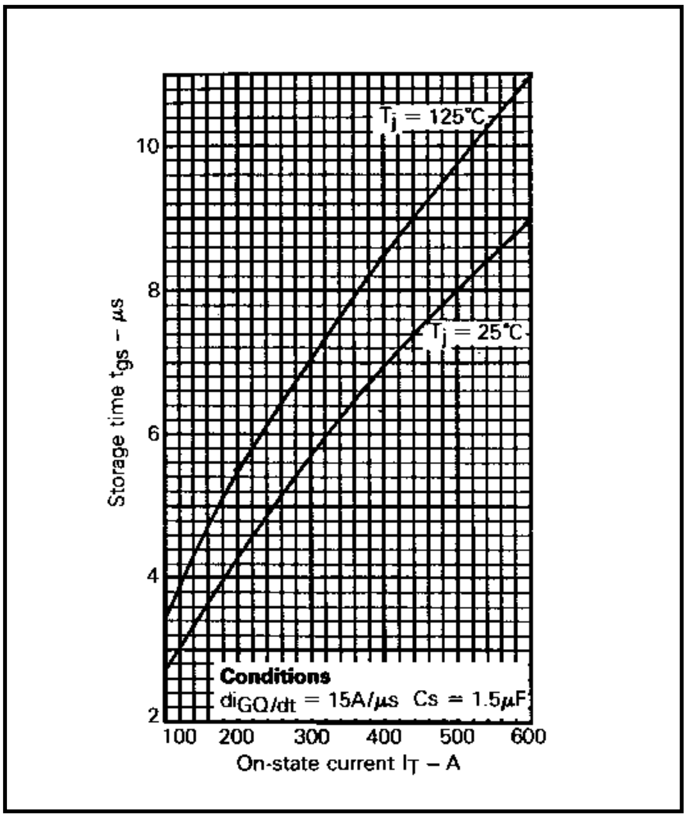


Fig.21 Storage time vs on-state current

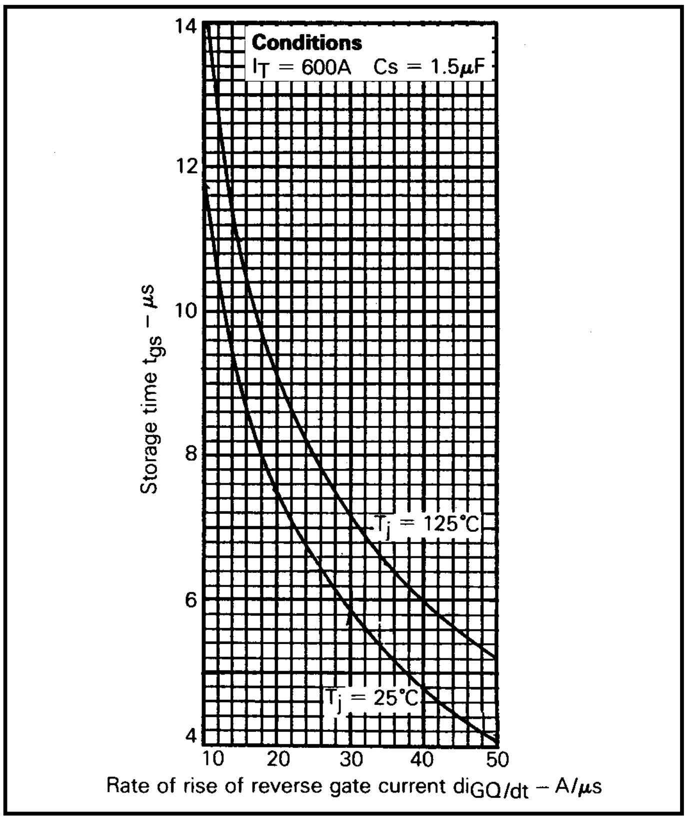


Fig.22 Storage time vs rate of rise of reverse gate current

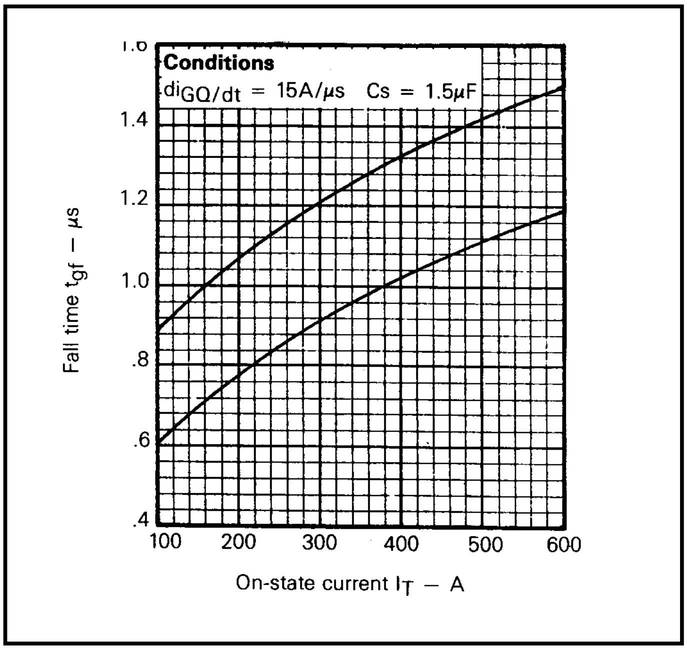


Fig.23 Fall time vs on-state current

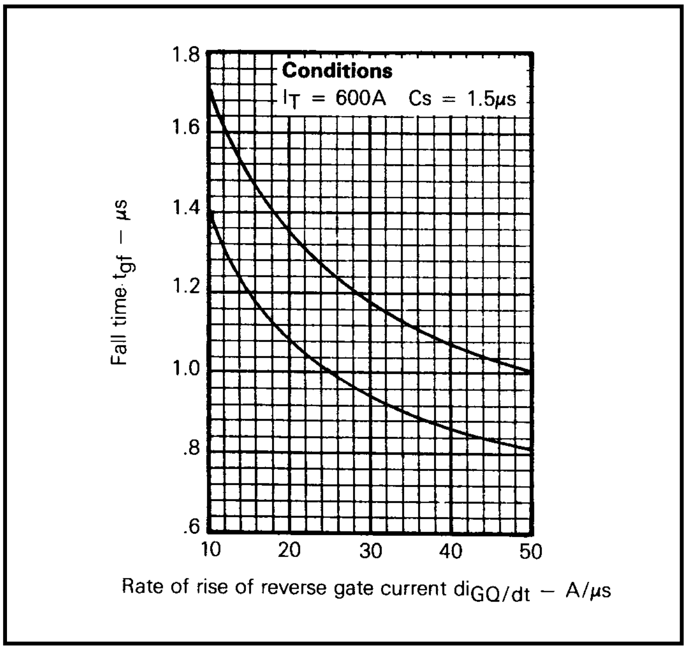


Fig.24 Fall time vs rate of rise of reverse gate current

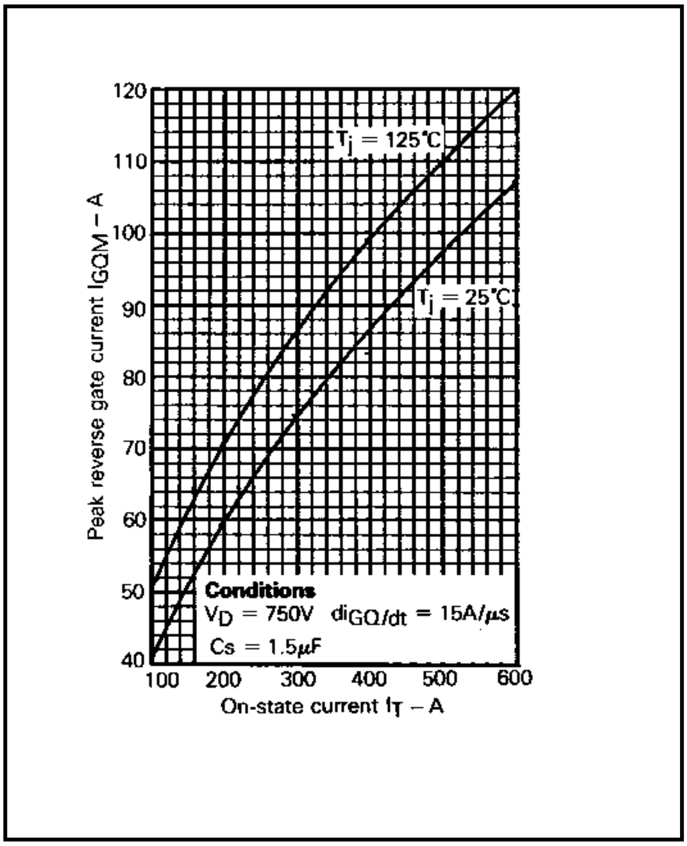


Fig.25 Peak reverse gate current vs on-state current

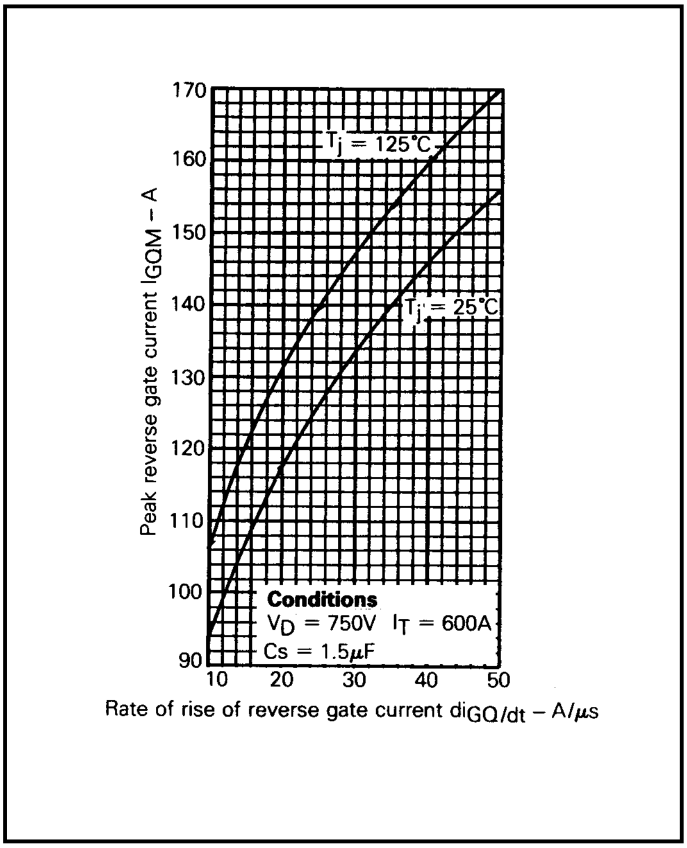


Fig.26 Peak reverse gate current vs rate of rise of reverse gate current

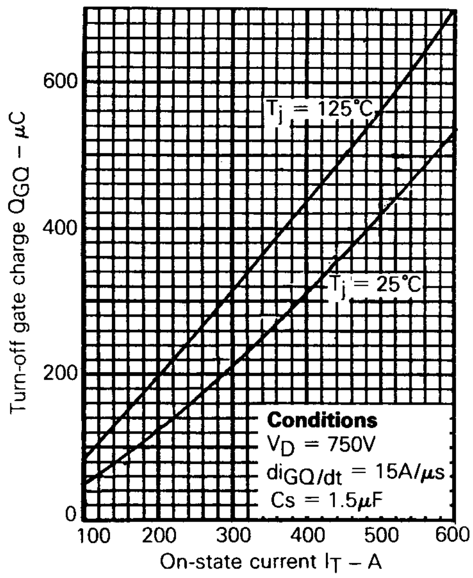


Fig.27 Turn-off gate charge vs on-state current

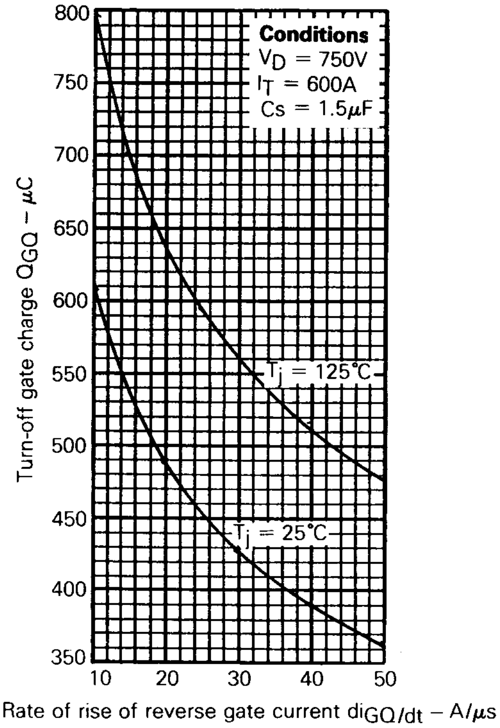


Fig.28 Turn-off gate charge vs rate of rise of reverse gate current

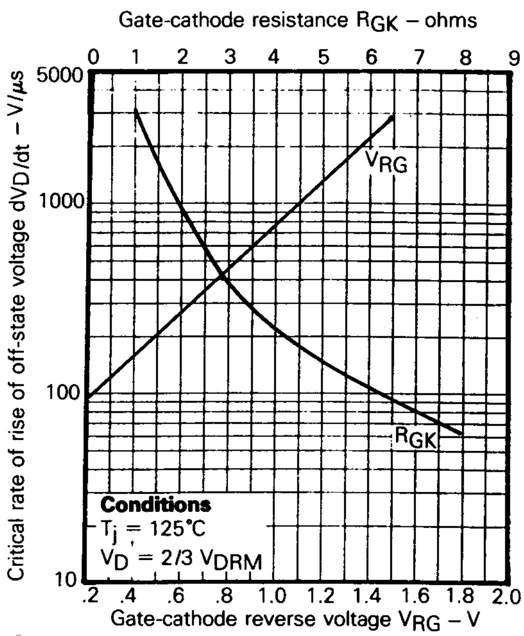
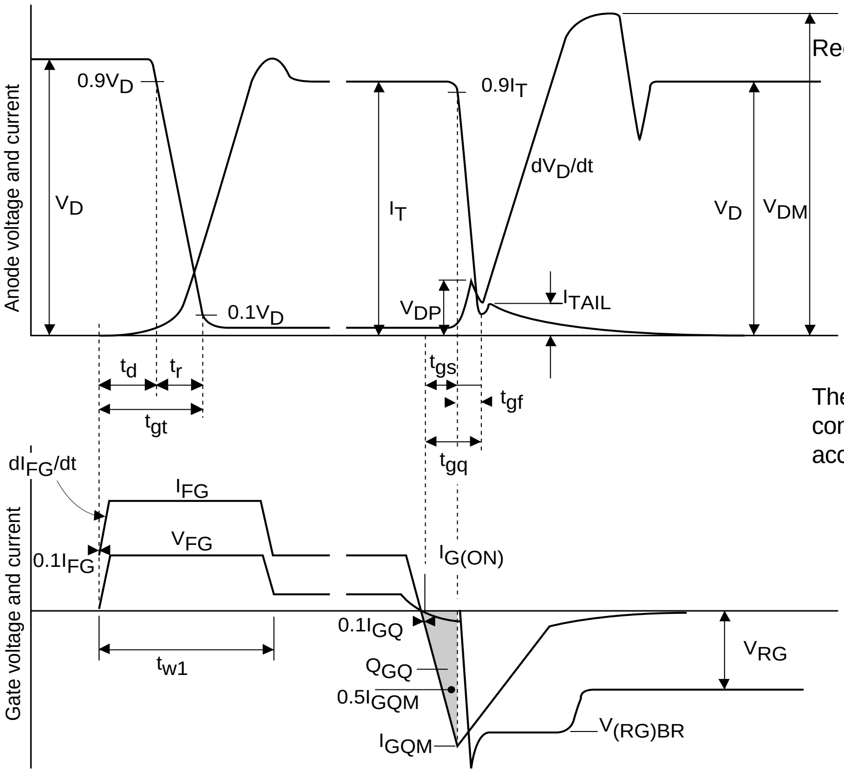


Fig.29 Dependence of critical dV_D/dt on gate-cathode resistance and gate-cathode reverse voltage

Snubber Capacitor Cs (μF)	Snubber Resistor Rs (Ω)	Minimum Reset Time (μs)
2	7	35
	5	30
1.5	7	26
	5	22
1	7	17
	5	15

Table of snubber discharge time variation with snubber capacitor value.



Recommended gate conditions:-

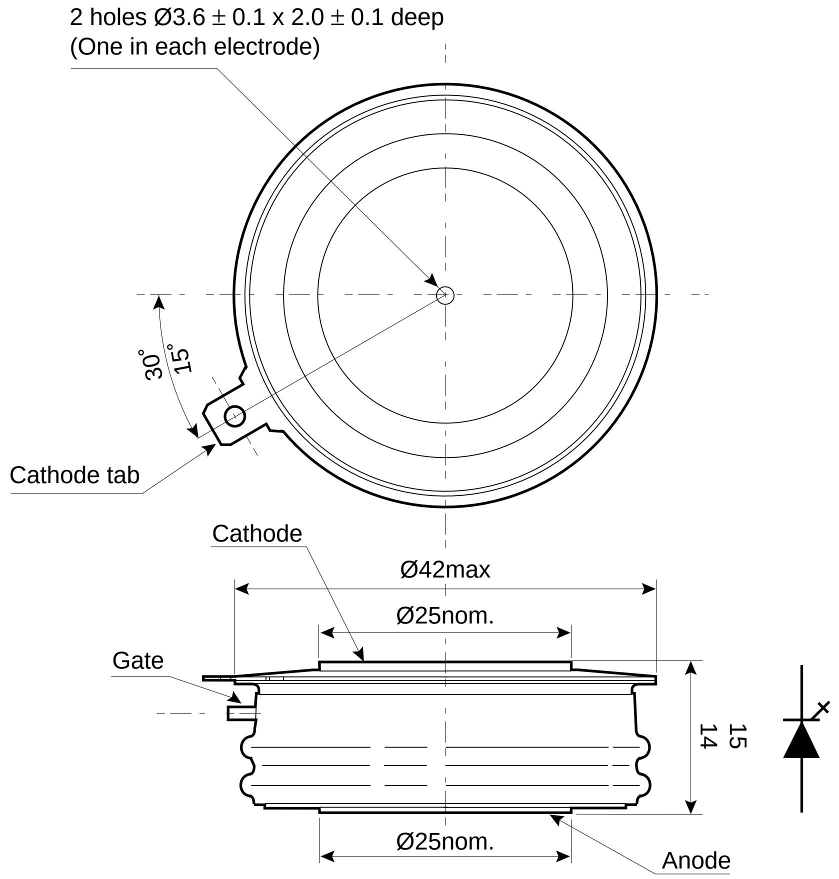
- I_{TCM} = 700A
- I_{FG} = 20A
- dI_{FG}/dt = 20A/µs
- $I_{G(ON)}$ = 2A d.c.
- $t_{w1(min)}$ = 4.5µs
- I_{GQM} = 120A
- dI_{GQ}/dt = 15A/µs
- Q_{GQ} = 700µc
- $V_{RG(min)}$ = 2V
- $V_{RG(max)}$ = 16V

These are recommended Dynex Semiconductor conditions. Other conditions are permitted according to users gate drive specifications.

Fig.30 General switching waveforms

PACKAGE DETAILS

For further package information, please visit our website or contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Nominal weight: 82g
Clamping force: 6kN ±10%

Package outine type code: E

ASSOCIATED PUBLICATIONS

Title	Application Note Number
Calculating the junction temperature or power semiconductors	AN4506
GTO gate drive units	AN4571
Recommendations for clamping power semiconductors	AN4839
Use of V_{TO}, r_T on-state characteristic	AN5001
Impoved gate drive for GTO series connections	AN5177

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group continues to offer high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

DEVICE CLAMPS

Disc devices require the correct clamping force to ensure their safe operation. The PACS range includes a varied selection of pre-loaded clamps to suit all of our manufactured devices. Types available include cube clamps for single side cooling of 'T' 23mm and 'E' 30mm discs, and bar clamps right up to 83kN for our 'Z' 100mm thyristors and diodes.

Clamps are available for single or double side cooling, with high insulation versions for high voltage assemblies.

Please refer to our application note on device clamping, AN4839

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks. They have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

http://www.dynexsemi.com

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Datasheet Annotations:

Dynex Semiconductor annotate datasheets in the top right hard corner of the front page, to indicate product status. The annotations are as follows:-

Target Information: This is the most tentative form of information and represents a very preliminary specification. No actual design work on the product has been started.

Preliminary Information: The product is in design and development. The datasheet represents the product as it is understood but details may change.

Advance Information: The product design is complete and final characterisation for volume production is well in hand.

No Annotation: The product parameters are fixed and the product is available to datasheet specification.