

September 1986 Revised February 2000

SEMICONDUCTORTM

# DM7400 Quad 2-Input NAND Gates

## **General Description**

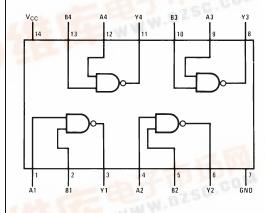
This device contains four independent gates each of which performs the logic NAND function.

## **Ordering Code:**

Order Number	Package Number	Package Description
DM7400M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM7400N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

#### **Connection Diagram**



### **Function Table**

Inp	Output	
Α	В	Y
L	L	Н
L	Н	Н
Н	L	H
Н	Н	

 $\boldsymbol{Y} = \overline{\boldsymbol{A}\boldsymbol{B}}$ 

H = HIGH Logic Level L = LOW Logic Level

## Absolute Maximum Ratings(Note 1)

Supply Voltage 7V Input Voltage 5.5V Operating Free Air Temperature Range 0°C to +70°C Storage Temperature Range -65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## **Recommended Operating Conditions**

Symbol	Parameter	Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage	4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltage	2			V
V <sub>IL</sub>	LOW Level Input Voltage			0.8	V
I <sub>OH</sub>	HIGH Level Output Current			-0.4	mA
l <sub>OL</sub>	LOW Level Output Current			16	mA
T <sub>A</sub>	Free Air Operating Temperature	0		70	°C

#### **Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -12 \text{ mA}$			-1.5	V
V <sub>OH</sub>	HIGH Level Output	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max	2.4	3.4		V
	Voltage	$V_{IL} = Max$				v
V <sub>OL</sub>	LOW Level Output	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max		0.2	0.4	V
	Voltage	$V_{IH} = Min$				
II	Input Current @ Max Input Voltage	$V_{CC} = Max, V_I = 5.5V$			1	mA
I <sub>IH</sub>	HIGH Level Input Current	$V_{CC} = Max, V_I = 2.4V$			40	μΑ
I <sub>IL</sub>	LOW Level Input Current	$V_{CC} = Max, V_I = 0.4V$			-1.6	mA
Ios	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 3)	-18		-55	mA
I <sub>CCH</sub>	Supply Current with Outputs HIGH	V <sub>CC</sub> = Max		4	8	mA
I <sub>CCL</sub>	Supply Current with Outputs LOW	V <sub>CC</sub> = Max		12	22	mA

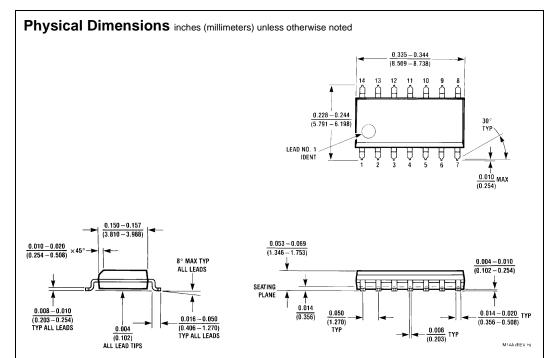
Note 2: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

Note 3: Not more than one output should be shorted at a time.

#### **Switching Characteristics**

at  $V_{CC} = 5V$  and  $T_A = 25^{\circ}C$ 

Symbol	Parameter	Conditions	Min	Max	Units
t <sub>PLH</sub>	Propagation Delay Time	C <sub>L</sub> = 15 pF		22	ns
	LOW-to-HIGH Level Output	$R_L = 400\Omega$		22	115
t <sub>PHL</sub>	Propagation Delay Time			15	ns
	HIGH-to-LOW Level Output			13	115



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow Package Number M14A

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)ก กฤก (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA $0.250 \pm 0.010$ (6.350 ± 0.254) PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{3.092}{(2.337)} \text{ DIA}$ 0.030 MAX (0.762) DEPTH OPTION 1 OPTION 02 $0.135 \pm 0.005$ 0.300 - 0.320 $(3.429 \pm 0.127)$ (7.620 - 8.128)0.145 - 0.200 0.060 4° TYP (1.651) (3.683 - 5.080)¥ $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 95° ± 5° 0.020 (0.508) 0.125 - 0.150 $0.075 \pm 0.015$ 0.280 0.014-0.023 TYP (7.112) MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 +0.040 -0.015 8.255 + 1.016

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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N14A (REV F)